

Effects of Supply Voltage and Body Bias on Variability of NEM Relay Switching Voltage

Maurice Roots^{1*}, Benjamin Osoba², Jatin Patil³, and Tsu-Jae King Liu¹

¹Department of Physics, Hampton University, Hampton, VA 23668

²Department of Electrical Engineering and Computer Sciences

³Department of Materials Science and Engineering
University of California, Berkeley, CA 94720

*E-mail: maurice.roots@my.hamptonu.edu

ABSTRACT

The Nano-Electro-Mechanical (NEM) relay is a promising switch design for ultra-low-power digital computation because it can achieve negligible off-state leakage current (to eliminate static power dissipation) and transition abruptly between ON and OFF states (to enable sub-100 mV operation). Variability in relay switching voltages can limit reductions in operating voltage, however, and therefore should be systematically quantified. In this work, the effects of the supply voltage (V_{DD}) and the body bias voltage (V_B) on variability in relay pull-in voltage (V_{PI}) and release voltage (V_{RL}) are investigated.

I. INTRODUCTION

The continuation of Moore's Law is a significant driving force in the integrated circuit (IC) industry. Continuation of this trend towards increased computing power requires great advancement in switching systems. Currently, the progress of transistor technology has met a physical limitation with thermal voltage at room temperature which prevents the scaling down of operating voltage for energy efficiency and performance. An alternative to traditional transistor switches has been demonstrated with the NEM relay. The negligible leakage current—effectively zero—of mechanical switches makes such devices a promising addition to the progression of computation strength and longevity. For NEM relays to be implemented into the IC industry their optimal operating conditions, lifespan, endurance, model, and stability need to be verified. Once IC's can be manufactured with fully optimized NEM relays, ultra-low-power computing can be mass produced. For this to be realized further research is required where this paper presents the effects of supply voltage and body bias on device performance variability for the benefit of optimization.

II. RELAY STRUCTURE AND OPERATION

The mechanical relays used in this study are a six-terminal vertically actuated design comprised of a movable electrode ("body") suspended by four folded flexures. Switching occurs when a sufficiently large voltage applied between the Body and an underlying Gate electrode causes the Channel Electrode (attached underneath the Body via an including layer) to contact Source and Drain electrodes to allow current to flow.

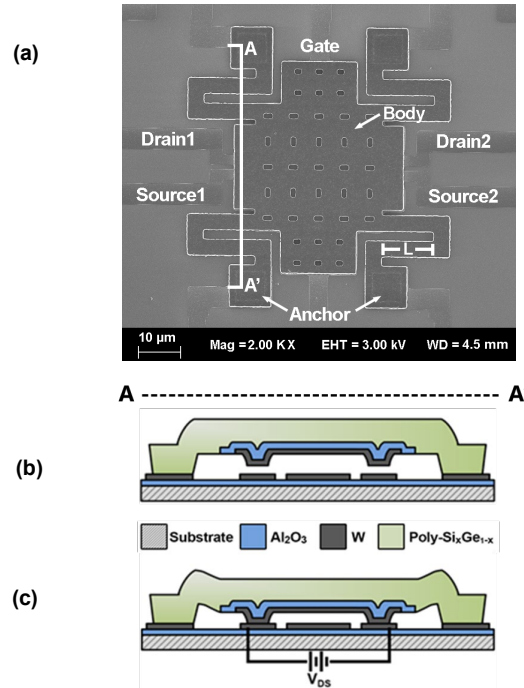


Fig. 1. (a) Scanning Electron Micrograph of the 6-Terminal relay design, with cross-section A-A' shown (b) pre-actuation and (c) post-actuation. Upon contact between the channel and S/D electrodes, surface adhesive force is introduced, thereby resulting in hysteresis.

III. METHODS

In analyzing the effects of supply voltage (V_{DD}) and body bias voltage (V_B) on variability in pull-in voltage (V_{PI}) and release voltage (V_{RL}) an approach must be designed to measure many actuations with various voltages. Methods for characterizing the effects of operating voltages on these relays is as follows: Perform one-hundred sweeps of the gate voltage (V_G) and measure the current flow through the source and drain electrodes; track V_{PI} and V_{RL} for each switching cycle.

IV. RESULTS

Data from this study further suggest that these NEM relays have promise for application into integrated circuits and ultra-low power computing. To be competitive with current transistor technology these relays must perform with steep

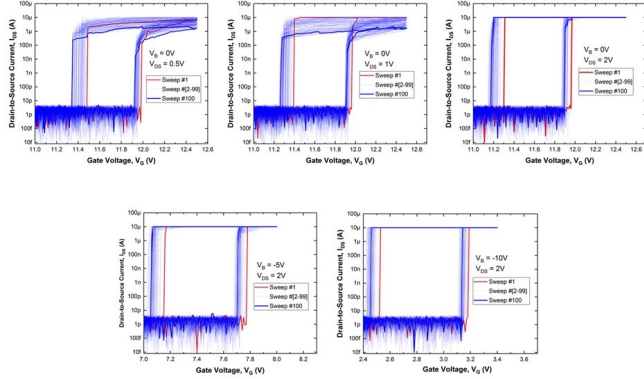


Fig. 2. 100 sweeps of I_{DS} vs. V_G used to track relay switching voltages under various operating conditions.

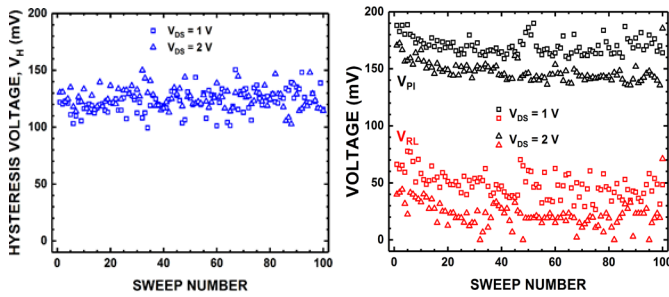


Fig. 3. (a) in relay switching voltages over 100 sweeps, for different values of V_{DS} . (b) Variation in hysteresis voltage over 100 sweeps, for different values of V_{DS} .

Noting the consistency of switching in Fig 2. As well as the steep sub-threshold swing of these device matches well with the goal of furthering reduction of power in computations. An important aspect of these devices is that the hysteresis voltage between V_{PI} and V_{RL} is mostly constant despite the decrease in V_{PI} overtime, which is largely attributed to the effect of dielectric charging in the Aluminum Oxide layer that forms on the surface of the Tungsten contactants.

V. CONCLUSION

Process variations (e.g., in the thicknesses of various deposited thin films) during relay fabrication result in variation in switching voltages from device to device. For a given relay, the switching voltages and hysteresis voltage were found to be very stable, assuring proper operation with sub-200mV gate voltage swing. This being verified further justifies the statement that NEM relays show promise for future ultra-low-power digital computation. As a disclaimer to this study, Actuation of devices in this study does not cover span of long performance periods, or rest; this aspect would be considered for further work on the theme of optimization of NEM relays for eventual application in competition with traditional transistors.

ACKNOWLEDGMENTS

M. Roots gratefully acknowledges the support of the UC-Berkeley HBCU REU program, Center for Energy Efficient Electronics Science (E³S), and the University of California at Berkeley, as well as Benjamin Osoba for mentorship, and Dr. Tsu-Jae King Liu and other members of her research group. As well as the efforts of Dr. Kedrick Perry, Mr. Perez Lowrey, Dr. Michelle Claville, Mr. Brandon Parker, Dr. Paul Gueye, and Dr. Bivas Saha.

This work was funded by the University of California: Office of the President, along with, the National Science Foundation [NSF Award 0939514]



REFERENCES

- [1] B. Calhoun et al., "Modeling and sizing for minimum energy operation in subthreshold circuits," *IEEE J. Solid State Circuits*, Vol. 40, pp. 1778-1786, 2005.
- [2] C. Qian et al., "Energy-delay performance optimization of NEM logic relay," *2015 IEEE International Electron Devices Meeting*, paper 18.1.
- [3] C. Qian et al., "Effect of body-biasing on the energy-delay performance of logic relays," *IEEE Electron Device Letters*, vol. 36, pp. 862-864, 2015.
- [4] F. Niroui et al., "Tunneling nanoelectromechanical switches based on compressible molecular thin-films," *ACS Nano*, vol. 9, no. 8, pp. 7886-7894, 2015.
- [5] F. Chen et al., "Integrated circuit design with NEM relays," *2008 IEEE/ACM Int'l Conf. Computer-Aided Design*, pp. 750-757, 2008.
- [6] A. Peschot et al., "Nanoelectromechanical switches for low-power digital computing," *Micromachines*, vol. 6, no. 8, pp. 1046-1065, 2015.
- [7] C. Pawashe et al., "Scaling limits of electrostatic nanorelays," *IEEE Trans. Elec. Dev.*, vol. 60, pp. 2936-2942, 2013.
- [8] R. Nathanael et al., "Multi-input/multi-output relay design for more compact and versatile implementation of digital logic with zero leakage," *Proceedings of Technical Program of 2012 VLSI Technology, System and Application*.
- [9] Y. Chen et al., "Reliability of MEM relays for zero leakage logic," *Proc. SPIE 8614, Reliability, Packaging, Testing, and Characterization of MOEMS/MEMS and Nanodevices XII*, p. 861404, 2013.
- [10] F. Niroui et al., "Nanoelectromechanical tunneling switches based on self-assembled molecular layers," *2014 IEEE 27th International Conference on Micro Electro Mechanical Systems*, pp. 1103-1106.
- [11] F. Niroui et al., "Tunneling nanoelectromechanical switches based on compressible molecular thin-films," *ACS Nano*, vol. 9, no. 8, pp. 7886-7894, 2015.
- [12] F. W. DelRio et al., "Elastic and adhesive properties of alkanethiol selfassembled monolayers on gold," *Appl. Phys. Lett.*, vol. 94, p. 131909, 2009.

