

Hardware Emulation of Boltzmann Machine Gibbs Sampling Algorithm

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Abstract

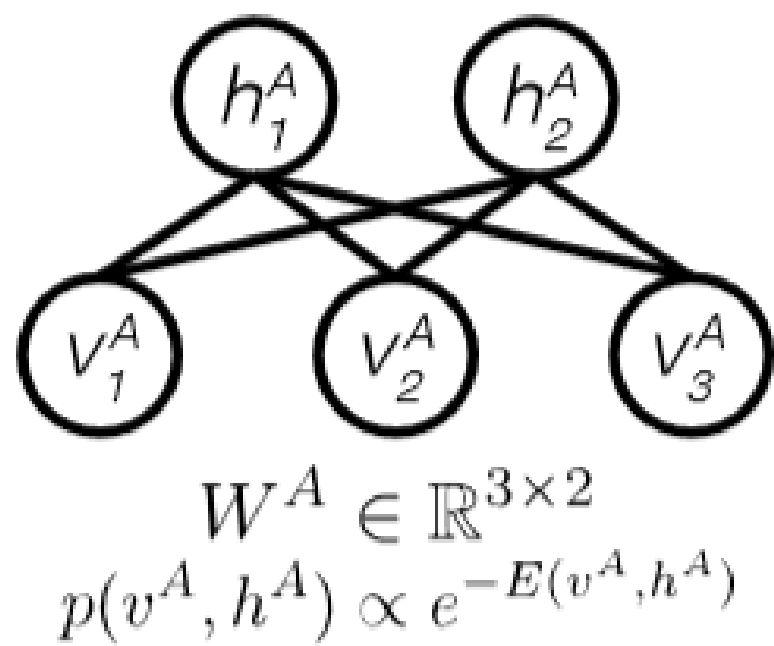
In order to arrive at a solution for NP-Hard combinatorial optimization problems, we have turned towards a dedicated hardware model. We utilized a machine learning-based algorithm that is governed by the stochastic formulations of the Restricted Boltzmann Machine (RBM), a type of neural network and probabilistic model. We then developed a circuit that imitates the RBM's Gibbs Sampling algorithm in the form of a single RBM neuron. This circuit outputs digital voltages in order to communicate results. This circuit board is a large-scale model of how an integrated circuit (IC), or a chip functions within modern technological devices. By constructing this circuit, we demonstrate that the hardware model can not only emulate the algorithm's behavior but also that of an integrated circuit.

Motivation

- Prove that this circuit model is viable for future large-scale chip implementation.

Background

RBM Architecture



Restricted Boltzmann Machine (RBM)

- Neural Network
- Probabilistic Model
- Assigns probability to output based on input

RBM

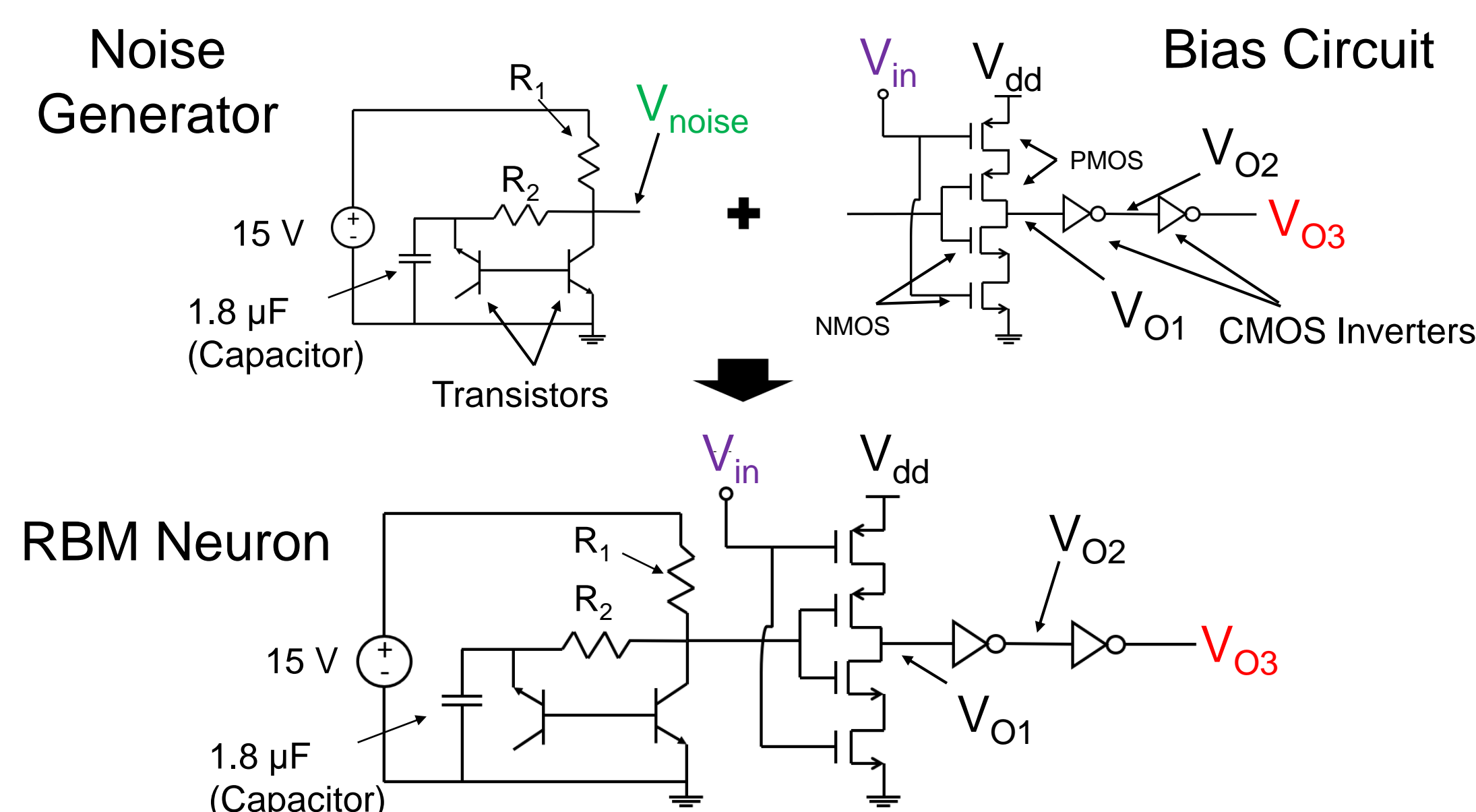
Probability Function
 $P(v_j = 1) = \sigma(\sum w_{ij} h_i + b_j)$
 Sigmoid Function V_{in}

Hardware

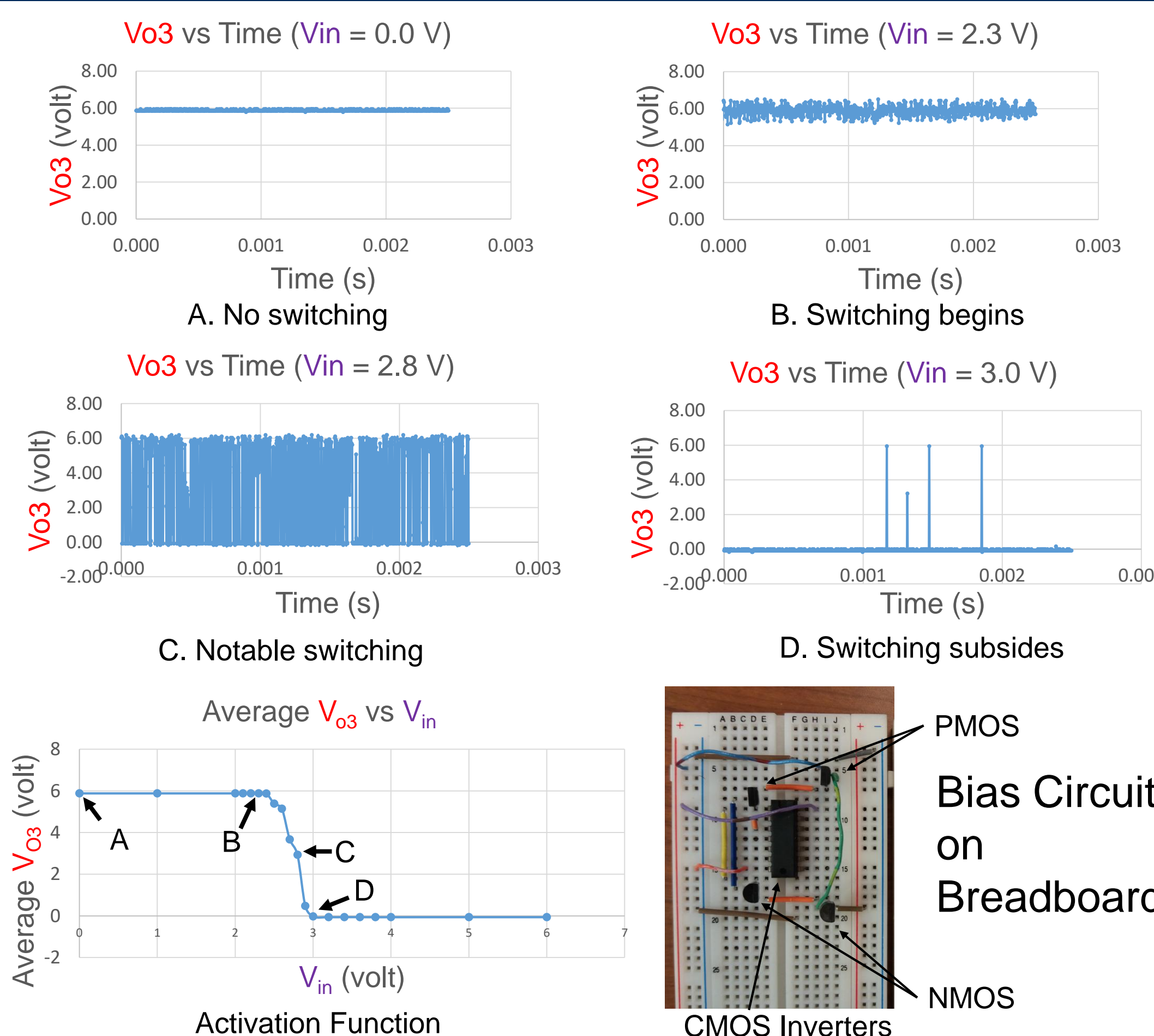
$P(v_j = 1) = \sigma(V_{in})$
 Noise Generator Bias Circuit

Methods

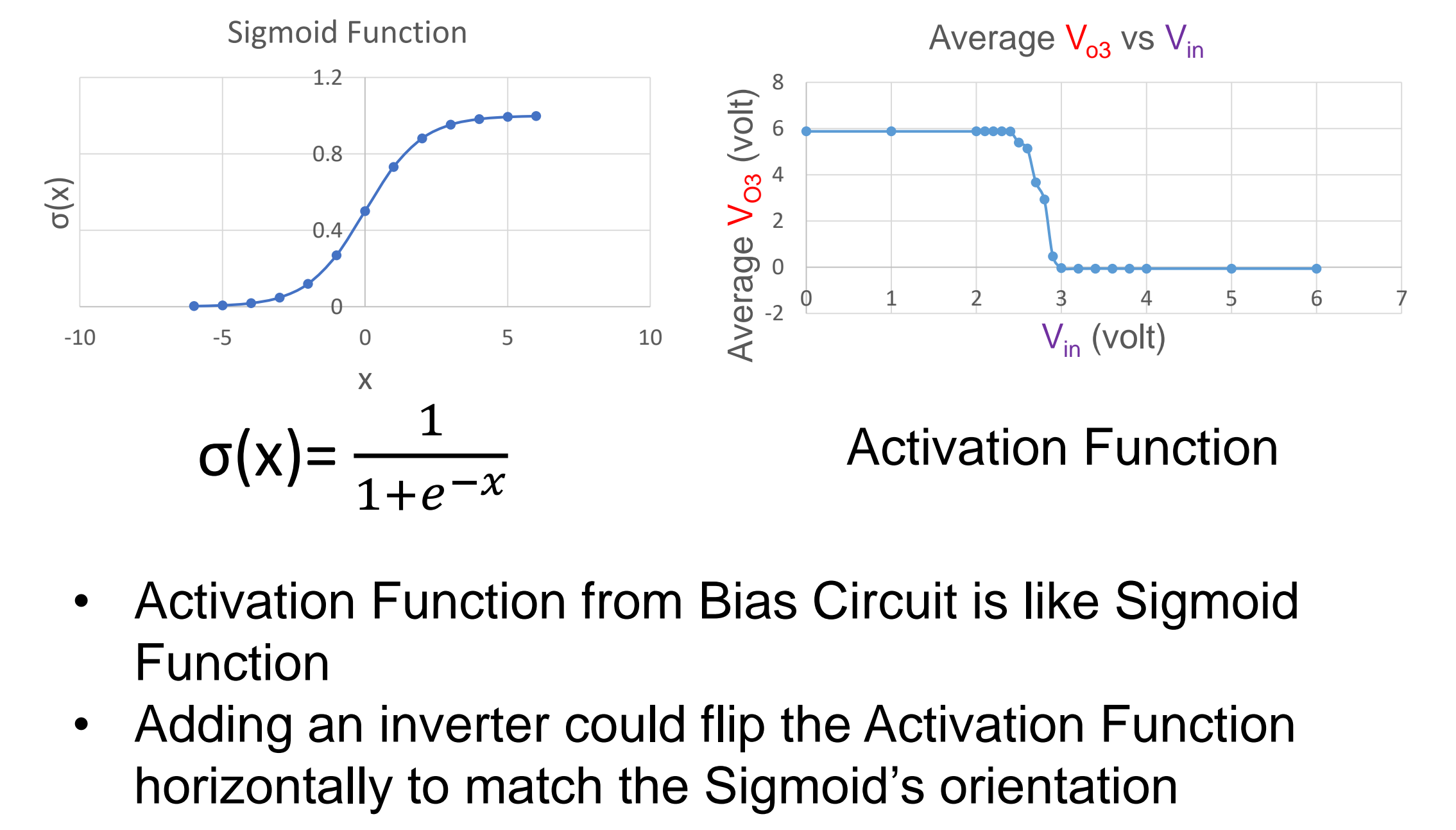
Objective: Create an RBM Neuron



Bias Circuit



Comparison



Conclusion

- Bias Circuit behavior is comparable to that of the Sigmoid Function
- Model can serve as a viable option for chip implementation in the future

References

[1] Hsin Chen, P. C. D. Fleury and A. F. Murray, "Continuous-valued probabilistic behavior in a VLSI generative model," in IEEE Transactions on Neural Networks, vol. 17, no. 3, pp. 755-770, May 2006. doi: 10.1109/TNN.2006.873278
 [2] S. Patel et al., "Hardware-aware, Scalable, Combinatorial Optimization on a Boltzmann Machine," unpublished.

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