Excess Off-State Current in InGaAs FinFETs

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***Abstract*— We present a detailed study of the off-state leakage current in scaled self-aligned InGaAs FinFETs. In long-channel devices, band-to-band tunneling at the drain-end of the channel is shown to be the root cause of excessive off-state current. This conclusion emerges from its characteristic electric field and temperature behavior and the absence of gate length and fin width dependencies. In short-channel devices, off-state current is significantly larger and it increases as the gate length shortens or the fin widens. We attribute this behavior to current multiplication through the gain of a floating-base parasitic bipolar transistor that is present inside the MOSFET. We extract the bipolar current gain which in short-channel devices is found to increase as the gate length shortens and decrease as the fin width narrows. In long channel devices, the current gain drops exponentially due to base recombination. This has allowed us to extract the diffusion length of electrons in the body of the transistor.**

***Index Terms*— III-V, FinFETs, self-aligned, tunneling, parasitic bipolar effect, GIDL.**

I. Introduction

InGaAs is a promising channel material candidate for CMOS technologies beyond the 7 nm node [1], [2]. In this dimensional range, only high aspect-ratio 3D transistors with a fin or nanowire configuration can deliver the necessary performance. Impressive InGaAs FinFET prototypes have recently been demonstrated [3]–[9]. Nevertheless, there are a number of serious concerns with this device technology. A pressing one is excessive off-state current that is believed to be a result of the narrow bandgap of the channel [10].

Recently, excessive off-state leakage current in self-aligned planar quantum-well InGaAs MOSFETs has been observed and studied [10]–[13]. Its origin has been attributed to band-to-band tunneling (BTBT) at the drain-end of the channel that is amplified by a parasitic bipolar transistor formed by the source, drain and floating body of the MOSFET. A similar effect ought to occur in InGaAs FinFETs and nanowire MOSFETs. Indeed, observations of poor turn-off in 3D III-V transistors have been reported [14] but a detailed experimental study is yet to be performed.

Manuscript received January 12, 2018; revised February 8, 2018; accepted February 12, 2018. Date of publication February 15, 2018; date of current version March 22, 2018. This work was supported in part by DTRA under Grant HDTRA1-14-1-0057, in part by the NSF Center for Energy Efficient Electronics Science E3S STC under Grant 0959514, and in part by Lam Research. The review of this letter was arranged by Editor S. J. Koester. *(Corresponding author: Xin Zhao.)*

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Digital Object Identifier 10.1109/LED.2018.2806559

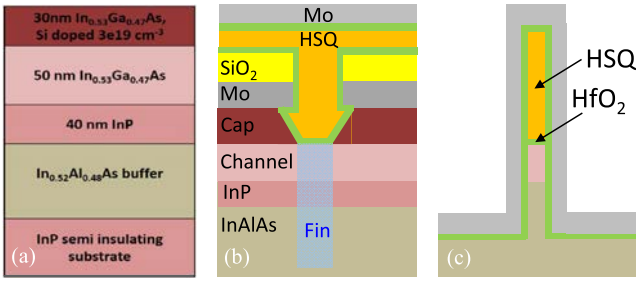


Fig. 1. (a) Starting heterostructure, (b) cross-sectional schematic along the fin length, and (c) perpendicular to the fin length in a finished device. In (b), the blue region indicates the location of the fin.

In this work, we study the turn-off behavior of tight-pitch self-aligned InGaAs FinFETs [9] with fin width (W_f) of 13 - 25 nm. Classic field and temperature (T) dependences establish BTBT as the origin of the off-state current in long-channel devices. The absence of a clear fin-width dependence suggests that tunneling mainly takes place in the extrinsic drain. Off-state current amplification through the parasitic bipolar transistor is evident in its gate-length and fin width dependence in short-channel devices.

II. Devices Under Investigation

Fig. 1 (a) shows the starting heterostructure that includes a 50 nm thick undoped InGaAs layer as channel and a 30 nm thick heavily-doped Si:InGaAs as cap. All layers are lattice matched to the InP substrate. Device fabrication followed a contact first, gate last process [9] and featured self-aligned ohmic contacts. Beneath the channel, a buffer layer consisting of 40 nm undoped InP and 400 nm undoped InAlAs was grown and no intentional contact was made to the body. A combination of dry etch and digital etch [15] was used to define high aspect ratio fins with smooth and vertical sidewalls. A dry cap recess process based on Cl_2/BCl_3 reactive ion etching and digital etch (DE) resulted in 5 nm separation between the edge of the cap and the fin (Fig. 1 (b)), critical to obtaining low access resistance and high performance. 3 nm HfO_2 as gate dielectric was deposited via ALD, corresponding to roughly 0.8 nm EOT. The HSQ mask that is used to define the fins is left in place making these double-gate FinFETs.

FinFETs with fin width W_f = 13–25 nm and gate length L_g = 60 nm - 16 μm were evaluated. The electrical characteristics of a typical fin array device with Nf = 34 fins, Wf = 13 nm and Lg = 50 nm are shown in Fig. 2. The output characteristics exhibit excellent current saturation. A peak transconductance ($g_{m,pk}$) of 752 μS/μm is obtained at V_{ds} = 0.5 V (all metrics normalized by the conducting gate periphery

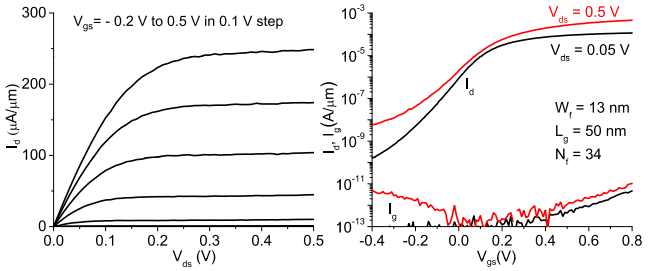


Fig. 2. Output and subthreshold characteristics of an InGaAs FinFET with $W_f = 13$ nm, $L_g = 50$ nm, and $N_f = 34$.

which is twice the channel thickness or 100 nm). A minimum subthreshold swing at $V_{ds} = 0.05$ V (S_{lin}) of 80 mV/dec is obtained. In the bias range of interest, the gate current is at least 1.5 orders of magnitude lower than the drain/source current. Compared to $V_{ds} = 0.05$ V, significant degradation of the subthreshold swing is observed at $V_{ds} = 0.5$ V with an undesirably high off-state current. Understanding the origin of this excess current is the goal of this work.

III. Band-to-Band Tunneling

The subthreshold characteristics of a device with $L_g = 620$ nm, $W_f = 17$ nm and $N_f = 34$ are shown in Fig. 3 (a) for different values of V_{ds}. The source current (in absolute value) is plotted to minimize contamination of the channel current by gate leakage. As V_{gs} swings negative, $|I_s|$ first decreases and then increases. The excess off-state current increases with drain bias. This is the characteristic shape of a tunneling current [14], [16].

To confirm this and gain further insight, we turn to the standard model of BTBT current [17]–[19]:

$$\frac{|I_{BTBT}|}{V_{dg}} \propto \exp(-A\frac{E_g^{1.5}}{V_{dg}}) \quad (1)$$

where V_{dg} is the bias between the drain and gate terminals, E_g is the semiconductor bandgap, and A is a material dependent constant. It is worth noting that, instead of V_{dg}, $V_{dg} - E_g/q$ was used in [17] and [18] where the body of the transistor is p-type doped. Here, the E_g/q term is dropped because the fin is undoped and the electric field around $V_{dg} = 0$ V is small. To verify the V_{dg} dependence in (1), the data of Fig. 3 (a) is replotted in Fig. 3 (b) as $|I_s|/V_{dg}$ in a semilog scale vs. $1/V_{dg}$. The overlapping curves for different V_{ds} in the off state reveal an exponential dependence on $1/V_{dg}$ that is consistent with (1).

To further test the BTBT origin of the excess off-state current, we performed measurements at different temperatures from 180 to 420 K for $V_{ds} = 0.8$ V, as shown in Fig. 3 (c). According to Eq. (1), the dominant temperature dependence is expected to come from the bandgap through $E_g^{1.5}$ term in the exponential factor [19]. Fig. 3 (d) shows $|I_s|$ at different temperatures for $V_{ds} = 0.8$ V and $V_{gs} = -0.9$ V as a function of $E_g^{1.5}$ where E_g of $In_{0.53}Ga_{0.47}As$ is obtained at the respective temperatures [20]. The exponential relationship that emerges, also obtained for other combinations of V_{gs} and V_{ds}, further confirms the BTBT origin of the excess current.

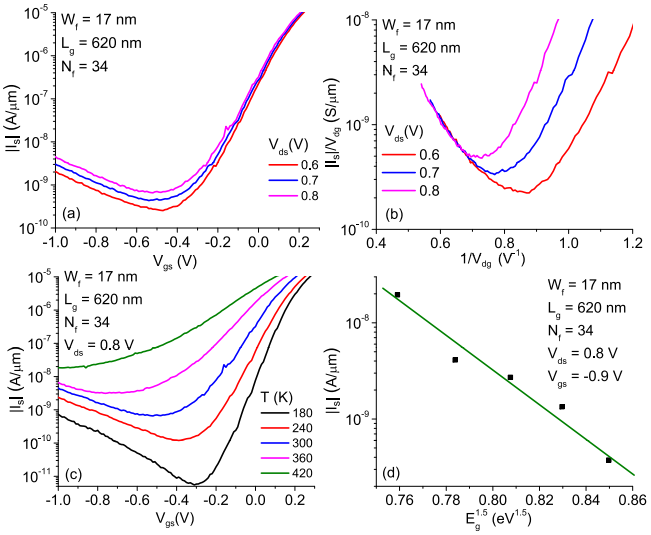


Fig. 3. (a) Subthreshold characteristics of a $W_f = 17$ nm, $L_g = 620$ nm $N_f = 34$ FinFET; (b) $|I_s|/V_{dg}$ in semilog scale vs. $1/V_{dg}$, revealing an exponential relationship; (c) Subthreshold characteristics of same device at $V_{ds} = 0.8$ V for T = 180 ~ 420 K; (d) $|I_s|$ shows linear dependence on $E_g^{1.5}$, confirming the tunneling nature of the current.

IV. Fin Width Dependence

We have studied the fin width dependence of the excess off-state current. Fig. 4 plots subthreshold characteristics for long- and short-channel devices with different W_f. In devices with $L_g = 5$ μm the off-state currents overlap for $V_{gs} < -0.6$ V regardless of W_f. This suggests that tunneling takes place in the extrinsic drain region (outside the fin). In contrast, devices with $L_g = 170$ nm show a much higher off-state current that scales with W_f. A pure BTBT mechanism that takes place in the high-field region on the drain side of the device should not have an L_g dependence [10]. This, plus the appearance of a W_f dependence in short-channel devices points at the role of a parasitic bipolar effect [10], [11], [21], [22]. This is treated in the next section.

V. Parasitic Bipolar Effect

The BTBT process generates electrons which flow out of the drain but it also generates holes that are collected in the fin body. In the absence of a body contact, the holes pile up and eventually reduce the source-channel barrier so that they can be injected into the source where they recombine. The source-channel barrier reduction also leads to electron injection from the source into the channel. This, in effect, amplifies the pure BTBT current through the current gain, β, of the parasitic bipolar transistor. As L_g is shortened, β increases, resulting in a larger off-state current.

To quantitatively investigate this bipolar effect in our FETs, the subthreshold characteristics of $W_f = 13$ nm devices with different L_g from 60 nm to 16 μm at $V_{ds} = 0.8$ V and T = 420 K are plotted in Fig. 5 (a). Here, an elevated temperature is used to mitigate contamination from gate current which becomes prominent at RT for long-channel devices. $V_{gt} = V_{gs} - V_t$ is used as the x-axis to correct V_t roll-off with L_g. V_t is extracted at constant $|I_s| \times L_g$ (10^{-6} A/μm $\times$ 1 μm) for

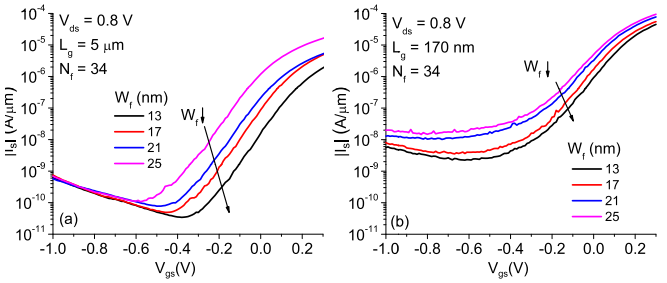


Fig. 4. Subthreshold characteristics of long $L_g = 5\ \mu$m (a) and short $L_g = 170$ nm devices (b) with different W_f.

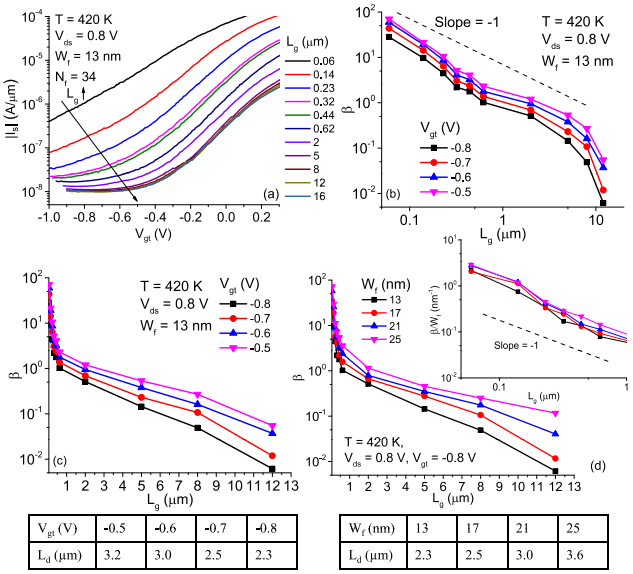
constant channel charge density. Fig. 5 (a) reveals a strong L_g dependence for $L_g < 5\ \mu$m.

β of the parasitic bipolar transistor can be quantitatively estimated by noting that in Fig. 5 (a), the off-state current is insensitive to L_g for $L_g \geq 8\ \mu$m. This suggests negligible bipolar amplification in this L_g regime. Following classical bipolar transistor physics, the ratio of the source current at a given L_g and that of $L_g = 16\ \mu$m at the same V_{gt} and V_{ds} should be equal to $\beta + 1$. This relies on the assumption that BTBT is independent of L_g all the way to the smallest dimensions. This assumption is justified from the observation in long-channel devices that BTBT takes place in the extrinsic drain region. The same observation allows us to neglect the impact of the bipolar effect on BTBT that was discussed in [14]. This is because the change in the channel potential induced by the bipolar effect is unlikely to affect the field distribution in the extrinsic drain region.

The extracted β is shown in Fig 5 (b). We indeed see a very prominent increase in β as L_g shrinks. Also, two different regimes are clearly noticeable. For $L_g < 1\ \mu$m, the data approach a linear dependence with a slope of -1. This is consistent with classic bipolar transistor physics. For $L_g > 1\ \mu$m, β drops rapidly as L_g increases. In fact, a plot of β vs. L_g in a semilog scale (Fig. 5 (c)) reveals that this dependence is exponential. This is to be expected since as the base width (L_g) becomes comparable or larger than the minority carrier diffusion length in the base (L_d), base recombination becomes dominant. From the slope of the β decay, we can extract the value of L_d, which, as given in the table below Fig. 5 (c), is of the order of 2-3 μm.

Figs. 5 (a) and (b) also reveal a V_{gt} dependence of β at all L_g: a higher (more positive) V_{gt} results in higher β up to V_{gt} of -0.5 V. As shown in [14], β might decrease for even higher (more positive) V_{gt} values. We cannot verify this because the background subthreshold current starts to increase for $V_{gt} > -0.5$ V masking the underlying BTBT current. The observed V_{gt} dependence is understandable since a more negative V_{gt} implies a higher energy barrier for electron injection into the channel [11]. For long L_g, we also see a reduction of L_d at lower V_{gt} (Fig. 5c). This is likely due to an increasing hole concentration in the base which enhances electron recombination.

Fig. 5 (d) shows β as a function of L_g for different W_f. For all L_g, β is reduced as W_f scales down. The physics are different in the two L_g regimes. For long L_g, a reduced



V_{gt} (V)	-0.5	-0.6	-0.7	-0.8
L_d (μm)	3.2	3.0	2.5	2.3

W_f (nm)	13	17	21	25
L_d (μm)	2.3	2.5	3.0	3.6

Fig. 5. (a) Subthreshold characteristics of $W_f = 13$ nm, $N_f = 34$ FinFETs with various L_g, showing saturating excess off-state current for $L_g > 5\ \mu$m, (b) Bipolar gain as a function of L_g for the device in Fig. 5 (a) at different V_{gt} in log-log scale; (c) Same data in semilog scale, and extracted electron diffusion length (L_d) in the base; (d) β (semilog scale) and β/W_f (inset, log-log scale) vs. L_g for devices with different W_f under identical conditions, and extracted L_d values.

L_d is observed in thinner fins. This suggests fin sidewall recombination as the dominant recombination mechanism. In our devices, defects on the fin sidewall, including semiconductor/oxide interface states [23], most likely become efficient recombination centers. For short L_g ($<1\ \mu$m), the inset demonstrates that β/W_f is independent of W_f. This indicates that β scales linearly with W_f. This is expected when recombination at the extrinsic source outside the fin is dominant and therefore W_f independent, while the channel current scales with W_f. As a result of this geometrical scaling factor, β in our FinFETs is much smaller than in planar QW-FET (at RT) [10], [11]. In this regard, the FinFET is intrinsically superior to the planar design as it comes to low-leakage operation.

To compete with Si technology where leakage can be lower than 10^{-10} A/μm for FinFETs with $L_g < 20$ nm at $V_{ds} = 0.8$ V [24], both BTBT and the bipolar effect need to be suppressed. Heterostructure engineering, including insertion of wide bandgap material at the drain [12] has been shown to reduce tunneling effectively. To alleviate bipolar amplification, providing a conductive path through the substrate to extract the holes [14], e.g. using bulk InGaAs FinFETs, is worth exploring.

VI. Conclusions

Extensive characterization of the off-state leakage current in state-of-the-art InGaAs FinFETs reveals a BTBT process that takes place in the extrinsic drain at its origin. In short-channel transistors, the BTBT current is amplified by a parasitic bipolar effect associated with the floating fin body. The bipolar current gain prominently increases as L_g shrinks. However, it decreases as W_f narrows. In this regard, scaled FinFETs have an inherent advantage over planar MOSFETs.

REFERENCES

[1] J. A. del Alamo, "Nanometer-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.

[2] J. A. del Alamo, D. A. Antoniadis, J. Lin, W. Lu, A. Vardi, and X. Zhao, "Nanometer-scale III–V MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 4, no. 5, pp. 205–214, Jul. 2016, doi: 10.1109/JEDS.2016.2571666.

[3] M. Radosavljevic, G. Dewey, D. Basu, J. Boardman, B. Chu-Kung, J. M. Fastenau, S. Kabehie, J. Kavalieros, V. Le, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, H. W. Then, and R. Chau, "Electrostatics improvement in 3-D tri-gate over ultra-thin body planar InGaAs quantum well field effect transistors with high-*K* gate dielectric and scaled gate-to-drain/gate-to-source separation," in *IEDM Tech. Dig.*, Dec. 2011, pp. 765–768, doi: 10.1109/IEDM.2011.6131661.

[4] T.-W. Kim, D. H. Kim, D. H. Koh, H. M. Kwon, R. H. Baek, D. Veksler, C. Huffman, K. Matthews, S. Oktyabrsky, A. Greene, Y. Ohsawa, A. Ko, H. Nakajima, M. Takahashi, T. Nishizuka, H. Ohtake, S. K. Banerjee, S. H. Shin, D.-H. Ko, C. Kang, D. Gilmer, R. J. W. Hill, W. Maszara, C. Hobbs, and P. D. Kirsch, "Sub-100 nm InGaAs quantum-well (QW) tri-gate MOSFETs with Al2O3/HfO2 (EOT <1 nm) for low-power applications," in *IEDM Tech. Dig.*, Dec. 2013, pp. 425–428, doi: 10.1109/IEDM.2013.6724641.

[5] S.-H. Kim, M. Yokoyama, R. Nakane, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, "High performance tri-gate extremely thin-body InAs-on-insulator MOSFETs with high short channel effect immunity and V_th tunability," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1354–1360, May 2014, doi: 10.1109/TED.2014.2312546.

[6] N. Waldron, C. Merckling, W. Guo, P. Ong, L. Teugels, S. Ansar, D. Tsvetanova, F. Sebaai, D. H. van Dorp, A. Milenin, D. Lin, L. Nyns, J. Mitard, A. Pourghaderi, B. Douhard, O. Richard, H. Bender, G. Boccardi, M. Caymax, M. Heyns, W. Vandervorst, K. Barla, N. Collaert, and A. V.-Y. Thean, "An InGaAs/InP quantum well FinFET using the replacement fin process integrated in an RMG flow on 300 mm Si substrates," in *VLSI Tech. Dig.*, Jun. 2014, pp. 1–2, doi: 10.1109/VLSIT.2014.6894349.

[7] R. Oxland, X. Li, S. W. Chang, S. W. Wang, T. Vasen, P. Ramvall, R. Contreras-Guerrero, J. Rojas-Ramirez, M. Holland, G. Doornbos, Y. S. Chang, D. S. Macintyre, S. Thoms, R. Droopad, Y.-C. Yeo, C. H. Diaz, I. G. Thayne, and M. Passlack, "InAs FinFETs with $H_{fin} = 20$ nm fabricated using a top–down etch process," *IEEE Electron Device Lett.*, vol. 37, no. 3, pp. 261–264, Mar. 2016, doi: 10.1109/LED.2016.2521001.

[8] A. Vardi and J. A. del Alamo, "Sub-10-nm fin-width self-aligned InGaAs FinFETs," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1104–1107, Sep. 2016, doi: 10.1109/LED.2016.2596764.

[9] A. Vardi, L. Kong, W. Lu, X. Cai, X. Zhao, J. Grajal, and J. A. del Alamo, "Self-aligned InGaAs FinFETs with 5-nm fin-width and 5-nm gate-contact separation," in *IEDM Tech. Dig.*, Dec. 2017, pp. 17.6.1–17.6.4.

[10] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Off-state leakage induced by band-to-band tunneling and floating-body bipolar effect in InGaAs quantum-well MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1203–1205, Dec. 2014, doi: 10.1109/LED.2014.2361528.

[11] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Physics and mitigation of excess OFF-state current in InGaAs quantum-well MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1448–1455, May 2015, doi: 10.1109/TED.2015.2410292.

[12] S. Lee, C.-Y. Huang, D. C.-Elias, J. J. M. Law, V. Chobpattanna, S. Krämer, B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, "High performance raised source/drain InAs/$In_{0.53}Ga_{0.47}As$ channel metal-oxide-semiconductor field-effect-transistors with reduced leakage using a vertical spacer," *Appl. Phys. Lett.*, vol. 103, no. 23, p. 233503, 2013, doi: 10.1063/1.4838660.

[13] J. Mo, E. Lind, G. Roll, and L.-E. Wernersson, "Reduction of off-state drain leakage in InGaAs-based metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 105, p. 033516, Jul. 2014, doi: 10.1063/1.4891569.

[14] B. Obradovic, T. Rakshit, W.-E. Wang, D. Lin, N. Waldron, N. Collaert, and M. S. Rodder. (May 2017). "Parasitic bipolar leakage in III-V FETs: Impact of substrate architecture." [Online]. Available: https://arxiv.org/abs/1705.06731

[15] X. Zhao and J. A. del Alamo, "Nanometer-scale vertical-sidewall reactive ion etching of InGaAs for 3-D III-V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 521–523, May 2014, doi: 10.1109/LED.2014.2313332.

[16] V. A. Tiwari, D. Jaeger, A. Scholze, and D. R. Nair, "Analysis of gate-induced drain leakage mechanisms in silicon-germanium channel pFET," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1270–1277, May 2014, doi: 10.1109/TED.2014.2312883.

[17] J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, "Subbreakdown drain leakage current in MOSFET," *IEEE Electron Device Lett.*, vol. 8, no. 11, pp. 515–517, Nov. 1987, doi: 10.1109/EDL.1987.26713.

[18] J. A. del Alamo, *Integrated Microelectronic Devices*, 1st ed. New York, NY, USA: Pearson, 2017, pp. 661–664.

[19] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York, NY, USA: Wiley, 1981, pp. 522–525.

[20] S. Paul, J. B. Roy, and P. K. Basu, "Empirical expressions for the alloy composition and temperature dependence of the band gap and intrinsic carrier density in $Ga_xIn_{1-x}As$," *J. Appl. Phys.*, vol. 69, no. 2, pp. 827–829, Jan. 1991, doi: 10.1063/1.348919.

[21] J. Chen, F. Assaderaghi, P.-K. Ko, and C. Hu, "The enhancement of gate-induced-drain-leakage (GIDL) current in short-channel SOI MOSFET and its application in measuring lateral bipolar current gain beta," *IEEE Electron Device Lett.*, vol. 13, no. 11, pp. 572–574, Nov. 1992, doi: 10.1109/55.192844.

[22] J.-Y. Choi and J. G. Fossum, "Analysis and control of floating-body bipolar effects in fully depleted submicrometer SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1384–1391, Jun. 1991, doi: 10.1109/16.81630.

[23] A. Higuera-Rodriguez, B. Romeira, S. Birindelli, L. E. Black, E. Smalbrugge, P. J. van Veldhoven, W. M. M. Kessels, M. K. Smit, and A. Fiore, "Ultralow surface recombination velocity in passivated InGaAs/InP nanopillars," *Nano Lett.*, vol. 17, no. 4, pp. 2627–2633, Mar. 2017, doi: 10.1021/acs.nanolett.7b00430.

[24] C. Auth, A. Aliyarukunju, M. Asoro, D. Bergstrom, V. Bhagwat, J. Birdsall, N. Bisnik, M. Buehler, V. Chikarmane, G. Ding, Q. Fu, H. Gomez, W. Han, D. Hanken, M. Haran, M. Hattendorf, R. Heussner, H. Hiramatsu, B. Ho, S. Jaloviar, I. Jin, S. Joshi, S. Kirby, S. Kosaraju, H. Kothari, G. Leatherman, K. Lee, J. Leib, A. Madhavan, K. Marla, H. Meyer, T. Mule, C. Parker, S. Parthasarathy, C. Pelto, L. Pipes, I. Post, M. Prince, A. Rahman, S. Rajamani, A. Saha, J. D. Santos, M. Sharma, V. Sharma, J. Shin, P. Sinha, P. Smith, M. Sprinkle, A. S. Amour, C. Staus, R. Suri, D. Towner, A. Tripathi, A. Tura, C. Ward, and A. Yeoh, "A 10 nm high performance and low-power CMOS technology featuring 3_{rd} generation FinFET transistors, self-aligned quad patterning, contact over active gate and cobalt local interconnects," in *IEDM Tech. Dig.*, Dec. 2017, pp. 29.1.1–29.1.4.