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Nanometer-Scale III-V MOSFETs

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ABSTRACT After 50 years of Moore's Law, Si CMOS, the mainstream logic technology, is on a course of diminishing returns. The use of new semiconductor channel materials with improved transport properties over Si offer the potential for device scaling to nanometer dimensions and continued progress. Among new channel materials, III-V compound semiconductors are particularly promising. InGaAs is currently the most attractive candidate for future III-V based n-type MOSFETs while InGaSb is of great interest for p-channel MOSFETs. At the point of most likely deployment, devices based on these semiconductors will have a highly three-dimensional architecture. This paper reviews recent progress toward the development of nanoscale III-V MOSFETs based on InGaAs and InGaSb with emphasis on scalable technologies and device architectures and relevant physics. Progress in recent times has been brisk but much work remains to be done before III-V CMOS can become a reality.

INDEX TERMS III-V compound semiconductors, CMOS, InGaAs, InGaSb.

I. INTRODUCTION

Si CMOS has been the engine that has powered the microelectronics revolution for the major part of the last 50 years. MOSFET scaling and its "triple dividends" of cost reduction, enhanced performance and greater energy efficiency, has made this possible. This extraordinary feat of human innovation is facing unprecedented challenges. Several features of MOSFETs long held at the heart of its unique suitability for logic circuits had to be replaced in the last few years: the SiO_2 gate oxide has given way to "high-K" (high permittivity) dielectrics and the planar structure has been superseded by FinFETs. Perhaps the time has come to discard Si itself as the active channel material.

One of the central difficulties of Si MOSFETs is the increase in parasitic capacitance and resistance relative to their intrinsic counterparts as device dimensions decrease. At a time when voltage reduction is imperative in order to manage power dissipation, increased parasitics translate into performance, i.e., current drive, that has stagnated. A potential solution to this is to substitute the Si channel by a new material where carriers travel at higher velocity. All things being equal, this should yield higher current and improved performance.

It is in this regard that certain III-V compound semiconductors have a lot to offer [1]. InGaAs for electrons and InGaSb for holes offer a good balance among the many requirements imposed on a MOSFET channel material: high mobility, low contact resistance, sufficient interfacial quality with high-K dielectrics and adequate bandgap energy. In addition, the InGaAs heterostructure system is relatively mature with InGaAs High Electron Mobility Transistors (HEMT) and Heterojunction Bipolar Transistors (HBT) at the heart of many advanced communication systems as well as in low-cost mass-market applications such as cellular phones [2].

The last few years have witnessed an explosion of research on InGaAs-based n-channel MOSFETs in industry and academia. This has delivered rapid progress in planar device designs as well as 3D architectures such as FinFETs and nanowire FETs [3]–[5]. For alternative p-type MOSFETs, Ge channels look very promising but InGaSb has also advantageous properties that make it attractive [1]. Much less research has been devoted to this latter topic but

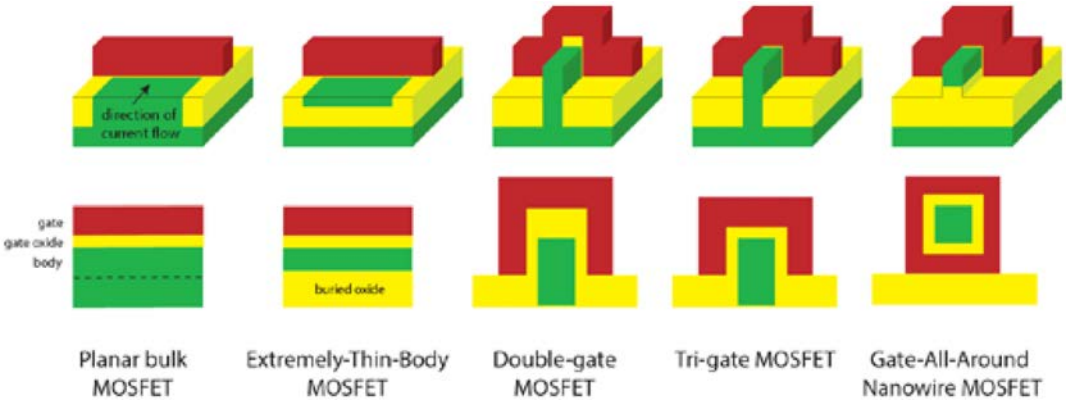

FIGURE 1. 3D schematic (top) and cross-sectional schematic (bottom) of MOSFET structures with increasing electrostatic gate control of the channel from left to right. In Planar bulk and Extremely-Thin-Body MOSFETs, channel charge is electrostatically controlled by gating from the device surface. In Double-gate MOSFETs, gate action takes places from two side surfaces of a fin-shaped channel. In Tri-gate MOSFETs, the gate wraps around three sides. The "Gate-All-Around" nanowire MOSFET, in its horizontal or vertical configuration, has a thin nanowire channel that is wrapped around its entire periphery by the gate.

recent results suggest InGaSb is a candidate worthy of close examination [6], [7].

This paper reviews recent progress towards the development of III-V n-channel and p-channel MOSFETs for future CMOS applications. The paper emphasizes recent developments on Si-compatible technologies and scalable transistor architectures as well as novel device physics of relevance to future logic CMOS. The paper is organized as follows. Section II deals with thin-body InGaAs planar device architectures. Section III concerns InGaAs FinFETs and Trigate FETs. Section IV reviews progress on InGaAs Nanowire MOSFETs. Finally, Section V summarizes recent research on InGaSb MOSFETs. For lack of space, the very important issues of III-V materials integration with Si wafer manufacturing is not discussed in this paper.

II. INGAAS PLANAR MOSFETS

Fig. 1 shows the evolution of MOSFET architecture in its quest for reduced footprint, enhanced transistor density and lower cost, the drivers of Moore's law. The challenge in transistor scaling is maximizing performance (i.e., drain current density) at reduced voltage while keeping short-channel effects in check. Footprint scaling demands shrinking all dimensions, including the gate length, in a harmonious way. Mitigating short-channel effects as gate length scales down, requires enhanced gate control of the channel. This has dictated looking beyond the planar bulk or thick SOI MOSFET to ultra-thin body MOSFET and eventually to so-called multi-gate structures such as the Double-Gate MOSFET, Trigate MOSFET (both referred to here as FinFETs) and the Gate-All-Around Nanowire MOSFET in a horizontal or vertical configuration. All these device structures have been demonstrated in the InGaAs system [3].

As the simplest possible structure, the planar InGaAs MOSFET has made great strides in recent times. The Quantum-Well (QW) MOSFET configuration, with a very thin quantum confined channel, has delivered the best results as it provides excellent electrostatic control from the top gate. As a measure of the progress that has recently been achieved, Fig. 2 shows the evolution of transconductance, g_m, of InGaAs MOSFETs (undoped body) and HEMTs as a function of year of demonstration. g_m is a critical figure of merit in just about any transistor application. While the first InGaAs MOSFETs were reported at about the same time as the first HEMTs appeared on the scene over 30 years ago, there has been a striking transconductance gap between the two types of devices that lasted for over 25 years. It is only recently that the InGaAs MOSFET has emerged as a viable transistor architecture. In fact, only this year the g_m of an InGaAs MOSFET has come to exceed that of the best InGaAs HEMT [8].

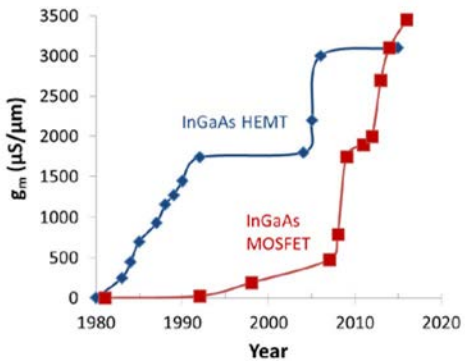

FIGURE 2. Transconductance comparison of InGaAs MOSFETs (undoped body) and HEMTs (with InAs composition between 0 and 1) *vs.* year of demonstration.

The dramatic emergence of InGaAs MOSFETs in the last few years would not have been possible without solving a long-standing problem in III-V MOS systems and that is Fermi level pinning at the oxide-semiconductor interface. Fermi level pinning is believed to be due to the formation of native oxides that create high concentration of defects at the semiconductor surface [9]. Fermi

level pinning prevents the modulation of the surface potential by the gate and the charge control that is essential for the operation of a MOSFET. A technological breakthrough has recently addressed this problem. This was the finding that the use of atomic layer deposition (ALD) to form the gate oxide involves a "self-cleaning effect" that eliminates the native oxides and associated defects at the semiconductor surface [10], [11]. Fast forward a few years and after several fundamental studies [12]–[14] and there are now many demonstrations of high-permittivity oxide/InGaAs interfaces with very high quality. Subthreshold swings in MOSFETs with values approaching 60 mV/dec have been demonstrated [15]–[17]. Interface state densities in the 10^{11} $eV^{-1}.cm^{-2}$ range have also been reported [18], [19].

Another key element that has greatly contributed to the dramatic recent improvement in InGaAs MOSFET performance has been the development of self-aligned device architectures. Self-alignment of gate and contacts is essential for manufacturability and to minimize parasitics and footprint. In essence, four different self-aligned designs have emerged in the last few years. A contact-first, gate last process in which the gate is nested in an opening created in the ohmic contacts has yielded excellent results [8], [16], [20]–[22]. The extensive use of Reactive Ion Etching (RIE) has afforded very tight contact-gate spacing and high performance. A schematic diagram of this device is shown in Fig. 3.

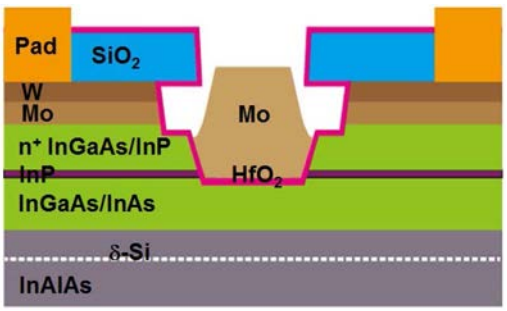

FIGURE 3. Cross-sectional schematic of a self-aligned InGaAs Quantum-Well MOSFET fabricated by a contact-first, gate-last process [21].

An alternative approach that has also delivered good results consists of raised, self-aligned source and drain epitaxial regions selectively grown around a gate or a dummy gate [23]–[25]. By virtue of the high doping that can be introduced in the source and drain contact regions, this design has yielded very small parasitic access resistance [24].

In yet another approach, a thin Ni layer is thermally reacted with InGaAs to give rise to a highly conducting and very shallow intermetallic compound with very low resistivity [26], [27]. The unreacted Ni can be selectively removed. This is exploited to fabricate self-aligned InGaAs MOSFETs in a process akin to that of silicided source and drain Si MOSFETs [28], [29]. The performance of such devices is lagging because of the relatively large contact resistance of the NiInGaAs/InGaAs system.

In a final approach, the combination of self-aligned ion implanted source and drain extensions and in-situ doped raised source and drain regions around a gate has also been used to fabricate self-aligned InGaAs MOSFETs with excellent characteristics [30].

In nanometer-scale transistors in which the space available for the ohmic contacts is very limited, achieving very low contact resistance is a critical issue. Fig. 4 compares different Si-compatible ohmic contact schemes to n^+-InGaAs in terms of the most important performance metrics: contact resistivity and metal film resistivity [31]. Both need to be small in order to minimize the contact resistance in actual transistor structures. The lowest contact resistivity has been obtained in the Pd-InGaAs system [32], however, its film resistivity is poor. On the other hand, refractory metals such as Mo and W have yielded excellent contact resistivity and also feature very low film resistivity [33]. Even with these materials, at the dimensions of interest, the best contact resistance that has been demonstrated is still too high by at least a factor of two [31]. A contact resistivity below 0.1 $\Omega.\mu m^2$ is required to accomplish the desired objective. This is a very challenging goal.

The path forward will require superior understanding and control of the metal-semiconductor interface. There is clear evidence that a contact-first approach protects the integrity of the interface and yields outstanding contacts [33], [34]. This highlights the promise of careful engineering of the metal/semiconductor interface. The Landauer limit for contacts to n^+-$In_{0.53}Ga_{0.47}As$ for practical doping levels is in the 0.1 $\Omega.\mu m^2$ range [35]. Higher doping levels should enable to reach below this value. In addition, the Schottky barrier height of metals on InGaAs can be engineered over a relatively wide range of values through the InAs composition at the surface [28].

Planar MOSFETs are limited in their scaling potential. This has become evident in a recent channel scaling study in which the gate length and channel thickness of self-aligned QW-MOSFETs was varied over a broad dimensional range [21]. Channel thickness was found to have a strong impact on device characteristics. A thick channel is beneficial to ON-state figures of merit, such as g_m, while a thin channel benefits OFF-state metrics, such as subthreshold swing, S, and drain-induced barrier lowering (DIBL). In fact, S and DIBL were found to follow classic scaling behavior. These observations are borne by other results in the literature. Fig. 5 shows linear S (low V_{ds}) vs. the ratio of the gate length to the electrostatic length for published InGaAs QW-MOSFETs. Many device demonstrations have been made that approach ideal electrostatic scaling behavior. The conclusion from this is that InGaAs QW MOSFETs are at the limit of scaling around $L_g = 50$ nm beyond which short-channel effects become too severe.

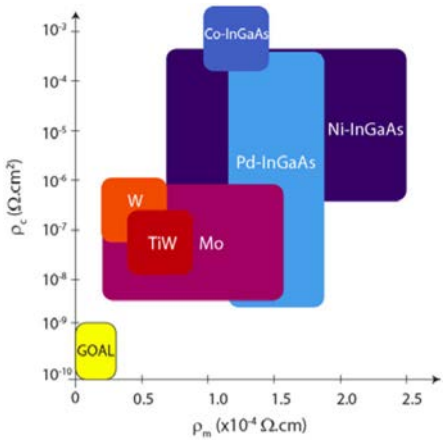

FIGURE 4. **Landscape of contact resistivity vs. metal film resistivity of Si-compatible ohmic contacts to n-InGaAs [31]. The desired regime of operation is the bottom left corner.**

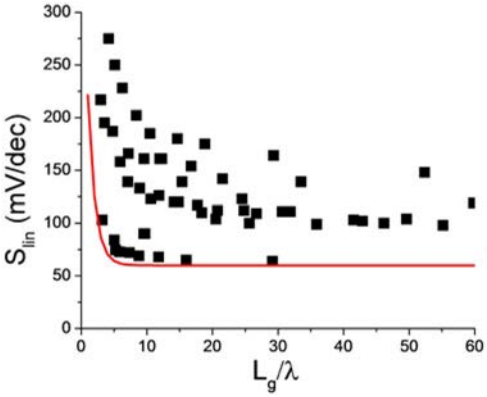

FIGURE 5. **Linear subthreshold swing vs. ratio of gate length to electrostatic scaling length of planar InGaAs Quantum-Well MOSFETs from the literature. The line indicates the expected theoretical behavior based on a simple model [21].**

Planar MOSFETs, though unable to meet the scaling goals, constitute an excellent platform for process development and device physics exploration. A recent example is the identification of the physics behind the excess off-state current that has been observed in tight-pitch InGaAs QW-MOSFETs and that prevents transistors from being effectively shut off [36], [37]. As Fig. 6 shows, the excess off-state current is strongly enhanced by V_{ds} and it also increases as the gate length scales down which makes this phenomenon highly problematic in nanoscale devices.

A detailed experimental and modeling study has revealed that the excess off-state current is due to band-to-band tunneling (BTBT) at the drain-end of the channel that is amplified by the parasitic lateral bipolar transistor formed by the channel (floating base), the source (emitter) and drain (collector) of the MOSFET [37]. With a base made out of InGaAs, the lateral bipolar transistor current gain can be very high, order $\sim 10^3$, so that even a small BTBT-generated current can result in sizable off-state leakage current. This deleterious phenomenon is a consequence of

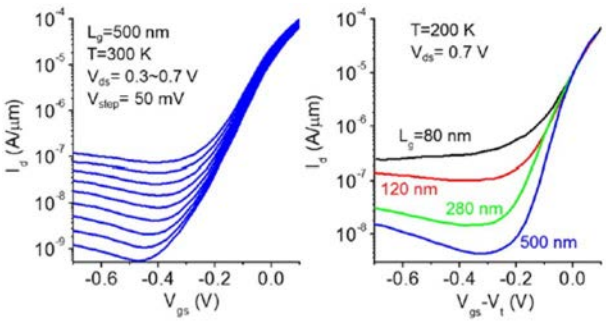

FIGURE 6. **Subthreshold characteristics of self-aligned InGaAs MOSFETs showing weak V_{gs} control of off-state current. Left: long-channel device as a function of V_{ds} at room temperature. Right: devices with different gate lengths at V_{ds} = 0.7 V and at 200 K [36], [37].**

the small bandgap of the InGaAs channel and from the fact that BTBT-generated holes cannot be easily extracted from the channel. As a consequence, this problem will affect all InGaAs transistor architectures unless a hole contact can be provided to the body of the transistor. Mitigating this problem is a key goal for future scaled devices.

III. INGAAS FINFETS

Improved MOSFET scalability over what planar devices can deliver requires 3D, or multigate, device designs. Double-gate or triple-gate (Trigate) InGaAs FinFETs (see Fig. 1) provide enhanced gate control over the channel yielding greater scaling potential. In commercial Si CMOS technology, FinFETs currently constitute the structure of choice for leading edge devices [38], [39].

InGaAs double-gate and Trigate FinFETs have been demonstrated by several groups [15], [40]–[45]. Top-down approaches based on RIE are common [15], [40], [41], [43]–[45], while bottom-up approaches using Aspect Ratio Trapping (ART) [46] have also been explored [42]. At the moment, InGaAs transistors fabricated by either of these techniques have demonstrated modest performance when compared with what is to be expected.

A summary of the state of the art for InGaAs FinFETs concerning carrier transport characteristics, can be seen in Fig. 7. This graph shows the peak transconductance demonstrated in InGaAs FinFETs to date as a function of fin width, W_f. For reference, estimations from selected state-of-the-art Si FinFETs have been included [38], [39]. In this figure, g_m has been normalized by the total conducting gate periphery (number of fins x ($2H_c+W_f$), where H_c is the channel height), as commonly done in FinFETs. The label next to each data point is the aspect ratio of the conducting channel in the fin (H_c/W_f). The figure highlights recent results from some of the present authors (red squares) [45].

Several observations can be made from Fig. 7. First, published InGaAs FinFETs prior to those in [45] are based on relatively wide fins with channel aspect ratios that are, at best, unity. With the exception of [45], no transistors have

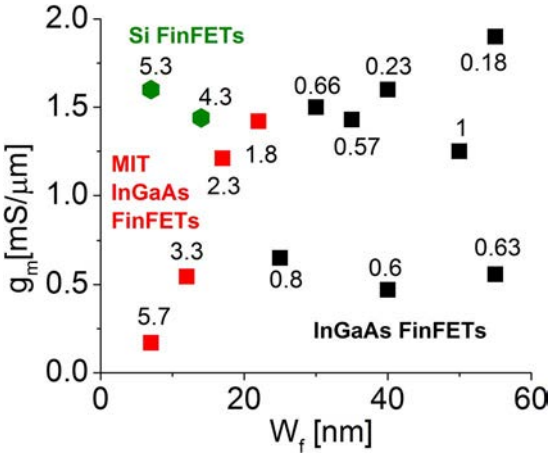

FIGURE 7. **Benchmark of transconductance normalized by conducting gate periphery for InGaAs and Si FinFETs (estimated) as a function of fin width. The number next to each symbol gives the aspect ratio of the channel. Recent results from some of the present authors are highlighted with red symbols [45].**

been reported with W_f<25 nm or channel aspect ratios greater than 1. This is in contrast with Si FinFETs where W_f<10 nm and channel aspect ratio in excess of 5 constitute the state of the art [39]. For future InGaAs FinFETs to realize the potential of this material system, far more aggressive fin designs are required [47].

The second observation to be made from the data of Fig. 7, though more subtle, is that InGaAs FinFETs are rather subpar when compared with Si FinFETs. The Si devices manage to extract a lot of g_m out of a tiny fin footprint, suggesting effective charge control from the sidewalls. In contrast, the InGaAs FinFETs have very large footprint and relatively short sidewalls and, nevertheless, they barely match the g_m of Si FinFETs. In fact, the InGaAs FinFETs in Fig. 7 are significantly worse than planar InGaAs MOSFETs where a peak g_m well in excess of 3 mS/μm has been demonstrated [8]. This is even though the experimental InGaAs FinFETs prototyped to date feature a relatively large contact area supplying current to comparatively narrow fins.

There are many reasons for this significant performance gap. In InGaAs FinFETs with etched fins, the majority of the data in Fig. 7, the quality of the sidewalls is a major concern. Sidewall roughness, relatively high interface state density on the sidewall MOS [48] and probably damaged sidewall stoichiometry [49] are undesirable byproducts of the etch process. In addition, in spite of the comparatively large contact area, access resistance in FinFETs tends to be significantly higher than in planar designs. This need not be the case, since Mo contacts on InGaAs fins have been demonstrated with contact resistance comparable to that of equivalent planar structures [50].

A key advantage of FinFETs is its enhanced scalability. As argued in the introduction, this stems from greater channel charge control. InGaAs FinFETs to date have indeed demonstrated excellent short-channel effects, as illustrated in Fig. 8. This figure shows linear subthreshold swing in experimental devices that approach the expected ideal scaling behavior [51]. It is this that makes the FinFET architecture a very promising one for deeply scaled devices.

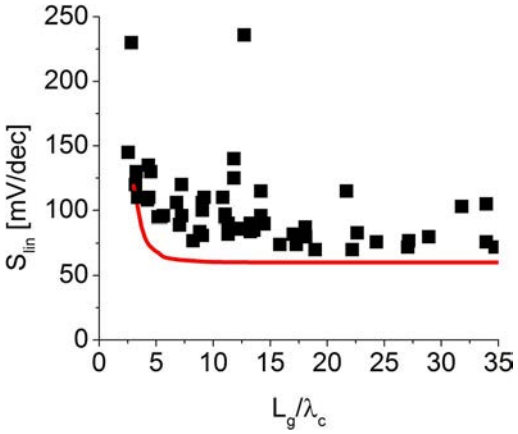

FIGURE 8. **Linear subthreshold swing (low V_{DS}) vs. ratio of gate length to electrostatic scaling length in experimental InGaAs FinFETs. For reference, the red line indicates ideal electrostatic behavior [51].**

An issue of concern in scaled InGaAs FinFETs is the strong dependence of electrical parameters on the fin width as a consequence of quantum confinement effects. This is expected to be much worse than in equivalent Si FinFETs due to the low effective mass of electrons in InGaAs [52]. Recent experiments have verified these predictions in doped-channel InGaAs FinFETs that were fabricated by a precision dry etching process [53]. For fins narrower than about 10 nm, a strong fin width dependence to the threshold voltage, V_T, was observed as shown in Fig. 9. The width sensitivity of V_T is about four times larger than in Si FinFETs with equivalent fin widths. Fig. 9 also shows a comparison of experimental with simulated V_T from Poisson-Schrodinger simulations of InGaAs FinFETs [53]. The agreement between model and simulations strongly supports the quantum origin of this phenomenon. This has important implications for the design and manufacturing of future InGaAs FinFETs.

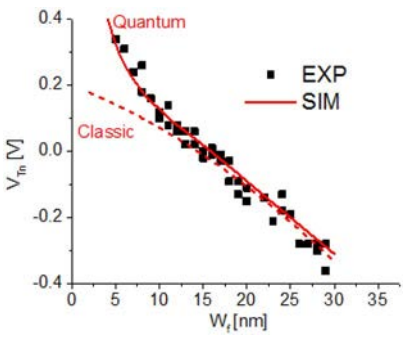

FIGURE 9. **Experimental vs. simulated threshold voltage of n-InGaAs FinFETs (double gate) vs. fin width. The quantum model gives the result of self-consistent Poisson-Schrodinger simulations (Nextnano). The classic model does not include quantum effects [53].**

IV. INGAAS NANOWIRE MOSFETS

The ultimate scalable MOSFET design is the nanowire architecture (Fig. 1). Nanowire MOSFETs come in two different geometries, horizontal and vertical. Both have been demonstrated in the InGaAs system.

Horizontal nanowire MOSFETs are essentially FinFETs in which the channel has been suspended through selective etching and a gate is wrapped around its entire periphery [19], [54]. This provides enhanced charge control and an ability to scale to smaller dimensions. Lateral InGaAs nanowires are more frequently prepared through etching, though lateral growth of GaAs and InAs nanowires has been demonstrated by the Vapor-Liquid-Solid technique [4]. Reviews of the state of the art in III-V Nanowire MOSFETs have recently been published [3], [4].

The *vertical* nanowire (VNW) MOSFET is a particularly attractive design because with a vertical current flow, footprint scaling and gate length scaling become uncoupled. This promises high transistor density, stemming from a very small footprint, yet acceptable short-channel effects due to the flexibility in L_g design [55]. In addition, there is also greater freedom in the selection of contact length as well as the length of the gate to ohmic contact spacer since neither contribute to the footprint. This should translate into lower contact resistance and parasitic capacitance and higher performance.

An intriguing aspect of VNW-MOSFETs is that they offer a plausible path for integration on a Si substrate. Bottom-up growth of InGaAs nanowires on Si substrates is relatively well established through Vapor-Liquid-Solid (VLS) epitaxy and selective-area epitaxy (SAE) on a templated substrate [3], [4]. Numerous VNW-MOSFET demonstrations have been published with NWs grown using either of these techniques [56]–[58].

Reactive Ion Etching, in combination with digital etch, has recently emerged as a technique capable of creating very high aspect ratio nanowires in the InGaAs system that feature smooth vertical walls and dimensions in the nanometer range [59], [60]. A particularly spectacular example is shown in Fig. 10. Digital etch allows the controlled trimming of nanowire diameter while preserving the aspect ratio of the structure and improving sidewall smoothness. InGaAs VNW-MOSFETs have been demonstrated by this technique with performance that matches that of transistors fabricated by bottom-up approaches [61]. The use of digital etch was shown to improve both the subthreshold characteristics as well as g_m presumably as a result of removing a thin damaged subsurface layer at the sidewalls.

While the ON-state characteristics are still below what is desirable (mostly due to difficulties with the top contact), OFF-state behavior of InGaAs VNW-MOSFETs is approaching ideal behavior. Fig. 11 shows the linear subthreshold swing of InGaAs VNW MOSFETs vs. the ratio of the gate length to the electrostatic characteristic length, λ_c. For reference, the ideal behavior is also indicated [62]. A number of device demonstrations already approach the theoretical expectations for this device architecture.

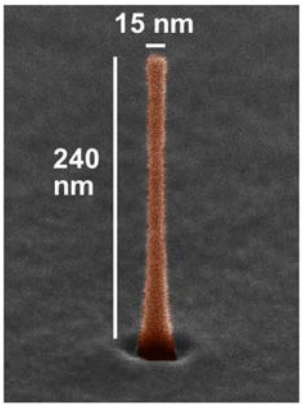

FIGURE 10. InGaAs nanowire fabricated by a combination of BCl/SiCl/Ar Reactive Ion Etching and digital etch [59].

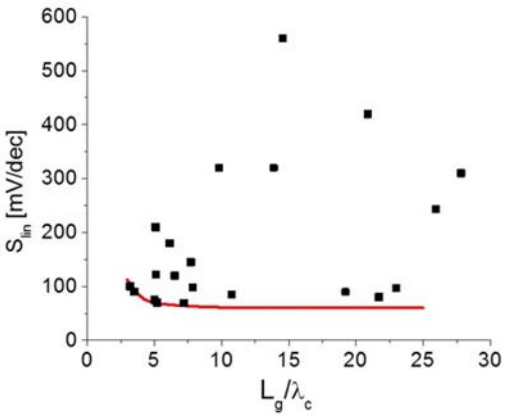

FIGURE 11. Linear subthreshold swing vs. ratio of gate length to electrostatic characteristic length of InGaAs VNW MOSFETs. For reference, the ideal electrostatic behavior is also indicated [62].

A challenge for InGaAs VNW-MOSFETs is scaling the nanowire diameter to the sub-10 nm regime. To date, the most aggressive VNW MOSFETs that have been demonstrated feature a 28 nm diameter [57], [58]. At a hypothetical point of insertion in the roadmap, nanowire diameters in the 7 nm range are needed [47]. At this scale, top contact resistance is a very significant problem. Additionally, nanowire survival during the fabrication process is a great concern.

V. INGASB P-TYPE MOSFETS

We now turn our attention to p-channel MOSFETs. Among all III-V semiconductors, the antimonide system, specifically $In_xGa_{1-x}Sb$ with $0<x<1$, has recently attracted considerable attention due to its high hole mobility and its strong enhancement through compressive stress [1], [63], [64]. Significant progress has been made in the last few years towards InGaSb p-channel MOSFETs [64]–[67]. Remarkable improvements in the transport characteristics have been reported when biaxial [68]–[70] or uniaxial compressive strain [6] is applied.

Until recently, one of the challenges hampering the development of high-performance antimonide-based p-channel MOSFETs has been the lack of low-resistance ohmic contact technology. Recently, a new p^+-InAs/InAsSb composite cap structure has resulted in Au-based contacts to antimonide heterostructures with contact resistivities approaching 1 $\Omega.\mu m^2$ [71]. In a more recent development, Au-less ohmic contacts have been achieved with contact resistivities just slightly higher [7]. These achievements bode well for the future of this device technology. Theoretical calculations of the Landauer limit for ohmic contact resistivity for this material system also suggest that significant improvements are to be expected [35].

A second critical requirement of an antimonide-based MOSFET is a high quality high-K oxide/semiconductor interface. Because of the highly reactive nature of antimonide compounds, surface passivation of GaSb or InGaSb is challenging. In recent years, several cleaning and passivation techniques have been proposed [72]–[75]. Among those, an HCl clean has been found to be an effective way to remove native oxides of GaSb. A lowest D_{it} value of $3x10^{11}$ $eV^{-1}.cm^{-2}$ [76] and a minimum subthreshold swing of 120 mV/dec [66] have been reported. Excellent planar MOSFETs [67] have been demonstrated that suggest significant performance potential for this material system.

As with InGaAs, in order to deploy InGaSb as a channel material in a future generation of CMOS technology, a multigate 3D structure is necessary. Recently, the first InGaSb p-channel FinFETs have been demonstrated [7]. Achieving this milestone required the development of dry-etch technology capable of creating high-aspect ratio fins with vertical sidewalls. As Fig. 12 shows, a novel BCl_3/N_2 RIE chemistry has made possible sub-20 nm wide InGaSb fins with vertical sidewalls and aspect ratio greater than 10. Also, dense fin patterns with excellent fin characteristics have been realized.

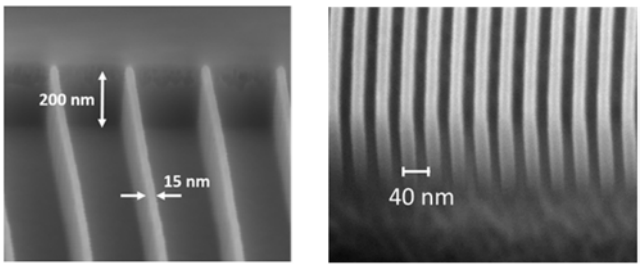

FIGURE 12. SEM images of sub-20 nm InGaSb (a) fins and (b) dense fin array with 20 nm fin spacing [7].

An encouraging finding about this RIE technology is the excellent electrical quality of the dry etched sidewalls after a light HCl etch treatment [7]. At least, this is the case for GaSb where initial experiments suggest a relatively low interface state density on the sidewall MOS structure. For InGaSb, the HCl chemical treatment is not suitable as it is difficult to control. A digital-etch process, similar to that used in the InGaAs system [60], is required for InGaSb-based heterostructures.

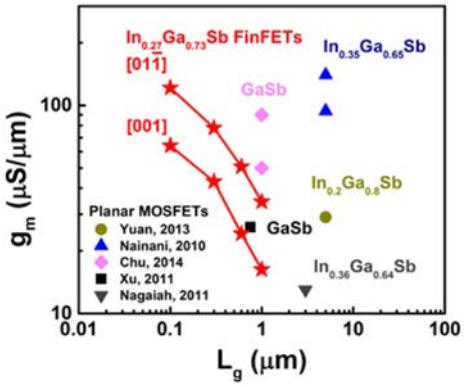

FIGURE 13. Maximum g_m vs. L_g of recently published InGaSb MOSFETs. All devices but the ones indicated by red stars are planar MOSFETs. The red star devices are FinFETs [7]. The strong orientation dependence of these devices suggests the important role of compressive uniaxial strain in hole transport.

The first InGaSb FinFETs feature fin widths as narrow as 30 nm and gate lengths down to 100 nm [7]. These are double-gate devices with carrier modulation taking place only through the sidewalls. In spite of this, these devices show promising electrical characteristics with a g_m (normalized by gate periphery) that approaches that of the best InGaSb planar MOSFETs. This highlights the excellent quality of the sidewalls that this process is capable of. A summary of the state of the art is shown in Fig. 13. The first InGaSb FinFETs also manifest a prominent orientation dependence. This suggests that the process of fin formation partially relaxes the as-grown biaxially strained channel resulting in a strong uniaxial compressive strain in the direction of hole transport [7].

The ultimate potential of the antimonide material system for logic p-type MOSFETs is uncertain as limited research has been carried out to date. Fast progress has recently been made in contacts, high-quality MOS stacks and high aspect ratio etching. This suggests substantial promise. However, the technology remains relatively immature when compared with alternatives (most prominently, Ge p-MOSFETs).

VI. CONCLUSION

Impressive recent III-V MOSFET progress gives hope for Moore's law to continue beyond the point where Si can reach. Planar and multigate InGaAs MOSFETs exhibit nearly ideal electrostatic scaling behavior. This bodes well for the potential of further scaling. However, device performance is still lacking particularly in scaled multigate designs. To overcome this problem, new research in low parasitic contact schemes and self-aligned designs is required. Recent progress in p-type InGaSb MOSFETs shows the promise of this material system for future nanoscale CMOS.

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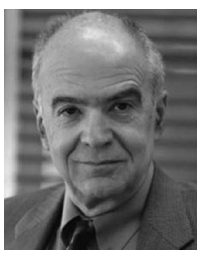

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