10. A. Schirotzek, C.-H. Wu, A. Sommer, M. W. Zwierlein, *Phys. Rev. Lett.* **102**, 230402 (2009).
11. S. Nascimbène *et al.*, *Phys. Rev. Lett.* **103**, 170402 (2009).
12. C. Kohstall *et al.*, *Nature* **485**, 615–618 (2012).
13. M. Koschorreck *et al.*, *Nature* **485**, 619–622 (2012).
14. Y. Zhang, W. Ong, I. Arakelyan, J. E. Thomas, *Phys. Rev. Lett.* **108**, 235302 (2012).
15. P. Massignan, M. Zaccanti, G. M. Bruun, *Rep. Prog. Phys.* **77**, 034401 (2014).
16. M. Sidler *et al.*, http://arXiv.org/abs/1603.09215 (2016).
17. J. Goold, T. Fogarty, N. Lo Gullo, M. Paternostro, T. Busch, *Phys. Rev. A* **84**, 063632 (2011).
18. M. Knap *et al.*, *Phys. Rev. X* **2**, 041020 (2012).
19. M. Cetina *et al.*, *Phys. Rev. Lett.* **115**, 135302 (2015).
20. See supplementary materials on *Science* Online.
21. D. Naik *et al.*, *Eur. Phys. J. D* **65**, 55–65 (2011).
22. J. Loschmidt, *Sitzungsber. Akad. Wissenschaften Wien* **73**, 128 (1876).
23. E. L. Hahn, *Phys. Rev.* **80**, 580–594 (1950).
24. P. Nozières, C. T. De Dominicis, *Phys. Rev.* **178**, 1097–1107 (1969).
25. R. A. Jalabert, H. M. Pastawski, *Adv. Solid State Phys.* **41**, 483–496 (2001).
26. F. Chevy, *Phys. Rev. A* **74**, 063628 (2006).
27. X. Cui, H. Zhai, *Phys. Rev. A* **81**, 041602 (2010).
28. J. Dubois *et al.*, *Nature* **502**, 659–663 (2013).
29. C. Mora, F. Chevy, *Phys. Rev. Lett.* **104**, 230402 (2010).
30. Z. Yu, S. Zöllner, C. J. Pethick, *Phys. Rev. Lett.* **105**, 188901 (2010).
31. W. Zwerger, Ed., *The BCS-BEC Crossover and the Unitary Fermi Gas* (Springer, 2012).
32. R. A. Hart *et al.*, *Nature* **519**, 211–214 (2015).
33. L. J. LeBlanc, J. H. Thywissen, *Phys. Rev. A* **75**, 053612 (2007).

ACKNOWLEDGMENTS

We thank M. Baranov, F. Schreck, G. Bruun, N. Davidson, and R. Folman for stimulating discussions. Supported by NSF through a grant for ITAMP at Harvard University and the Smithsonian Astrophysical Observatory (R.S.); the Technical University of Munich-Institute for Advanced Study, funded by the German Excellence Initiative and the European Union FP7 under grant agreement 291763 (M.K.); the Harvard-MIT Center for Ultracold Atoms, NSF grant DMR-1308435, the Air Force Office of Scientific Research Quantum Simulation Multidisciplinary University Research Initiative (MURI), the Army Research Office MURI on Atomtronics, M. Rössler, the Walter Haefner Foundation, the ETH Foundation, and the Simons Foundation (E.D.); and the Austrian Science Fund (FWF) within the SFB FoQuS (F4004-N23) and within the DK ALM (W1259-N27).

SUPPLEMENTARY MATERIALS

www.sciencemag.org/content/354/6308/96/suppl/DC1
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20 February 2016; accepted 6 September 2016
10.1126/science.aaf5134

DEVICE TECHNOLOGY

MoS_2 transistors with 1-nanometer gate lengths

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Scaling of silicon (Si) transistors is predicted to fail below 5-nanometer (nm) gate lengths because of severe short channel effects. As an alternative to Si, certain layered semiconductors are attractive for their atomically uniform thickness down to a monolayer, lower dielectric constants, larger band gaps, and heavier carrier effective mass. Here, we demonstrate molybdenum disulfide (MoS_2) transistors with a 1-nm physical gate length using a single-walled carbon nanotube as the gate electrode. These ultrashort devices exhibit excellent switching characteristics with near ideal subthreshold swing of ~65 millivolts per decade and an On/Off current ratio of ~10^6. Simulations show an effective channel length of ~3.9 nm in the Off state and ~1 nm in the On state.

As Si transistors rapidly approach their projected scaling limit of ~5-nm gate lengths, exploration of new channel materials and device architectures is of utmost interest (*1*–*3*). This scaling limit arises from short channel effects (*4*). Direct source-to-drain tunneling and the loss of gate electrostatic control on the channel severely degrade the Off state leakage currents, thus limiting the scaling of Si transistors (*5*, *6*). Certain semiconductor properties dictate the magnitude of these effects for a given gate length. Heavier carrier effective mass, larger band gap, and lower in-plane dielectric constant yield lower direct source-to-drain tunneling currents (*7*). Uniform and atomically thin semiconductors with low in-plane dielectric constants are desirable for enhanced electrostatic control of the gate. Thus, investigation and introduction of semiconductors that have more ideal properties than Si could lead to further scaling of transistor dimensions with lower Off state dissipation power.

Transition metal dichalcogenides (TMDs) are layered two-dimensional (2D) semiconductors that have been widely explored as a potential channel material replacement for Si (*8*–*11*), and each material exhibits different band structures and properties (*12*–*16*). The layered nature of TMDs allows uniform thickness control with atomic-level precision down to the monolayer limit. This thickness scaling feature of TMDs is highly desirable for well-controlled electrostatics in ultrashort transistors (*3*). For example, monolayer and few-layer MoS_2 have been shown theoretically to be superior to Si at the sub-5-nm scaling limit (*17*, *18*).

The scaling characteristics of MoS_2 and Si transistors as a function of channel thickness and gate length are summarized in Fig. 1. We calculated direct source-to-drain tunneling currents ($I_{SD\text{-}LEAK}$) in the Off state for different channel lengths and thicknesses using a dual-gate device structure (fig. S1) as a means to compare the two materials. MoS_2 shows more than two orders of magnitude reduction in $I_{SD\text{-}LEAK}$ relative to Si mainly because of its larger electron effective mass along the transport direction ($m_n^* \sim 0.55m_0$ for MoS_2 versus $m_n^* \sim 0.19m_0$ for Si [100]) (*19*), with a trade-off resulting in lower ballistic On current. Notably, $I_{SD\text{-}LEAK}$ does not limit the scaling of monolayer MoS_2 even down to the ~1-nm gate length, presenting a major advantage over Si [see more details about calculations in the supplementary materials (*20*)]. Finally, few-layer MoS_2 exhibits a lower in-plane dielectric constant (~4) compared with bulk Si (~11.7), Ge (~16.2), and GaAs (~12.9), resulting in a shorter electrostatic characteristic length (λ) as depicted in fig. S2 (*21*).

The above qualities collectively make MoS_2 a strong candidate for the channel material of future transistors at the sub-5-nm scaling limit. However, to date, TMD transistors at such small gate lengths have not been experimentally explored. Here, we demonstrate 1D gated, 2D semiconductor field-effect transistors (1D2D-FETs) with a single-walled carbon nanotube (SWCNT) gate, a MoS_2 channel, and physical gate lengths of ~1 nm. The 1D2D-FETs exhibit near ideal switching characteristics, including a subthreshold swing (SS) of ~65 mV per decade at room temperature and high On/Off current ratios. The SWCNT diameter $d \sim 1$ nm for the gate electrode (*22*) minimized parasitic gate to source-drain capacitance, which is characteristic of lithographically patterned tall gate structures. The ~1-nm gate length of the SWCNT also allowed for the experimental exploration of the device physics and properties of MoS_2 transistors as a function of semiconductor thickness (i.e., number of layers) at the ultimate gate-length scaling limit.

The experimental device structure of the 1D2D-FET (Fig. 2A) consists of a MoS_2 channel (number of layers vary), a ZrO_2 gate dielectric, and a SWCNT gate on a 50-nm SiO_2/Si substrate with a physical gate length ($L_G \sim d$) of ~1 nm. Long, aligned SWCNTs grown by chemical vapor deposition

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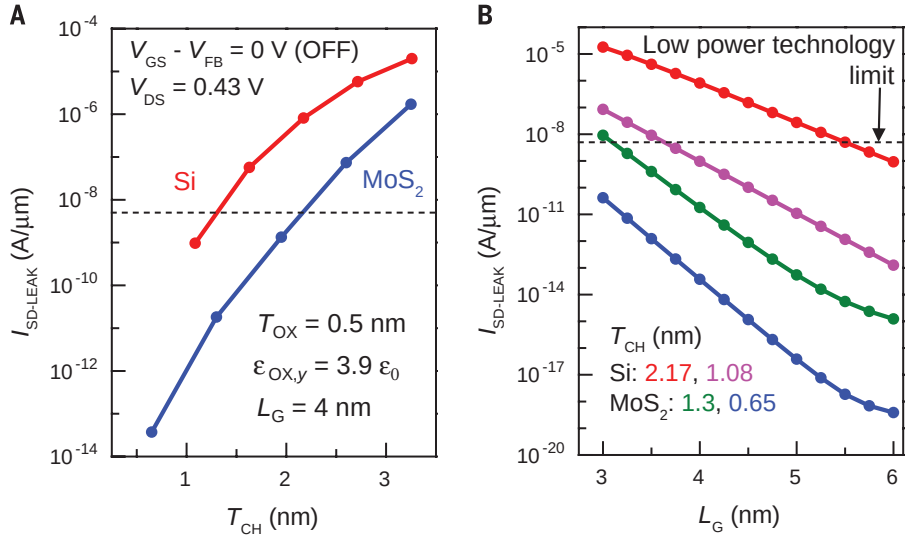

Fig. 1. Direct source-to-drain tunneling leakage current. (**A**) Normalized direct source-to-drain tunneling leakage current ($I_{SD-LEAK}$), calculated using the WKB (Wentzel-Kramers-Brillouin) approximation as a function of channel thickness T_{CH} for Si and MoS_2 in the Off state. $V_{DS} = V_{DD} = 0.43$ V from the International Technology Roadmap for Semiconductors (ITRS) 2026 technology node. (**B**) $I_{SD-LEAK}$ as a function of gate length L_G for different thicknesses of Si and MoS_2 for the same Off state conditions as Fig. 1A. The dotted line in Fig. 1, A and B represents the low operating power limit for the 2026 technology node as specified by the ITRS.

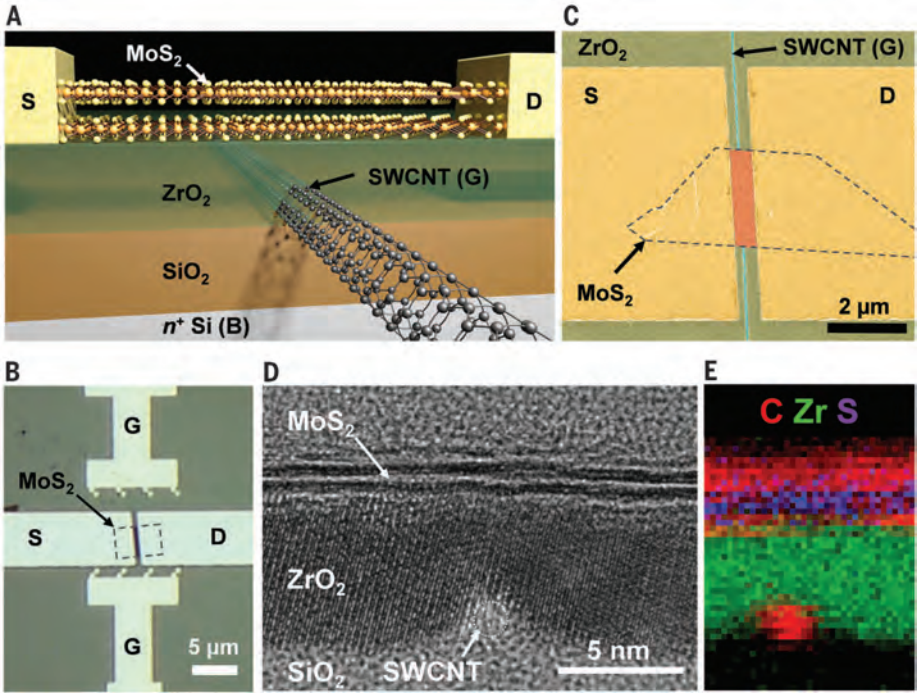

Fig. 2. 1D2D-FET device structure and characterization. (**A**) Schematic of 1D2D-FET with a MoS_2 channel and SWCNT gate. (**B**) Optical image of a representative device shows the MoS_2 flake, gate (G), source (S), and drain (D) electrodes. (**C**) False-colored SEM image of the device showing the SWCNT (blue), ZrO_2 gate dielectric (green), MoS_2 channel (orange), and the Ni source and drain electrodes (yellow). (**D**) Cross-sectional TEM image of a representative sample showing the SWCNT gate, ZrO_2 gate dielectric, and bilayer MoS_2 channel. (**E**) EELS map showing spatial distribution of carbon, zirconium, and sulfur in the device region, confirming the location of the SWCNT, MoS_2 flake, and ZrO_2 dielectric.

were transferred onto a n^+ Si/SiO_2 substrate (50-nm-thick SiO_2) (*23*), located with a scanning electron microscope (SEM), and contacted with palladium via lithography and metallization. These steps were followed by atomic layer deposition (ALD) of ZrO_2 and pick-and-place dry transfer of MoS_2 onto the SWCNT covered by ZrO_2 (*14*). Nickel source and drain contacts were made to MoS_2 to complete the device. The detailed process flow and discussion about device fabrication is provided in fig. S3.

Figure 2B shows the optical image of a representative 1D2D-FET capturing the MoS_2 flake, the source and drain contacts to MoS_2, and the gate contacts to the SWCNT. The SWCNT and the MoS_2 flake can be identified in the false-colored SEM image of a representative sample (Fig. 2C). The 1D2D-FET consists of four electrical terminals; source (S), drain (D), SWCNT gate (G), and the n^+ Si substrate back gate (B). The SWCNT gate underlaps the S/D contacts. These underlapped regions were electrostatically doped by the Si back gate during the electrical measurements, thereby serving as n^+ extension contact regions. The device effectively operated like a junctionless transistor (*24*), where the SWCNT gate locally depleted the n^+ MoS_2 channel after applying a negative voltage, thus turning Off the device.

A cross-sectional transmission electron microscope (TEM) image of a representative 1D2D-FET (Fig. 2D) shows the SWCNT gate, ZrO_2 gate dielectric (thickness T_{OX}~5.8 nm), and the bilayer MoS_2 channel. The topography of ZrO_2 surrounding the SWCNT and the MoS_2 flake on top of the gate oxide was flat, as seen in the TEM image. This geometry is consistent with ALD nucleation initiating on the SiO_2 substrate surrounding the SWCNT and eventually covering it completely as the thickness of deposited ZrO_2 exceeds the SWCNT diameter d (*25*). The spatial distribution of carbon, zirconium, and sulfur was observed in the electron energy-loss spectroscopy (EELS) map of the device region (Fig. 2E), thus confirming the location of the SWCNT, ZrO_2, and MoS_2 in the device (fig. S4) (*20*).

The electrical characteristics for a 1D2D-FET with a bilayer MoS_2 channel (Fig. 3) show that the MoS_2 extension regions (the underlapped regions between the SWCNT gate and S/D contacts) could be heavily inverted (i.e., n^+ state) by applying a positive back-gate voltage of $V_{BS} = 5$ V to the Si substrate. The I_D-V_{BS} characteristics (fig. S5) indicate that the MoS_2 flake was strongly inverted by the back gate at $V_{BS} = 5$ V. The I_D-V_{GS} characteristics for the device at $V_{BS} = 5$ V and $V_{DS} =$ 50 mV and 1 V (Fig. 3A) demonstrate the ability of the ~1-nm SWCNT gate to deplete the MoS_2 channel and turn Off the device. The 1D2D-FET exhibited excellent subthreshold characteristics with a near ideal SS of ~65 mV per decade at room temperature and On/Off current ratio of ~10^6. The drain-induced barrier lowering (DIBL) was ~290 mV/V. Leakage currents through the SWCNT gate (I_G) and the n^+ Si back gate (I_B) are at the measurement noise level (Fig. 3A). The interface trap density (D_{IT}) of the ZrO_2-MoS_2 interface estimated from SS was ~1.7 × 10^{12} cm^{-2} eV^{-1},

which is typical for transferred MoS_2 flakes (*26*) because of the absence of surface dangling bonds (*20*).

Figure 3B shows the I_D-V_{DS} characteristics at different V_{GS} values and fixed V_{BS} = 5 V. The I_D-V_{GS} characteristics depended strongly on the value of V_{BS}, which affects the extension region resistance. The inversion of the extension regions increased with increasing V_{BS}, thus reducing the series resistance and contact resistance and led to an increase in the On current and an improvement in the SS. At more positive values of V_{BS}, V_{GS} had to be more negative in order to deplete the MoS_2 channel, which in turn made the threshold voltage (V_T) more negative. Above V_{BS} = 1 V, the SS and I_{On} did not improve any further, and the extension regions were strongly inverted (Fig. 3C). Thus, the 1D2D-FET operated as a short-channel device.

We performed detailed simulations using Sentaurus TCAD to understand the electrostatics of the 1D2D-FET. The Off and On state conditions correspond to (V_{GS}-V_T) of −0.3 V and 1.5 V, respectively (which give an On/Off current ratio of ~10^6). The electric field contour plot (Fig. 3D) in the Off state has a region of low electric field in the MoS_2 channel near the SWCNT, indicating that it is depleted. The reduced electron density in the MoS_2 channel (Fig. 3E), and the presence of an energy barrier to electrons in the conduction band (fig. S6A) are also consistent with the Off state of the device. The extension regions are still under inversion because of the positive back-gate voltage. The electron density of the MoS_2 channel in the depletion region can be used to define the effective channel length (L_{EFF}) of the 1D2D-FET, which is the region of channel controlled by the SWCNT gate (*27*–*29*). The channel is considered to be depleted if the electron density falls below a defined threshold ($n_{threshold}$). The Off state L_{EFF}, defined as the region of MoS_2 with electron density $n < n_{threshold}$ ($n_{threshold}$ = 1.3 × 10^5 cm^{-2}), for this simulated 1D2D-FET is L_{EFF} ~ 3.9 nm (Fig. 3E). L_{EFF} is dependent on V_{GS} and the value of $n_{threshold}$ (fig. S7).

As the device is turned Off, the fringing electric fields from the SWCNT (Fig. 3D) deplete farther regions of the MoS_2 channel and thus increase L_{EFF}. The short height of the naturally defined SWCNT gate prevents large fringing fields from controlling the channel and hence achieves a smaller L_{EFF} compared with lithographically patterned gates (fig. S8). The electric field and electron density contours for the device in the On state confirm the strong inversion of the channel region near the SWCNT (Fig. 3, F and G) with L_{EFF} ~ L_G = 1 nm. The energy bands in this case are flat in the entire channel region (fig. S6B), with the On state current being limited by the resistance of the extension regions and mainly the contacts. Doped S/D contacts along with shorter extension regions will result in increased On current.

The effect of T_{OX} scaling on short-channel effects like DIBL was also studied using simulations (fig. S9). The electrostatics of the device improves, and the influence of the drain on the channel reduces, as T_{OX} is scaled down to values

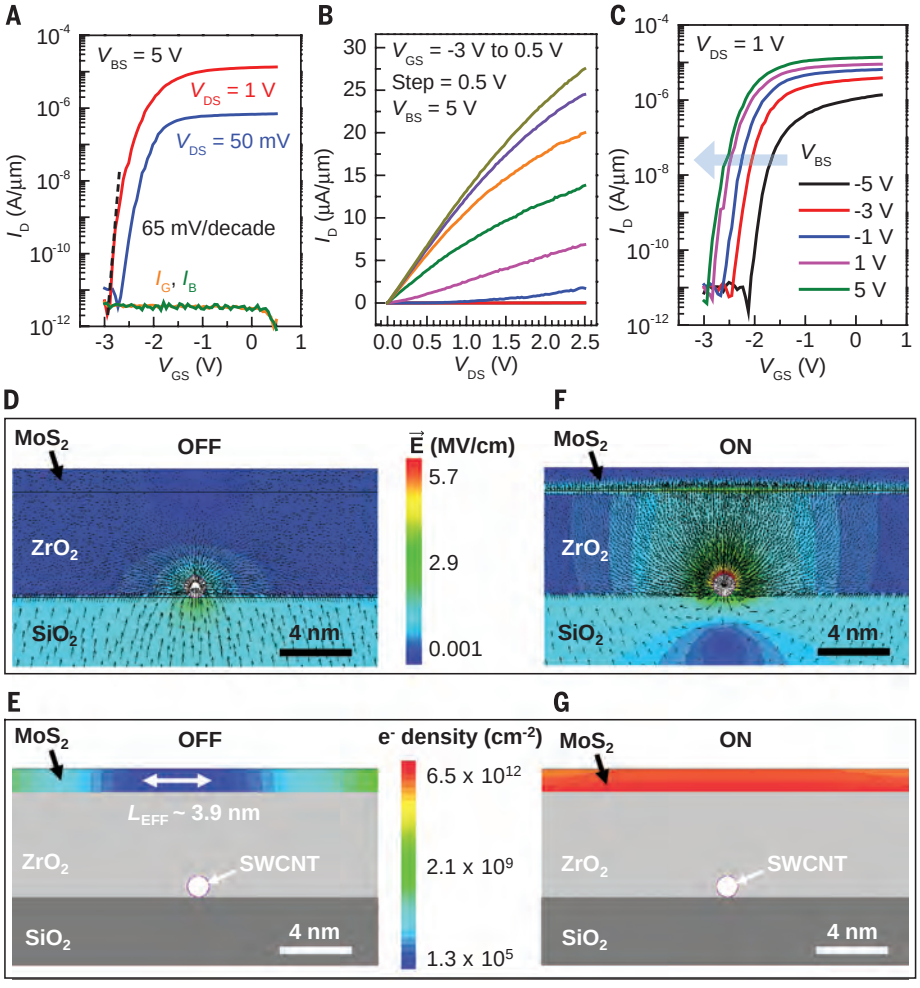

Fig. 3. Electrical characterization and TCAD simulations of 1D2D-FET. (**A**) I_D-V_{GS} characteristics of a bilayer MoS_2 channel SWCNT gated FET at V_{BS} = 5 V and V_{DS} = 50 mV and 1 V. The positive V_{BS} voltage electrostatically dopes the extension regions n^+. (**B**) I_D-V_{DS} characteristic for the device at V_{BS} = 5 V and varying V_{GS}. (**C**) I_D-V_{GS} characteristics at V_{DS} = 1 V and varying V_{BS} illustrating the effect of back-gate bias on the extension region resistance, SS, On current, and device characteristics. Electric field contour plots for a simulated bilayer MoS_2 device using TCAD in the (**D**) Off and (**F**) On state. Electron density plots for the simulated device using TCAD in the (**E**) Off and (**G**) On state. The electron density in the depletion region is used to define the L_{EFF}. L_{EFF} ~ d ~ L_G in the On state and L_{EFF} > L_G in the Off state because of the fringing electric fields from the SWCNT gate.

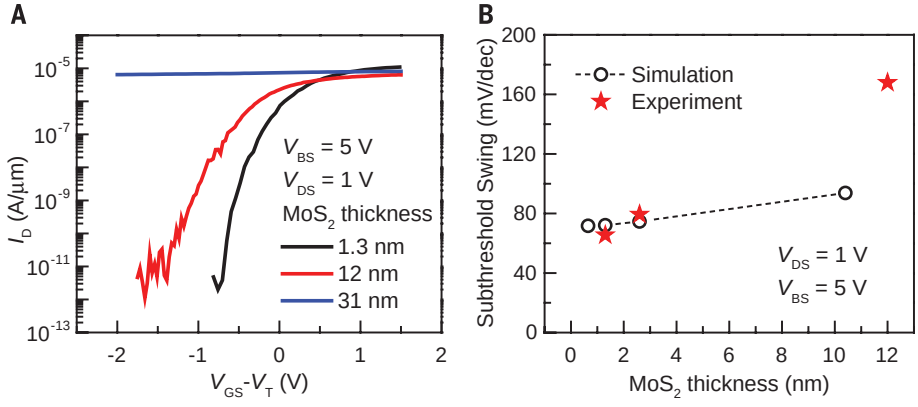

Fig. 4. MoS_2 thickness dependence. (**A**) Dependence of MoS_2 channel thickness on the performance of 1D2D-FET. SS increases with increasing MoS_2 channel thickness. (**B**) Extracted SS from experimental curves and TCAD simulations show increasing SS as channel thickness T_{CH} increases.

commensurate with L_G. This effect is seen by the strong dependence of DIBL on T_{OX}, thus demonstrating the need for T_{OX} scaling and high-κ (dielectric constant) 2D dielectrics to further enhance the device performance.

The effect of MoS_2 thickness on the device characteristics was systematically explored. At the scaling limit of the gate length, the semiconductor channel thickness must also be scaled down aggressively, as described earlier. The electrostatic control of the SWCNT gate on the MoS_2 channel decreased with increasing distance from the ZrO_2-MoS_2 interface. Thus, as the MoS_2 flake thickness was increased, the channel could not be completely depleted by applying a negative V_{GS}. Because of this effect, the SS for a 12-nm-thick MoS_2 device (~170 mV per decade) was much larger than that of bilayer MoS_2 (~65 mV per decade), and as the thickness of MoS_2 was increased to ~31 nm, the device could no longer be turned off (Fig. 4A). The experimental SS as a function of MoS_2 thickness was qualitatively consistent with the TCAD simulations (Fig. 4B and S10), showing an increasing trend with increasing channel thickness. The unwanted variations in device performance caused by channel thickness fluctuations (Fig. 4B and fig. S10), and the need for low Off state current at short channel lengths (Figs. 1 and 3), thus justify the need for layered semiconductors like TMDs at the scaling limit.

TMDs offer the ultimate scaling of thickness with atomic-level control, and the 1D2D-FET structure enables the study of their physics and electrostatics at short channel lengths by using the natural dimensions of a SWCNT, removing the need for any lithography or patterning processes that are challenging at these scale lengths. However, large-scale processing and manufacturing of TMD devices down to such small gate lengths are existing challenges requiring future innovations. For instance, research on developing process-stable, low-resistance ohmic contacts to TMDs, and scaling of the gate dielectric by using high-κ 2D insulators is essential to further enhance device performance. Wafer-scale growth of high-quality films (*30*) is another challenge toward achieving very-large-scale integration of TMDs in integrated circuits. Finally, fabrication of electrodes at such small scale lengths over large areas requires considerable advances in lithographic techniques. Nevertheless, the work here provides new insight into the ultimate scaling of gate lengths for a FET by surpassing the 5-nm limit (*3*–*7*) often associated with Si technology.

REFERENCES AND NOTES

1. T. N. Theis, P. M. Solomon, *Science* **327**, 1600–1601 (2010).
2. R. Chau, B. Doyle, S. Datta, J. Kavalieros, K. Zhang, *Nat. Mater.* **6**, 810–812 (2007).
3. A. D. Franklin, *Science* **349**, aab2750 (2015).
4. M. Lundstrom, *Science* **299**, 210–211 (2003).
5. M. Luisier, M. Lundstrom, D. A. Antoniadis, J. Bokor, in *Electron Devices Meeting (IEDM), 2011 IEEE International* (IEEE, 2011), pp. 11.12.11–1.12.14.
6. H. Kawaura, T. Sakamoto, T. Baba, *Appl. Phys. Lett.* **76**, 3810–3812 (2000).
7. W. S. Cho, K. Roy, *IEEE Electron Device Lett.* **36**, 427–429 (2015).
8. B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, A. Kis, *Nat. Nanotechnol.* **6**, 147–150 (2011).
9. D. Sarkar *et al.*, *Nature* **526**, 91–95 (2015).
10. H. Liu, A. T. Neal, P. D. Ye, *ACS Nano* **6**, 8563–8569 (2012).
11. H. Wang *et al.*, *Nano Lett.* **12**, 4674–4680 (2012).
12. K. F. Mak, K. L. McGill, J. Park, P. L. McEuen, *Science* **344**, 1489–1492 (2014).
13. D. Jariwala, V. K. Sangwan, L. J. Lauhon, T. J. Marks, M. C. Hersam, *ACS Nano* **8**, 1102–1120 (2014).
14. H. Fang *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **111**, 6198–6202 (2014).
15. K. S. Novoselov *et al.*, *Proc. Natl. Acad. Sci. U.S.A.* **102**, 10451–10453 (2005).
16. C.-H. Lee *et al.*, *Nat. Nanotechnol.* **9**, 676–681 (2014).
17. Y. Yoon, K. Ganapathi, S. Salahuddin, *Nano Lett.* **11**, 3768–3773 (2011).
18. L. Liu, Y. Lu, J. Guo, *IEEE Trans. Electron. Dev.* **60**, 4133–4139 (2013).
19. D. Wickramaratne, F. Zahid, R. K. Lake, *J. Chem. Phys.* **140**, 124710 (2014).
20. Supplementary materials are available on *Science* Online.
21. K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, Y. Arimoto, *IEEE Trans. Electron. Dev.* **40**, 2326–2329 (1993).
22. J. Svensson *et al.*, *Nanotechnology* **19**, 325201 (2008).
23. N. Patil *et al.*, *IEEE Trans. NanoTechnol.* **8**, 498–504 (2009).
24. J.-P. Colinge *et al.*, *Nat. Nanotechnol.* **5**, 225–229 (2010).
25. A. Javey *et al.*, *Nano Lett.* **4**, 1319–1322 (2004).
26. X. Zou *et al.*, *Adv. Mater.* **26**, 6255–6261 (2014).
27. Y. Taur, *IEEE Trans. Electron. Dev.* **47**, 160–170 (2000).
28. L. Barbut, F. Jazaeri, D. Bouvet, J.-M. Sallese, *Int. J. Microelectron. Comput. Sci.* **4**, 103–109 (2013).
29. S. Hong, K. Lee, *IEEE Trans. Electron. Dev.* **42**, 1461–1466 (1995).
30. K. Kang *et al.*, *Nature* **520**, 656–660 (2015).

ACKNOWLEDGMENTS

S.B.D. and A.J. were supported by the Electronics Materials program funded by the Director, Office of Science, Office of Basic Energy Sciences, Materials Sciences and Engineering Division of the U.S. Department of Energy under contract DE-AC02-05CH11231. A.B.S. was funded by Applied Materials, Inc., and Entegris, Inc., under the I-RiCE program. J.P.L. and J.B. were supported in part by the Office of Naval Research BRC program. J.P.L. acknowledges a Berkeley Fellowship for Graduate Studies and the NSF Graduate Fellowship Program. Q.W. and M.J.K. were supported by the NRI SWAN Center and Chinese Academy of Sciences President's International Fellowship Initiative (2015VTA031). G.P. and H.-S.P.W. were supported in part by the SONIC Research Center, one of six centers supported by the STARnet phase of the Focus Center Research Program (FCRP) a Semiconductor Research Corporation program sponsored by MARCO and DARPA. A.J., H.-S.P.W., and J.B. acknowledge the NSF Center for Energy Efficient Electronics Science (E^3S). A.J. acknowledges support from Samsung. The authors acknowledge the Molecular Foundry, Lawrence Berkeley National Laboratory for access to the scanning electron microscope. The authors acknowledge H. Fahad for useful discussions about the analytical modeling. All data are reported in the main text and supplementary materials.

SUPPLEMENTARY MATERIALS

www.sciencemag.org/content/354/6308/99/suppl/DC1
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30 June 2016; accepted 7 September 2016
10.1126/science.aah4698

BIOCATALYSIS

An artificial metalloenzyme with the kinetics of native enzymes

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Natural enzymes contain highly evolved active sites that lead to fast rates and high selectivities. Although artificial metalloenzymes have been developed that catalyze abiological transformations with high stereoselectivity, the activities of these artificial enzymes are much lower than those of natural enzymes. Here, we report a reconstituted artificial metalloenzyme containing an iridium porphyrin that exhibits kinetic parameters similar to those of natural enzymes. In particular, variants of the P450 enzyme CYP119 containing iridium in place of iron catalyze insertions of carbenes into C–H bonds with up to 98% enantiomeric excess, 35,000 turnovers, and 2550 hours^{-1} turnover frequency. This activity leads to intramolecular carbene insertions into unactivated C–H bonds and intermolecular carbene insertions into C–H bonds. These results lift the restrictions on merging chemical catalysis and biocatalysis to create highly active, productive, and selective metalloenzymes for abiological reactions.

The catalytic activity of a metalloenzyme is determined by both the primary coordination sphere of the metal and the surrounding protein scaffold. In some cases, laboratory evolution has been used to develop variants of native metalloenzymes for selective reactions of unnatural substrates (*1*, *2*). Yet with few exceptions (*3*), the classes of reactions that such enzymes undergo are limited to those of biological transformations. To combine the favorable qualities of enzymes with the diverse reactivity of synthetic transition-metal catalysts, abiological transition-metal centers or cofactors have been incorporated into native proteins. The resulting artificial metalloenzymes catalyze classes of reactions for which there is no known enzyme (abiological transformations) (*3*, *4*).

Although the reactivity of these artificial systems is new for an enzyme, the rates of these reactions have been much slower and the

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Science

MoS_2 transistors with 1-nanometer gate lengths

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Science **354** (6308), 99-102.
DOI: 10.1126/science.aah4698

A flatter route to shorter channels

High-performance silicon transistors can have gate lengths as short as 5 nm before source-drain tunneling and loss of electrostatic control lead to unacceptable leakage current when the device is off. Desai *et al.* explored the use of MoS_2 as a channel material, given that its electronic properties as thin layers should limit such leakage. A transistor with a 1-nm physical gate was constructed with a MoS_2 bilayer channel and a single-walled carbon nanotube gate electrode. Excellent switching characteristics and an on-off state current ratio of ~10^6 were observed.

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