Design Requirements for a Spintronic MTJ Logic Device for Pipelined Logic Applications

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***Abstract*— Spintronic devices have been spotlighted due to their nonvolatility and potential for low-voltage operation. However, their potential performance and energy efficiency require greater scrutiny. In this paper, a circuit-level energy-performance analysis is used to derive the design requirements for a spintronic magnetic tunnel junction logic device, *mLogic*, for pipelined logic applications. An analytical equation for the domain wall mobility of *mLogic* is derived to predict the performance of future designs and used to point to key directions for further device improvement. We show that the energy dissipation of a logic pipeline under delay constraints is a convex function of the write/read-path resistance ratio and the supply voltage. Scaling the supply voltage can reduce the energy dissipation at the expense of switching speed, but is limited by an extrinsic pinning effect and thermal noise. The energy reduction by maximizing the tunnel magnetoresistance (TMR) will be saturated for TMR larger than 100. But maximizing TMR can mitigate the thermal noise limit of scaling the supply voltage. The energy gap between MOSFETs and *mLogic* gets smaller for more advanced technology nodes. With 32-nm technology, a future *mLogic* design can be more optimal than MOSFETs in low-power and low-performance applications, such as emerging Internet-of-Things devices.**

***Index Terms*— Domain wall (DW) motion, Internet-of-Things (IoT), magnetic logic device, magnetic tunnel junction (MTJ), *mLogic*, optimization, pipelined logic, spin Hall effect (SHE), spin-transfer torque (STT), spintronics.**

I. Introduction

SPINTRONIC logic devices are given the spotlight as a potential alternative to MOSFETs, which are facing obstacles in scalability due to high power density induced by the finite subthreshold slope [1]. Of special interest is a category of spintronic devices, which uses a magnetic tunnel junction (MTJ) or a spin valve (SV) as a read path that is analogous to the MOSFET channel, and flips the free layer magnetization of the MTJ/SV by the charge current in a write path that is analogous to the MOSFET gate [2]. Such a category of spintronic devices can be called the spintronic MTJ logic. All-metallic properties of the spintronic MTJ logic enable sub-100-mV voltage operation, and so the spintronic MTJ logic has the potential to be more optimal than MOSFETs in low-performance and low-power applications, such as Internet of Things (IoT) [4], [5]. Most things in the IoT, including sensors, actuators, connectivity products, and so on, are mobile and energy hungry, and so operate at subgigahertz clock frequencies for low-power consumption [6], [7]. This paper will assess the potential of spintronic MTJ logic for subgigahertz clock frequency applications.

Many spintronic devices [8]–[17] fall in the category of spintronic MTJ logic, and among them, *mLogic* [8]–[12] is one of the scalable and energy-efficient designs. There are various possible physical mechanisms to flip the MTJ/SV free layer magnetization. One of the early designs of spintronic MTJ logic, transpinnor, uses the Oersted field generated by the write-path current to flip their SV free layer magnetization [13]. However, such devices [13], [14] are neither scalable nor energy efficient [2]. Other mechanisms that are both scalable and energy efficient include spin-transfer torque (STT)-driven domain wall (DW) motion [15], spin injection via spin accumulation in a ferromagnetic/nonmagnetic layer interface [16], and spin Hall effect (SHE)-generated spin injection [17]. The *mLogic* is both scalable and energy efficient as it utilizes the DW motion driven by both the STT and SHE in the write path. A prototype of *mLogic* was fabricated and tested [10]–[12]. Although a few circuit-level analyses on *mLogic* are given for specific applications, including FFT [8], associative memory [18], and SRAM [19], there is a lack of general circuit-level analysis and design methodology that captures the energy-delay tradeoffs and possible tuning knobs. This paper will optimize and analyze a general logic pipeline of *mLogic* in various performance regimes.

Following the setup in [3] used for CMOS switches, we aim to identify the key device optimization knobs and connect them to the application/block level energy and performance metrics, in order to help the device designers understand their key constraints and future opportunities for device development. This paper first derives a compact model of *mLogic* [8]–[12] that will be used for a circuit-level analysis. The equations for time delay and energy dissipation of an *mLogic* buffer chain that represents a general logic pipeline will be derived as a function of geometric parameters and material parameters of the device. The energy is optimized under a delay constraint using the Lagrange multiplier method. The optimization gives the optimal values for the read/write-path resistance ratio and the supply voltage. The layout of the device is reviewed to minimize the geometric dimensions, and an equation for the

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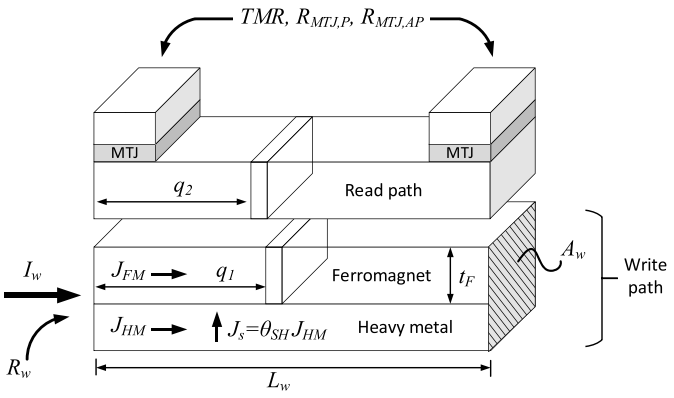

Fig. 1. Structure and dimensions of the *mLogic* device. q_1 and q_2 are the positions of the DWs in the write and read paths, respectively.

DW mobility is inspected to provide a guideline for choosing optimal magnetic properties for the device. We discuss two limiting effects of scaling the supply voltage: an extrinsic pinning effect and thermal noise-induced circuit errors. Finally, a scaled design of an *mLogic* device is conceived and compared with MOSFETs.

II. Spintronic MTJ Device Modeling

The *mLogic* device can be modeled as a nonvolatile four-terminal switch that has one read port and one write port. The physical device of *mLogic* has two ferromagnetic nanowires: the read path and the write path (see Fig. 1). On top of the read path are two MTJs, which are connected to the read port. So, the resistance seen at the read port depends on the magnetization configuration in the read path. The two ends of the write path are connected to the write port. Below the write path is a paramagnetic heavy-metal layer. As charge current I_w is injected into the write port, the electron current in the ferromagnetic layer of the write path drags the DW by the conventional STT [20]. At the same time, charge current in the heavy-metal layer generates spin current via the SHE (J_s in Fig. 1), and the spin current provides additional driving force to the DW motion in the write path if the DW has Neel characteristic [21]. The Neel characteristic of the DW can be sustained by the Dzyaloshinskii–Moriya interaction (DMI) from other peripheral layers [21]. Since the ferromagnetic layer of the write path is thicker than 1 nm, the STT term cannot be ignored as in [21] or [22]. The magnetizations in the two nanowires are coupled by a Ruderman-Kittel-Kasuya-Yosida-style exchange interaction through a magnetic oxide [23]. The write and read paths must be electrically isolated to prevent the read current from perturbing the DW motion in the write path. The DW position in the read path represents the internal state of the device and determines the resistance seen at the read port.

For a given charge current density into the write port, the DW speed in the read path determines the switching speed of the device. So, a new performance-related parameter called DW mobility, μ_{DW}, can be defined as the ratio between the DW speed in the read path and the current density in the write path. The DW speed v_J and the dynamics of the azimuth angle of magnetization ϕ for one independent nanowire are given in [21]. The DMI interaction stabilizes the Neel DW against deformation, which implies that the azimuth angle ϕ sustains its steady value, which is close to zero and so we can assume $\phi \simeq 0$. The exchange interaction with the magnetization in the read path hinders the DW motion in the write path, and so halves the DW speed in both nanowires, i.e., $dq_1/dt = dq_2/dt = v_J/2$, where q_1 and q_2 are the positions of the DWs in the write and read paths, respectively (see the Supplementary Material). Thus, the equation for μ_{DW} can be derived as

$$\mu_{\mathrm{DW}} \equiv \frac{1}{J}\frac{dq_2}{dt} = \frac{v_J}{2J} = \frac{1}{2(1+\alpha^2)}\left[\frac{(1+\alpha\beta)\mu_B P}{eM_s}\frac{J_{\mathrm{FM}}}{J} + \frac{\pi\alpha\gamma_0\Delta\hbar\theta_{\mathrm{SH}}}{4\mu_0 eM_s t_F}\frac{J_{\mathrm{HM}}}{J}\right] \quad (1)$$

where J is the total average current density in the write path, J_{FM} (or J_{HM}) is the current density in the ferromagnetic (or heavy-metal) part of the write path, α is the Gilbert damping factor, β is the degree of nonadiabatic STT, P is the degree of spin polarization, M_s is the saturation magnetization, μ_B is the Bohr magnetron, γ_0 is the gyromagnetic ratio, Δ is the DW width, θ_{SH} is the spin Hall angle, and t_F is the ferromagnetic layer thickness.

Equation (1) for μ_{DW} can be used to predict the DW mobility of either an existing or future design of *mLogic*. For example, (1) gives an approximate value for μ_{DW} of a fabricated prototype of *mLogic* [10]–[12]. We can estimate (see the Supplementary Material) the DW mobility to be $\mu_{\mathrm{DW}} = 1.81 \times 10^{-11}$ m^3/C, which is close to those obtained from the Kerr image ($\mu_{\mathrm{DW}} = 3.33 \times 10^{-11}$ m^3/C) [10] and the measured switching speed of the fabricated prototype ($\mu_{\mathrm{DW}} = 2.75 \times 10^{-11}$ m^3/C) [10]–[12].

III. Energy and Delay Equation Derivation

This section derives the energy dissipation and time delay equations for a chain of *mLogic* buffers/inverters that represents an abstracted logic pipeline stage (see Fig. 2). The resistive power dissipation of each buffer is

$$P_R^{(1)} = \frac{(V_{\mathrm{DD}}/2 - V_o)^2}{R_{\mathrm{pu}}} + \frac{(V_{\mathrm{DD}}/2 + V_o)^2}{R_{\mathrm{pd}}} + \frac{V_o^2}{2FR_w} \quad (2)$$

where V_{DD} is the voltage difference between the two power supply rails, $R_{\mathrm{pu/pd}}$ is the pull-up/pull-down network resistance of the buffer, R_w is the resistance of the write path, F is the number of the next stage buffers that each buffer drives, and V_o is the output voltage at steady state [8]

$$V_o = \frac{V_{\mathrm{DD}}}{2}\frac{\left(\frac{1}{R_{\mathrm{pu}}} - \frac{1}{R_{\mathrm{pd}}}\right)}{\left(\frac{1}{2FR_w} + \frac{1}{R_{\mathrm{pu}}} + \frac{1}{R_{\mathrm{pd}}}\right)}. \quad (3)$$

Depending on the state of the buffer, either $R_{\mathrm{pu}} = R_{\mathrm{MTJ,P}}$, $R_{\mathrm{pd}} = R_{\mathrm{MTJ,AP}}$ or $R_{\mathrm{pu}} = R_{\mathrm{MTJ,AP}}$, $R_{\mathrm{pd}} = R_{\mathrm{MTJ,P}}$, where $R_{\mathrm{MTJ,P/AP}}$ is the parallel/antiparallel resistance of the MTJ of the read path. Since the energy dissipation and the time

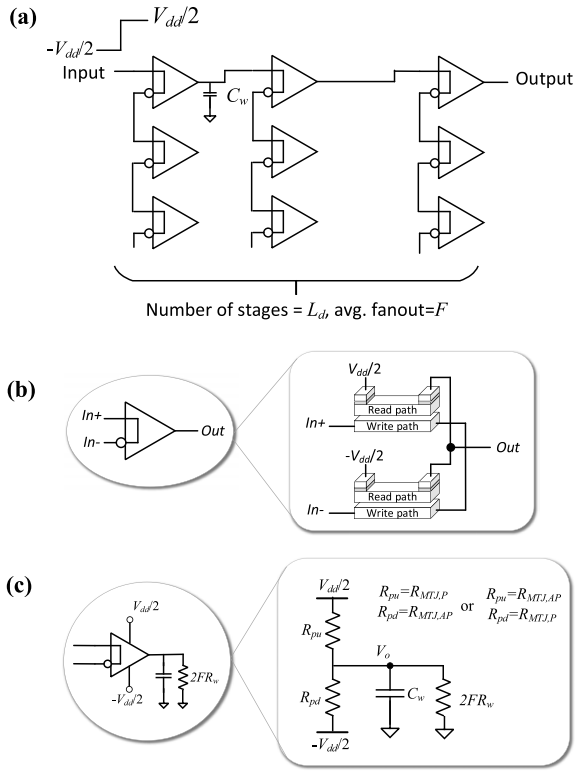

Fig. 2. (a) L_d-stage buffer chain used to represent a general logic pipeline stage of *mLogic*. The whole circuit represents a single pipeline stage, where each stage of *mLogic* buffers represents a logic stage. Every logic stage is constantly driven by the two power rails $V_{\rm DD}/2$ and $-V_{\rm DD}/2$. Every two consecutive logic stages are connected to each other by a long wire that has $O(1\ \text{fF})$ parasitic capacitance. (b) Internal circuit of an *mLogic* buffer. (c) Equivalent circuit for each *mLogic* buffer in the buffer chain in (a). The pull-up and pull-down network resistances of the buffer, $R_{\rm pu/pd}$, are the MTJ resistance of the read path, $R_{\rm MTJ,AP/P}$. The output of each buffer is connected to the parasitic wire capacitor C_w and a series of the write path resistors of the next stage buffers $2FR_w$.

delay of the buffer are the same in both states, the follow-on expressions are valid for both states. If we define a new variable x as

$$x \equiv R_w/R_{\rm MTJ,AP} \tag{4}$$

then we can rewrite V_o and $P_R^{(1)}$ as

$$|V_o| = \frac{V_{\rm DD}}{2}\frac{2xF\cdot \text{TMR}}{1+2xF(\text{TMR}+2)} \tag{5a}$$

$$P_R^{(1)} = \frac{V_{\rm DD}^2}{8FR_w}\frac{2xF[2+8xF+(1+8xF)\text{TMR}]}{1+2xF(\text{TMR}+2)} \tag{5b}$$

where $\text{TMR} = R_{\rm MTJ,AP}/R_{\rm MTJ,P}-1$ is the tunnel magnetoresistance (TMR) of the read path MTJ. As the read path of *mLogic* corresponds to the MOSFET channel, the TMR is analogous to the $I_{\rm ON}/I_{\rm OFF}$ ratio of charge-based transistors. While the $I_{\rm ON}/I_{\rm OFF}$ ratio of MOSFETs is $\sim 10^5$, a typical value of the TMR ranges from 1 to 6.

Due to the parasitic wire capacitance C_w between two consecutive logic stages, there is additional dynamic energy for charging/discharging the wire caps. Using the Kirchhoff current law, we can derive the dynamic energy of each wire capacitance between adjacent buffers as (see the Supplementary Material)

$$E_C^{(1)} = 2C_w V_o^2. \tag{6}$$

The total dynamic energy of the buffer chain is $E_C = \alpha_{\rm sw} L_d F E_C^{(1)}$, where $\alpha_{\rm sw}$ is the activity factor and L_d is the total number of logic stages in the buffer chain.

In a low-voltage operation regime, the resistance of *mLogic* is $O(1\ \text{k}\Omega)$, and the DW propagation time is $O(1\ \text{ns})$ [8], [9]. So, the RC delay which is $1\ \text{fF}\times 1\ \text{k}\Omega = O(1\ \text{ps})$ is negligible compared with the DW propagation time. Therefore, the time delay for each buffer stage is dominated by the time for the DW in the read path to travel from one end to another

$$t_d^{(1)} = \gamma_c \frac{L_w}{|dq_2/dt|} = \gamma_c \frac{L_w}{\mu_{\rm DW}|J_w|} = \gamma_c \frac{L_w A_w}{\mu_{\rm DW}|I_w|} \tag{7}$$

where dq_2/dt is the DW speed in the read path, γ_c is a correction factor due to the overlap of transitions between two adjacent stages, L_w is the length of the write/read path, I_w (or J_w) is the charge current (density) in the write path, and A_w is the cross-sectional area of the write path. Since $I_w = V_o/2FR_w$, the total time delay of the buffer chain is

$$t_d = L_d t_d^{(1)} = \gamma_c \cdot L_d F \cdot \frac{4\mu_{\rm DW}^{-1}\rho_w L_w^2}{V_{\rm DD}} \cdot \frac{1+2xF(\text{TMR}+2)}{2xF\cdot \text{TMR}}. \tag{8}$$

Finally, the total energy dissipation per switching is

$$\begin{aligned} E &= E_C + E_R = \alpha_{\rm sw} L_d F E_C^{(1)} + L_d F P_R^{(1)} t_d \\ &= \frac{1}{2}\alpha_{\rm sw} L_d F C_w V_{\rm DD}^2 \frac{(2xF)^2\text{TMR}^2}{(1+2xF(\text{TMR}+2))^2} \\ &\quad + \frac{1}{2}\gamma_c L_d^2 F \mu_{\rm DW}^{-1} L_w A_w V_{\rm DD} \frac{2+8xF+(1+8xF)\text{TMR}}{\text{TMR}}. \end{aligned} \tag{9}$$

The order of magnitude of the ratio between the dynamic and the resistive energy is around $E_C/E_R \sim C_w V_{\rm DD}/L_d \mu_{\rm DW}^{-1} L_w A_w \sim R_w C_w/t_d$, which is the ratio between the RC delay ($R_w C_w$) and the DW propagation time t_d. Since the DW propagation time is much longer than the RC delay in a low-voltage operation regime, the energy dissipation of the logic pipeline of *mLogic* is always dominated by the resistive energy. This contrasts the CMOS where the dominance of the resistive (or leakage) and dynamic energies varies with the operation regions.

IV. Energy-Delay Optimization

There are seven independent parameters that can be tweaked by either the change of the material or redesign of the device: $x = R_w/R_{\rm MTJ,AP}$, TMR, ρ_w, L_w, A_w, $V_{\rm DD}$, and $\mu_{\rm DW}$. In this section, we will minimize the energy dissipation subject to a delay constraint, that is

$$\begin{aligned} &\min\ E(x, \text{TMR}, \rho_w, L_w, A_w, V_{\rm DD}, \mu_{\rm DW}) \\ &\text{when}\ D(x, \text{TMR}, \rho_w, L_w, A_w, V_{\rm DD}, \mu_{\rm DW}) \le t_d \end{aligned} \tag{10}$$

where D is the time delay function. There are no positive optimal values for ρ_w, L_w, A_w, $\mu_{\rm DW}$, and TMR because for a given delay constraint, the lower limit of energy dissipation will be a monotonic function of each of those parameters.

TABLE I
DESIGN REQUIREMENTS FOR *mLogic* DEVICES

parameter	name	requirement
μ_{DW}	DW mobility	as large as possible
ρ_w	write path resistivity	as small as possible
L_w	write path length	as small as possible
A_w	write path cross-section	as small as possible
TMR	read path MTJ TMR	as large as possible

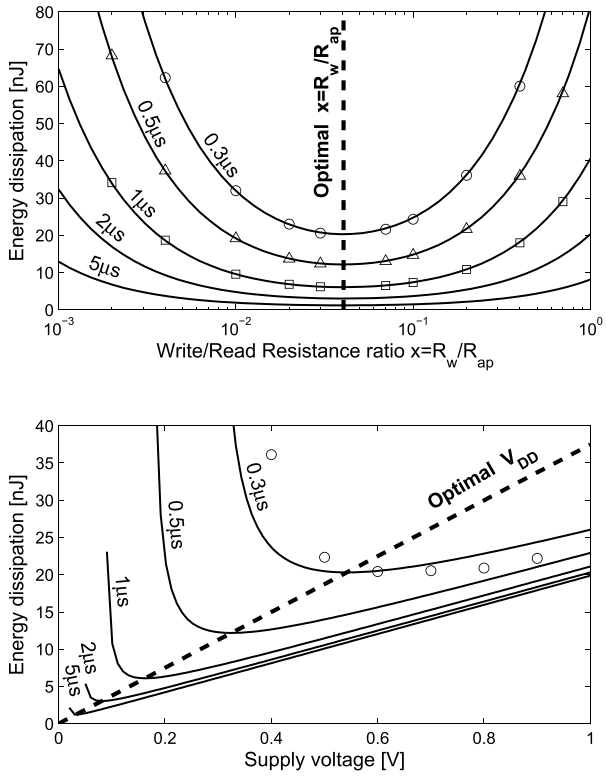

Fig. 3. Energy dissipation of an *mLogic* buffer chain ($L_d = 10$, $F = 4$, and $\alpha_{\text{sw}} = 0.05$) versus $x = R_w/R_{\text{MTJ,AP}}$ or supply voltage V_{DD} for the fixed time delays of the *mLogic* buffer chain. The full lines are derived from the energy-delay equations (8) and (9), and the data points are SPICE simulations with time delay being equal to 0.3, 0.5, and 1 μs for ○, △, and □, respectively. The correction factor γ_c is fitted to $\gamma_c = 0.46$ to match with the SPICE results. The device parameters of *mLogic* are set to those of a fabricated prototype [10]–[12], i.e., $L_w = 273$ nm, $A_w = 1\ \mu\text{m} \times 4.3$ nm, $\rho_w = 8.48 \times 10^{-8}\ \Omega \cdot \text{m}$, TMR = 138%, $\mu_{\text{DW}} = 1.81 \times 10^{-11}\ \text{C}^{-1}\text{m}^3$, and $C_w = 5$ fF.

Therefore, the requirement for each of those parameters can be summarized as shown in Table I. It is preferred to design a small volume of the material with low electrical resistivity for the write path and have a high TMR for the read-path MTJ. But the energy dissipation is convex in the other parameters: x and V_{DD} (see Fig. 4).

For a given set of values of ρ_w, L_w, A_w, μ_{DW}, and TMR, the energy dissipation can be minimized with respect to x and V_{DD} by using the method of Lagrange multipliers (see the Supplementary Material). The optimal value of x is

$$x_{\text{opt}} = \frac{1}{4F} \frac{1}{\sqrt{\text{TMR} + 1}}$$

or

$$4F R_w = \sqrt{R_{\text{MTJ,P}} \cdot R_{\text{MTJ,AP}}} \tag{11}$$

where the last equation shows a V_{DD}-independent relation between the MTJ resistance and the write-path resistance

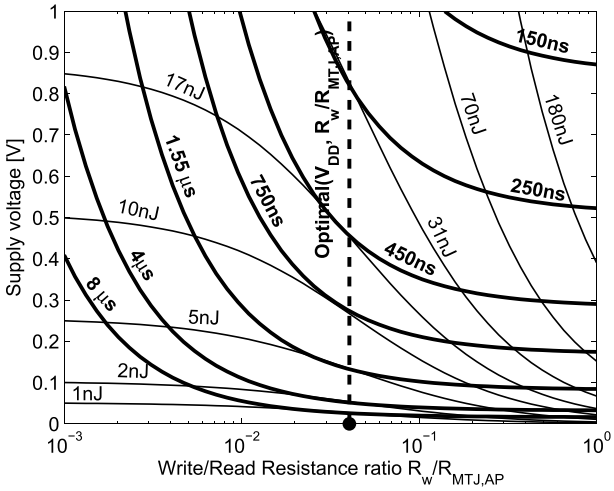

Fig. 4. Constant energy and time delay contour lines for an *mLogic* buffer chain ($L_d = 10$, $F = 4$, and $\alpha_{\text{sw}} = 0.05$). The contour lines are derived from the energy-delay equations (8) and (9). Dashed line: energy-optimal points of (x, V_{DD}). Filled circle at $(x, V_{\text{DD}}) = (0.16, 0)$: global minimum energy point where $E = 0$. The device parameters of *mLogic* are set to those of a fabricated prototype [10]–[12], i.e $L_w = 273$ nm, $A_w = 1\ \mu\text{m} \times 4.3$ nm, $\rho_w = 8.48 \times 10^{-8}\ \Omega \cdot \text{m}$, TMR = 138%, $\mu_{\text{DW}} = 1.81 \times 10^{-11}\ \text{C}^{-1}\text{m}^3$, and $C_w = 5$ fF.

for the minimum energy dissipation. The relation is very similar to the relation between the MTJ resistance and the total series resistance of MOSFETs, R_s, in a 2T-1MTJ STT-Magnetoresistive random-access memory cell for the maximum sense margin ($R_s = (R_{\text{MTJ, P}} \cdot R_{\text{MTJ,AP}})^{1/2}$ [24]). The optimal value of V_{DD} is

$$(V_{\text{DD}})_{\text{opt}} = \frac{4\gamma_c L_d F \mu_{\text{DW}}^{-1} \rho_w L_w^2}{t_d} \cdot \frac{2\sqrt{\text{TMR}+1} + (\text{TMR}+2)}{\text{TMR}}. \tag{12}$$

Fig. 3 shows the energy dissipation of a buffer chain for a fabricated *mLogic* prototype [10]–[12] for constant time delays with varying x or V_{DD}. The x–E (or V_{DD}–E) curve confirms that energy is minimum when $x = x_{\text{opt}}$ [or $V_{\text{DD}} = (V_{\text{DD}})_{\text{opt}}$]. Fig. 4 shows the energy contour lines and the time delay contour lines for the same *mLogic* buffer chain in an x–V_{DD} plane. The energy contour lines and the time delay contour lines meet tangentially at $x = x_{\text{opt}}$, reconfirming the derived expression for x_{opt}. Fig. 4 shows that the global minimum energy is zero if $V_{\text{DD}} = 0$, and so the energy dissipation of a pipelined *mLogic* can be traded off monotonically with delay by scaling the supply voltage V_{DD}. This contrasts the case of MOSFETs whose global minimum energy is nonzero in the $V_{\text{th}} - V_{\text{DD}}$ plane [25] (see Fig. 5). However, an extrinsic pinning effect and thermal noise-induced errors will be shown to set a lower limit for scaling the supply voltage of *mLogic*-based logic pipelines.

The optimal values of x and V_{DD} give the minimum energy dissipation as

$$E_{\text{min}} = \frac{8\alpha_{\text{sw}} \gamma_c^2 L_d^3 F^3 \mu_{\text{DW}}^{-2} \rho_w^2 L_w^4 C_w}{t_d^2} + \frac{2\gamma_c^2 L_d^3 F^2 \mu_{\text{DW}}^{-2} \rho_w L_w^3 A_w}{t_d}$$

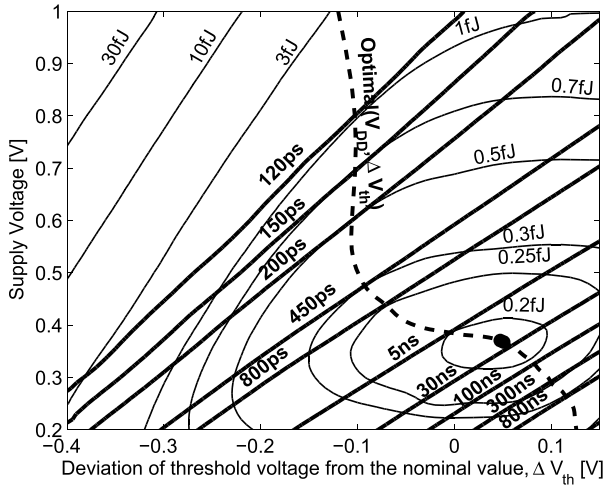

Fig. 5. Constant energy and time delay contour lines for a 32-nm CMOS inverter chain with $L_d = 10$, $F = 4$, and $\alpha_{\rm sw} = 0.05$. The contour lines are obtained from SPICE simulation using a predictive technology model [28]. Dashed line: energy-optimal points of $(\Delta V_{\rm th}, V_{\rm DD})$. Filled circle at $(\Delta V_{\rm th}, V_{\rm DD}) = (0.05\ {\rm V}, 0.37\ {\rm V})$: global minimum energy point where $E = 0.19$ fJ.

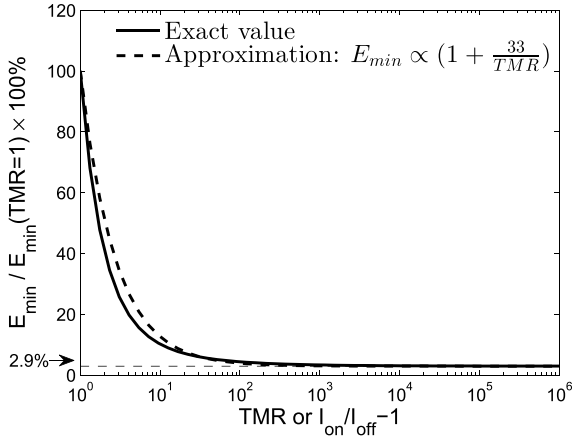

Fig. 6. Energy reduction of an *mLogic* logic pipeline versus the TMR or $I_{\rm ON}/I_{\rm OFF}$ ratio of the *mLogic* device. The graph is plotted using (14). The energy cannot be reduced below 2.9% of the minimum energy for $I_{\rm ON}/I_{\rm OFF} = 2$ (or TMR = 100%).

$$\times \frac{[2\sqrt{\rm TMR+1}+({\rm TMR}+2)]}{({\rm TMR})^2} \times \left[2+\frac{2}{\sqrt{\rm TMR+1}}+\left(1+\frac{2}{\sqrt{\rm TMR+1}}\right){\rm TMR}\right] \quad (13)$$

where the first term represents the dynamic energy and the second term represents the resistive energy. Since the resistive energy is $10^3\times$ larger than the dynamic energy, the minimum energy $E_{\rm min}$ scales with the TMR approximately as

$$\frac{E_{\rm min}({\rm TMR})}{E_{\rm min}({\rm TMR}=1)} \simeq \frac{1}{34}\left(1+\frac{33}{\rm TMR}\right). \quad (14)$$

In the ideal case of the $I_{\rm ON}/I_{\rm OFF}$ ratio or for TMR $= \infty$, $E_{\rm min}({\rm TMR} = \infty)/E_{\rm min}({\rm TMR} = 1) = 0.029$. So, the energy dissipation cannot be reduced below 2.9% of the minimum energy for TMR $= 1$ by maximizing the TMR (see Fig. 6). This saturation of energy reduction can be explained as follows: *mLogic* gates have to inject a certain minimum amount of charge through the write path of the next stage *mLogic* to drive the DW motion. At a certain point in increasing the TMR, the antiparallel resistance of the MTJ becomes much larger than the write-path resistance of the next stage *mLogic*, and so the current through the antiparallel resistance of the MTJ becomes negligible compared with that in the write path of the next stage *mLogic*. Beyond this point, the resistive energy of the *mLogic* gate remains almost constant regardless of how further we increase the TMR and completely depends on the required write-path current to achieve a certain delay constraint. In addition, this saturation begins at a rather small value of the TMR. For TMR $= 10$, the energy reduction is already a factor of $E_{\rm min}({\rm TMR} = 10)/E_{\rm min}({\rm TMR} = 1) = 0.10$, which implies that we cannot expect orders of magnitude energy reduction by increasing the TMR much beyond 10. Considering that an MTJ with TMR $= 6$ has been already demonstrated with CoFeB/MgO/CoFeB [27], any further effort to increase the TMR will not benefit anymore in terms of the energy efficiency of *mLogic* for pipelined logic applications. However, maximizing the TMR will be shown to still benefit in other ways such as mitigating the noise limit of scaling the supply voltage of *mLogic*-based logic pipelines.

TABLE II
MATERIAL REQUIREMENTS FOR HIGH DW MOBILITY $\mu_{\rm DW}$

symbol	name	requirement
α	Gilbert damping factor	close to one
β	Degree of non-adiabatic STT	as large as possible
P	Degree of spin polarization	as large as possible
θ_{SH}	Spin Hall angle	as large as possble
M_s	Saturation magnetization	as small as possible
t_F	Write path ferromagnet thickness	as small as possible
Δ	Domain wall width	as large as possible

V. IMPLICATIONS

Figs. 3 and 4 show that the fabricated *mLogic* prototype [10]–[12] has both poor performance and low energy efficiency (5-nJ dissipation at 1.55-μs delay) even after optimization of x and $V_{\rm DD}$. So, further optimization of other device parameters should be considered. The physical body of *mLogic* is essentially a metallic wire, which is traversed by four other wires. Therefore, the lateral dimensions of *mLogic* are constrained by the minimum wire pitch/width. The minimum write-path length L_w is three wire pitches, 6λ, and the minimum write-path width is the minimum wire width, 2λ, where λ is the minimum feature size for a given fabrication technology [26]. In addition, the TMR of the CoFeB/MgO/CoFeB MTJ junction can be as high as TMR $= 600\%$ [27]. The equation for the DW mobility (1) provides an optimal guideline when choosing magnetic materials for an *mLogic* device. To maximize $\mu_{\rm DW}$, the magnetic properties of the write path should be optimized according to the rules in Table II. The magnetic properties of the fabricated prototype [10]–[12] are not optimized according to Table II, and so the DW mobility of the fabricated prototype is much smaller than a theoretically achievable value. If one chose the

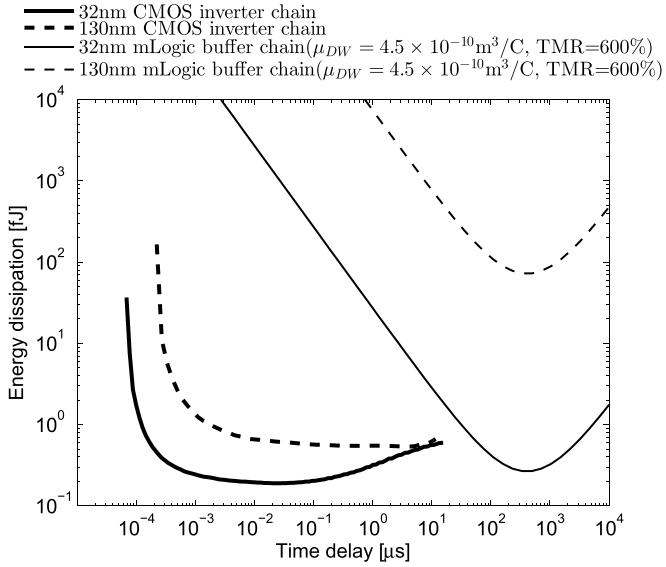

Fig. 7. Comparison between a CMOS inverter chain and an *mLogic* buffer chain for 32- and 130-nm technologies. For both the buffer/inverter chains, $L_d = 10$, $F = 4$, and $\alpha_{\rm sw} = 0.05$. The Pareto-optimal curve for the CMOS inverter chain is extracted from SPICE simulation using a predictive technology model [28]. The supply voltage of the *mLogic* graphs ranges from $O(0.1\ \mu\text{V})$ to $O(10\ \text{V})$, while that of the CMOS graphs ranges from 0.2 to 1 V.

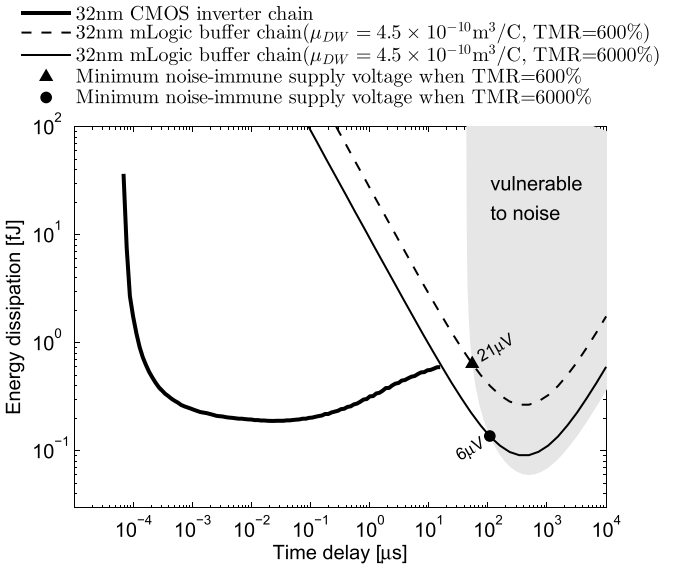

Fig. 8. Comparison between a 32-nm CMOS inverter chain and a 32-nm *mLogic* buffer chain ($L_d = 10$, $F = 4$, and $\alpha_{\rm sw} = 0.05$). The Pareto-optimal curve for the CMOS inverter chain is extracted from SPICE simulation using a predictive technology model [28]. Shaded region: region where the circuit error probability p is larger than 3×10^{-20} with varying TMR from 0.2 to 10^6 and a fixed $\mu_{\rm DW}$. Note that all the regions in the CMOS graph are noise-free as the supply voltage for CMOS is not smaller than 0.2 V, which is larger than the minimum noise-immune supply voltage for CMOS: $\sim\sqrt{kT/C} \sim O(10\ \text{mV})$.

magnetic materials, such that $\alpha = 0.1$, $P = 1$, $\theta_{\rm SH} = 0.4$, $M_s = 0.4$ MA/m, $\Delta = 20$ nm, and $t_F = 1$ nm, then the DW mobility would be $\mu_{\rm DW} = 5 \times 10^{-10}$ m^3/C, which is close to the value extracted from a micromagnetics simulation in [9]: $\mu_{\rm DW} = 4.5 \times 10^{-10}$ m^3/C. We will use this value to project the DW mobility of a future *mLogic* device.

Two extrinsic pinning phenomena are reported in this paper of the fabricated *mLogic* prototype [10]–[12]. First, the stray magnetic field from the reference layer of the MTJ in the read path pins the read-path DW. But, this stray magnetic field can be either reduced or removed by redesigning the device structure. The energy barrier for the prevention of erroneous free motion of DW pins the write-path DW. This pinning effect cannot be removed as the energy barrier is introduced intentionally. The magnitude of the effective pinning field for the both pinning effects is $H_p = 50$ Oe for a 1-μm-wide device [10]–[12]. Since the DW energy is linearly proportional to the DW cross-sectional area, the effective pinning field for the energy barrier varies as $H_p = 50\ \text{Oe} \times 2\lambda/(1\ \mu\text{m})$ for different technology nodes. Since a micromagnetics simulation [9] gives the critical write current density for depinning an effective pinning field of 10 000 Oe to be 1.5 MA/cm^2, the critical write current density for depinning an effective pinning field of $H_p = 50\ \text{Oe} \times 2\lambda/(1\ \mu\text{m})$ is $J_w^{\rm cr} = 15\ \text{kA/cm}^2 \times (\lambda/1\ \mu\text{m})$. Because of the nonzero critical-depinning current density $J_w^{\rm cr}$, the minimum energy (13) should be modified as

$$E_{\min} \simeq 2\gamma_c^2 L_d^3 F^2 \mu_{\rm DW}^{-2} \rho_w L_w^3 A_w \times t_d \left(\frac{1}{t_d} + \frac{\mu_{\rm DW} J_w^{\rm cr}}{\gamma_c L_d L_w}\right)^2 \left(1 + \frac{33}{\text{TMR}}\right). \quad (15)$$

If the write-path current density J_w is reduced below the twice of the critical current density $2J_w^{\rm cr}$, then the time delay t_d becomes longer than $\gamma_c L_d L_w/\mu_{\rm DW} J_w^{\rm cr}$, and the minimum energy dissipation $E_{\min}$ starts to increase with t_d (see Figs. 7 and 8). This is because as J_w approaches $J_w^{\rm cr}$, the reduction of the resistive power is saturated, while the time delay increases hyperbolically, i.e., $P_R(J_w) \geq P_R(J_w^{\rm cr})$ and

$$t_d = \gamma_c L_d \frac{L_w}{|dq_2/dt|} = \gamma_c L_d \frac{L_w}{\mu_{\rm DW} |J_w - J_w^{\rm cr}|}. \quad (16)$$

Because of the pinning effect, the fan-out F has an upper limit. As the write current (or the output current of an *mLogic* gate) decreases with the fan-out, one cannot increase the fan-out further, when the write current density is right above the critical-depinning current density, $J_w^{\rm cr}$. For a given supply voltage, the maximum allowed fan-out can be written as

$$F_{\max} = \frac{V_{\rm DD}}{4 J_w^{\rm cr} \rho_w L_w} \frac{\text{TMR}}{2\sqrt{\text{TMR} + 1} + (\text{TMR} + 2)}. \quad (17)$$

The maximum allowed fan-out saturates to $V_{\rm DD}/4 J_w^{\rm cr} \rho_w L_w$ as $\text{TMR} \to \infty$. And even if TMR = 100, the maximum fan-out is already 82% of that saturation value. So, we do not need to maximize the TMR aggressively to push up the upper limit of the fan-out.

Besides the pinning effect, the thermal noise in the resistors of an *mLogic* device also limits the scaling of the supply voltage. Since *mLogic* will operate in sub-100-mV voltages [9], an information bit at circuit nodes can be potentially flipped by the thermal fluctuation causing circuit errors. For IoT applications, electronic devices are expected to operate without error for at least one year, and the *mLogic* pipeline is best to operate at clock frequency below 1 MHz. So, a circuit with 10^6 *mLogic* gates should have error probability at each node less than $p = 3 \times 10^{-20}$ per switching. For a given

allowed error probability of circuit error, p, the minimum allowed supply voltage of a logic pipeline of *mLogic* is given by (see the Supplementary Material)

$$(V_{\mathrm{DD}})_{\mathrm{noise-immune}} \geq [\mathrm{erfc}^{-1}(2p)]^2 \cdot \frac{8\ kT\mu_{\mathrm{DW}}}{L_w A_w \cdot xF \cdot \mathrm{TMR}} \tag{18}$$

which is inversely proportional to the TMR. So, maximizing the TMR can decrease the minimum noise-immune supply voltage of a logic pipeline of *mLogic*.

Fig. 7 shows the Pareto-optimal curves for a logic pipeline of *mLogic* and CMOS for the 32- and 130-nm technologies. The 32-nm E–D curve of *mLogic* is much closer to the 32-nm E–D curve of CMOS than the 130-nm E–D curve of *mLogic* is to the 130-nm E–D curve of CMOS. This is because the minimum energy dissipation of *mLogic* for fixed time delays scales as $\sim\lambda^4$, while that of CMOS scales as $\sim\lambda$ or λ^2, where λ is the minimum feature size. So, scaling the device size of *mLogic* will increase the size of the window where *mLogic* is more energy efficient than MOSFETs.

Fig. 8 compares a logic pipeline of *mLogic* and that of CMOS for the 32-nm technology with consideration of the thermal noise-induced errors. For TMR = 600%, the *mLogic* pipeline with a supply voltage less than 20 μV dissipates less energy than the CMOS pipeline does. But, the minimum noise-free supply voltage is 21 μV for the 32-nm *mLogic* pipeline. So, for TMR = 600%, the *mLogic* pipeline cannot win over the CMOS pipeline without any error-correction circuits. However, if the TMR is increased by a factor of 10, the minimum noise-free supply voltage will decrease down to 6 μV. The 32-nm *mLogic* pipeline with a supply voltage between 0.4 mV and 6 μV will be both noise-free and more energy efficient than the CMOS pipeline. Therefore, moderately maximizing the TMR increases the size of the window where the *mLogic* pipeline is both noise-immune and more energy efficient than MOSFETs.

VI. Conclusion

This paper models and optimizes the energy performance of a logic pipeline of one of the most mature spintronic MTJ logic devices called *mLogic* [8]–[12]. An equation for the DW mobility is derived to predict the performance of a fabricated prototype of *mLogic* [10]–[12] and provides a guideline for the optimization of the magnetic properties of future designs of *mLogic*. The optimization of an *mLogic* pipeline gives a relation between the MTJ resistance and the write-path resistance: $4FR_w = (R_{\mathrm{MTJ,P}} \cdot R_{\mathrm{MTJ,AP}})^{1/2}$. Maximizing the TMR will not reduce the energy dissipation significantly for TMR $>$ 100. The minimum energy dissipation of an *mLogic* pipeline monotonically decreases with an increase in delay by supply voltage scaling, but is limited by thermal noise and an extrinsic pinning effect. Increasing the TMR to $\sim$100 can reduce the lower limit of the supply voltage by mitigating the thermal noise and leaving the extrinsic pinning as the limiting mechanism to further energy scaling. A 32-nm logic pipeline of a projected future *mLogic* device can be more energy efficient than the CMOS technology for a clock frequency between 100 and 10 kHz. This clock frequency range is usually used by ultralow-power applications in the IoT [6], [7]. Therefore, the *mLogic* has a potential to replace MOSFETs in low-performance and low-power applications, such as the IoT. Since the cost is also an important constraint for IoT applications, one would need to evaluate the cost of *mLogic*, when available in the future, to assess the complete potential of *mLogic* for the IoT market. This paper also identified that the energy of the *mLogic* quadratically depends on the DW mobility, which is, hence, one of the most sensitive design knobs, and could lead to even more promising device designs.

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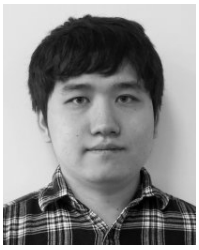

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