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2D-2D tunneling field-effect transistors using WSe_2/$SnSe_2$ heterostructures

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Two-dimensional materials present a versatile platform for developing steep transistors due to their uniform thickness and sharp band edges. We demonstrate 2D-2D tunneling in a WSe_2/$SnSe_2$ van der Waals vertical heterojunction device, where WSe_2 is used as the gate controlled *p*-layer and $SnSe_2$ is the degenerately *n*-type layer. The van der Waals gap facilitates the regulation of band alignment at the heterojunction, without the necessity of a tunneling barrier. ZrO_2 is used as the gate dielectric, allowing the scaling of gate oxide to improve device subthreshold swing. Efficient gate control and clean interfaces yield a subthreshold swing of ~100 mV/dec for >2 decades of drain current at room temperature, hitherto unobserved in 2D-2D tunneling devices. The subthreshold swing is independent of temperature, which is a clear signature of band-to-band tunneling at the heterojunction. A maximum switching ratio I_{ON}/I_{OFF} of 10^7 is obtained. Negative differential resistance in the forward bias characteristics is observed at 77 K. This work bodes well for the possibilities of two-dimensional materials for the realization of energy-efficient future-generation electronics. © *2016 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4942647]

Scaling the size of transistors has resulted in improved speed, functionality, density, and affordability of microprocessors. However, a monumental increase in power consumption is concomitant with these advancements. The minimum supply voltage of the metal oxide semiconductor field-effect transistors (MOSFET) is governed by the carrier injection mechanism of thermionic emission over the energy barrier at the source. Thus, the Boltzmann limit of 60 mV/dec severely impedes the scaling of supply voltage, in order to obtain a satisfactory I_{ON} and I_{ON}/I_{OFF}. Tunneling across the energy barrier at the source opens the prospects of reduced supply voltage, since a pure band-to-band tunneling (BTBT) process is not thermally activated. The use of conventional three-dimensional semiconductors in tunnel FETs (TFETs) has shown promise. Reports of sub-60 mV/decade subthreshold swing (SS) have been made in silicon, germanium, and III-V-based TFETs.[1–10] However, an SS less than 60 mV/dec at room temperature, over several orders of magnitude of drain current, has not been frequently observed.[11] The main reason for the difficulty in obtaining sharp switching along with a high I_{ON}/I_{OFF} is due to the presence of band-tail states in conventional semiconductors.[12] The tunnel current modulation in most cases is due to the effect of modulation of the tunneling barrier width by the gate field, as opposed to the modulation of available energy density of states. Here, two-dimensional materials come to the forefront with their interesting electronic and optoelectronic properties, including sharp band edges even at a thickness of a monolayer. The optical band edge sharpness of a monolayer WSe_2–monolayer MoS_2 heterojunction is experimentally found to be ~30 meV/decade, despite atomic imperfections and introduction of fabrication-induced impurities.[13] This value is close to that of a perfect crystal of bulk Si, which has a band-edge sharpness of 23 meV/dec.[14] The introduction of dopants, thickness scaling, and heterojunctions would further smear the band-edge and introduce band-tail states in conventional semiconductors. Moreover, incorporating the two-dimensional materials to a device structure that can eliminate doping by using electrostatic gating is advantageous to the preservation of the band edge sharpness. Thus, 2D-2D heterojunctions can theoretically provide switching by turning off the energy density of states using the gate fields.

There have been several reports of tunneling in layered materials. For example, resonant tunneling was previously reported in graphene-insulator-graphene structures.[15] However, the absence of bandgap in graphene prevents the realization of a tunnel transistor with high I_{ON}/I_{OFF}. We reported the direct observation of gate-controlled band-to-band tunneling in transition metal dichalcogenide-based heterostructure devices. Gate controlled BTBT and negative differential resistance (NDR) were observed at 77 K, and the NDR peak height and position could be tuned by the gate voltage.[16] Tunneling and NDR in epitaxially grown WSe_2/MoS_2 heterostructures were shown using conductive atomic force microscopy.[17] Black phosphorus/$SnSe_2$ heterojunctions showed band-to-band tunneling induced NDR at room temperature, using a two-terminal device structure without a gate.[18] Very recently, a steep transistor was realized with polymer electrolyte gating of a p+ Ge/MoS_2 3D-2D van der Waals heterojunction.[11] Bulk Ge, with its 3D density of states, is the p-side of the tunneling junction. The n-side is an atomically thin MoS_2 layer, which has 2D density of states. This device shows a subthreshold swing of sub-60 mV/dec over several decades of drain current at low current levels. However, a steep switch taking advantage of 2D-2D tunneling, where both n and p-sides are realized with 2D layered materials, has not been realized yet.

In our previous report on BTBT of a MoS_2/WSe_2 heterostructure, a large electric field across the heterojunction was

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required to form a type III (broken gap) alignment from the initial type II alignment of the heterostack at equilibrium. The necessity for high fields for the inception of BTBT limited the performance of these devices as steep switches.[16] In this paper, we report a vertical heterojunction tunnel FET with WSe_2 as the *p*-layer and $SnSe_2$ as the degenerate *n*-layer, which has been theoretically predicted to be close to a type III alignment at equilibrium.[19–21] Due to degeneracy of $SnSe_2$, a single gate is sufficient to control the band alignment of WSe_2 and $SnSe_2$ from type II to type III. In the tunnel FET fabricated, an SS of $\sim$100 mV/decade is observed at room temperature for >2 decades, with a minimum SS of 100 mV/dec. The SS is independent of temperature, confirming that the current is due to direct BTBT. NDR is observed at forward bias at 77 K and diminishes with increasing temperature. While maintaining the quality of the gate oxide/WSe_2 interface and $WSe_2/SnSe_2$ interface the same across all devices, the use of high-κ ZrO_2 as the gate dielectric facilitates gate oxide scaling and allows the reduction of SS.

The process flow for fabrication of $WSe_2/SnSe_2$ tunnel FETs is shown in Fig. S1.[22] Heterostacks of $SnSe_2$ on WSe_2 were made by dry transfer method.[23] The $WSe_2/SnSe_2$ heterostacks were then dry transferred onto fabricated local bottom gates. Source/drain contacts to $SnSe_2$ and WSe_2 were then deposited. Electrical measurements on the heterostructure device were performed by holding the potential at the source ($SnSe_2$ side) at 0 V. The potential applied at the WSe_2 contact is considered the drain voltage, V_D. The gate voltage applied on the bottom gate (V_G) modulates the band offset, hence the tunneling current across the $SnSe_2/WSe_2$ heterojunction. For all measurements, the Si/SiO_2 substrate was kept at ground potential. Measurements reported in this paper were all performed in vacuum at 10^{-5} Torr.

Before delving into the electrical behavior of $WSe_2/SnSe_2$ heterojunctions, we study the band alignment of WSe_2 and $SnSe_2$. Bulk $SnSe_2$ has a bandgap of 1.1 eV.[24] Monolayer and bulk WSe_2 have bandgaps of 1.6 eV and 1.2 eV, respectively.[25] The 3–6 layers of WSe_2 used in our experiments have a bandgap close to 1.6 eV. In order to obtain the band alignment of WSe_2 and $SnSe_2$, X-ray photoelectron spectroscopy was performed on the bulk $SnSe_2$ and WSe_2 samples. Figure 1(a) shows secondary electron cut-offs of the photoelectron spectra. The workfunction of the materials can be extracted by plotting the kinetic energy from the Al Kα X-ray excitation energy of 1486.7 eV (the spectra are corrected for an externally applied bias of -9.87 V on the sample, which accelerates photoelectrons away from the sample into the detector) and extrapolating the linear part of the cutoff to zero intensity. The workfunction for the Au reference is 5.1 eV, which agrees well with values found in literature. The workfunction $\Phi = (E_{vac} - E_F)/q$ (E_{vac} is the vacuum level; E_F is the Fermi level) of $SnSe_2$ is extracted to be 4.6 eV, and the workfunction of WSe_2 is 3.7 eV. The valence band spectra of the WSe_2 and $SnSe_2$ are shown in Figure 1(b). The Fermi level is represented by the binding energy of 0 eV. Again, by extrapolation of the linear part of the decaying tail of the valence band to zero intensity, the valence band energy can be obtained with respect to the Fermi level. For $SnSe_2$, E_F-E_V is obtained to be 1.0 eV, and that for WSe_2 is 1.1 eV, where E_V is the valence band edge. From the E_F-E_V and $q\Phi = E_{vac}$-E_F extracted from the XPS spectra, along with the bandgaps of bulk $SnSe_2$ and WSe_2 reported in literature, we can obtain the band alignment of WSe_2 and $SnSe_2$. WSe_2 and $SnSe_2$ form a nearly type III or broken gap alignment, with a conduction band offset of 1.2 eV and a valence band offset of 0.8 eV. This implies that efficient carrier tunneling can be obtained by applying moderate gate voltages.

$SnSe_2$ is an n-type layered semiconductor, whose electrical properties as a two dimensional layered system have not been widely explored yet.[26] Figure S2(a) shows the transfer characteristics of an $SnSe_2$ flake of thickness $\sim$2 nm with 8 nm ZrO_2 back gate and Pd contacts, at temperatures ranging from 77 K to 300 K. As-received $SnSe_2$ is degenerately n-doped with the drain current showing little gate control at room temperature. At 77 K, the device still shows degenerate behavior, with the drain current modulation being within an order of magnitude for the entire gate bias range. The output characteristics of the same device at 100 K and 300 K are shown in Fig. S2(b). The resistance of the Pd contacts on $SnSe_2$ can be estimated to be $\sim$3.8 kΩ, using a model described in the supplementary material S2.[22] The carrier concentration at $V_G = 0$ V can be estimated by $n = \sigma/q\mu = (I/V)|_{(VD\ =\ 0.05\ V)} \times (1/q\mu)$, where n is the sheet carrier concentration, σ is the conductivity, q is the charge of an electron, and μ is the mobility. The mobility extraction is also shown in the supplementary material S2.[22] The sheet carrier concentration of $SnSe_2$ is calculated to be $\sim 10^{13}$ cm^{-2}. Figure S3(a)–S3(b) shows the X-ray photoelectron spectra of the Se*3d* and Sn*3d* core levels of as-exfoliated bulk $SnSe_2$.[22] The presence of oxygen impurities bonded to Se indicates the presence of a large number of defects in the $SnSe_2$ crystal. Defects in $SnSe_2$ contribute to the n-type degeneracy of the material. The transfer characteristics of few-layer WSe_2 are shown in Fig. S4.[22] WSe_2 shows ambipolar behavior with Pd contacts.

In our previous report on BTBT in MoS_2/WSe_2 heterostructures, we used dual gates, with one gate controlling the carrier concentration and chemical potential of the WSe_2 layers and the other gate controlling the MoS_2 layers, to regulate the band alignment of the heterojunction from type II to type III.[16] Because of the n-type degeneracy of $SnSe_2$ at all temperatures, the gating of $SnSe_2$ to control the carrier concentration and potential of $SnSe_2$ in the $WSe_2/SnSe_2$ heterojunction is unnecessary. A single-gated heterojunction simplifies the fabrication process for the tunnel device. The bottom gate is used to modulate the potential of WSe_2 and hence controls the band alignment of the $WSe_2/SnSe_2$ heterostructure. Since the WSe_2 layer is between 3 and 6 layers, the electrostatic potential of the entire flake is well controlled by the bottom gate. The gate field can affect the $SnSe_2$ layers close to the interface. However, since $SnSe_2$ is degenerately n-type, the band alignment of $SnSe_2$ at the interface would be relatively unaffected by the gate fields. Also, an interfacial tunnel barrier is not required for modulation of the band alignment. The van der Waals gap prevents the Fermi level pinning at the hetero-interface.[16] It is worth noting that the redundancy of a physical tunnel barrier at the hetero-interface of a van der Waals heterostructure is a major advantage over that in a covalently bonded heterostructure where the Fermi level gets pinned at

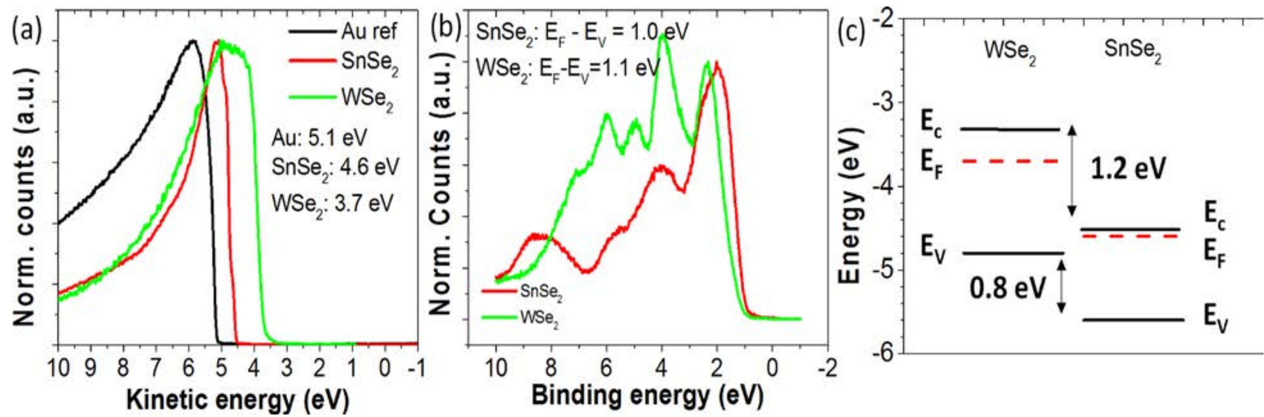

FIG. 1. Energy band alignment of $WSe_2/SnSe_2$. (a) Secondary electron cutoffs of the X-ray photoelectron spectra of $SnSe_2$ and WSe_2, with the kinetic energy corrected for the applied bias. (b) Valence band spectra of WSe_2 and $SnSe_2$ from XPS. (c) Energy band alignment of WSe_2 and $SnSe_2$.

the interface and requires a barrier layer to allow the band alignment modulation.[27]

Figures 2(a)–2(b) show the gated $WSe_2/SnSe_2$ heterojunction device structure and optical image of a representative device. Figures 2(c)–2(e) show the electrical characteristics of the $WSe_2/SnSe_2$ heterojunction tunnel FET. The bottom gate consists of $\sim$8 nm thick ZrO_2 as the gate dielectric, and the heterojunction area is $\sim 100\,\mu m^2$. At the extreme negative gate voltage, WSe_2 is accumulated with holes, while $SnSe_2$ is still accumulated with electrons, and the heterojunction is at type III alignment. The I_D-V_G at $V_D = -1$ V shows the gate-controlled tunnel current, with an I_{ON}/I_{OFF} of $>10^3$ (Fig. 2(c)), and a minimum SS of 100 mV/decade at room temperature (Fig. 2(d)). The tunneling current reduces as V_G approaches less negative voltages, and the heterojunction alignment goes towards type II from type III turning the tunnel junction OFF. At $V_G \sim -1.45$ V, the current due to tunneling subsides. The current observed at $V_G > -1.45$ V is due to the electron current across the n-WSe_2-$SnSe_2$ heterojunction. The SS for the p-tunnel FET thus obtained is $\sim$100 mV/dec for $>$2 orders of magnitude of drain current. The I_D-V_D with varying gate voltage at room temperature shows an inflection close to $V_D = 0$ V, indicating the presence of a Schottky barrier at the WSe_2 contact (Fig. 2(e)). Figure S5 shows the performance of another $WSe_2/SnSe_2$ heterojunction device fabricated on a 20 nm thick ZrO_2 gate, with a heterojunction area of $\sim 140\,\mu m^2$. The I_{ON}/I_{OFF} is $\sim 10^7$, with an ON current of $\sim 4\,\mu$A, leading to a current density of ~ 30 nA/μm^2. Due to a thicker gate dielectric, the SS of this device is $<$200 mV/dec for $\sim$4 decades of drain current, while the minimum SS is 164 mV/dec at room temperature. The SS is strongly dependent on the effective oxide thickness (EOT) of the gate dielectric.

In order to confirm that the current observed across the heterojunction is due to BTBT, we performed temperature dependent measurements of the I_D-V_G. The results are shown

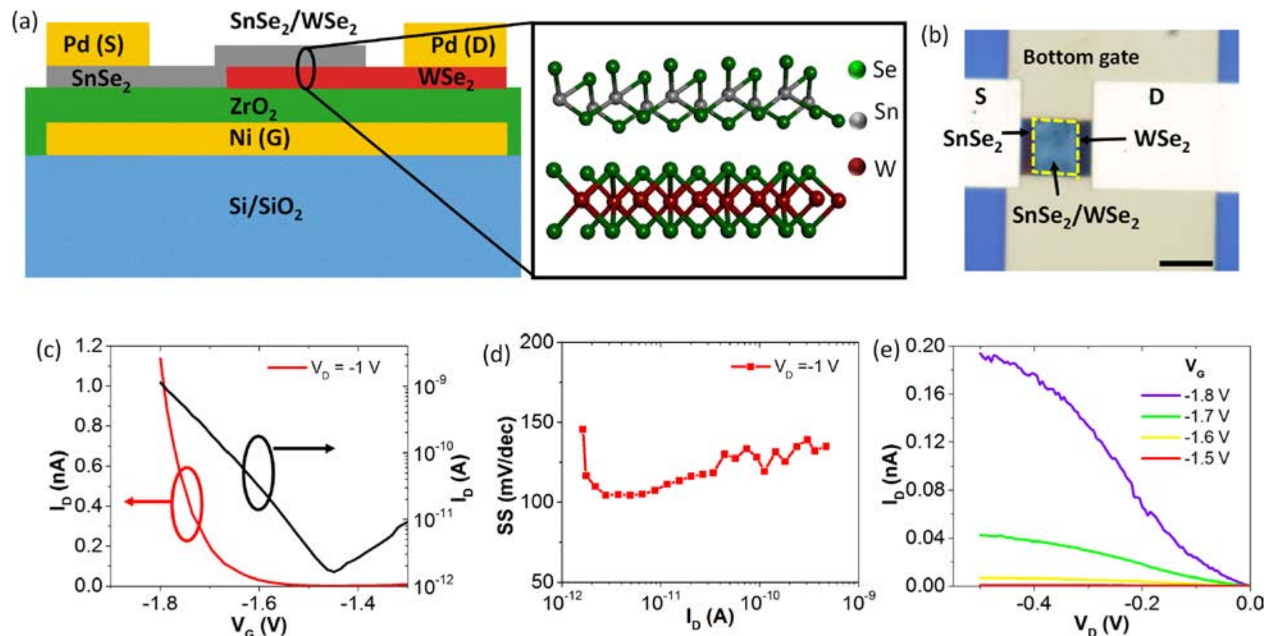

FIG. 2. Device structure and characteristics of $WSe_2/SnSe_2$ heterojunction TFET at room temperature (295 K), in vacuum. (a) Cross-section of device (not to scale). (b) Optical image of a representative device (scale bar 5 μm). (c) I_D-V_G at $V_D = -1$ V. The red curve corresponds to linear scale, and the black curve corresponds to log scale. (d) Subthreshold swing *vs.* I_D. (e) I_D-V_D for varying gate voltages. (Note: The inconsistency in the current levels of I_D-V_G and I_D-V_D is due to hysteresis in the measurement.)

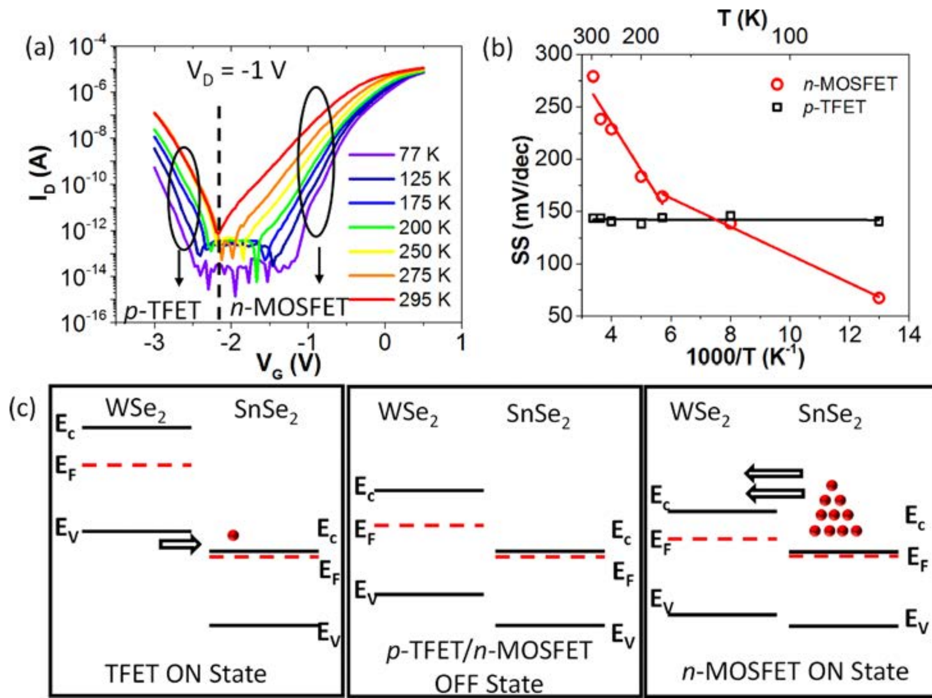

FIG. 3. Temperature dependence of current in $WSe_2/SnSe_2$ heterojunction TFET. (a) I_D-V_G at temperatures varying from 77 K to 295 K. (b) SS as a function of 1000/*T* for *p*-TFET and *n*-MOSFET operations in the $WSe_2/SnSe_2$ heterojunction device. (c) Qualitative band diagrams for three conditions: *p*-TFET ON, *p*-TFET and *n*-MOSFET OFF, and *n*-MOSFET ON states.

in Fig. 3(a), using a device different from the one in Fig. 2. The current at large negative gate voltages (*p*-branch) is due to tunneling, and the slope of the I_D-V_G curve does not vary with temperature. The tunneling threshold voltage of the *p*-TFET shifts positively owing to the change in Schottky barrier at the WSe_2/Pd contacts. On the other hand, the slope of the I_D-V_G for the *n*-MOSFET, which operates in the higher V_G range, is strongly dependent on temperature. Figure 3(b) shows the weak dependence of SS on temperature for the *p*-TFET, and a linear variation of subthreshold slope with temperature for the *n*-MOSFET. The SS of the *n*-MOSFET as a function of 1000/T can be fitted with two different linear curves – one for temperature range 77 K to 175 K and the other for the range between 175 K and 295 K. First, the subthreshold slope of the *n*-MOSFET is much larger than 60 mV/dec at room temperature, possibly due to the presence of traps at the interface between WSe_2 and the back gate and at the $WSe_2/SnSe_2$ interface. The SS of the MOSFET at 77 K is ~67 mV/dec, while that of the *p*-TFET is ~140 mV/dec. The invariance of SS with temperature for I_D corresponding to $V_G < -2.2$ V confirms the tunnel FET operation of the $WSe_2/SnSe_2$ heterostructure device for this gate voltage range. Figure 3(c) shows qualitative energy band diagrams of WSe_2 and $SnSe_2$ under three different conditions: when TFET is ON, when both *p*-TFET and *n*-MOSFET are OFF and when *n*-MOSFET is ON. The type III (broken) band alignment when V_G is highly negative allows tunneling of carriers from valence band of WSe_2 to conduction band of $SnSe_2$. The tunneling is reduced as V_G is made less negative, and stops when the $WSe_2/SnSe_2$ band alignment goes to type II. However, in this situation, the barrier between $SnSe_2$ and WSe_2 conduction bands is still large to impede thermionic emission over the barrier. The *n*-MOSFET operation commences when the barrier at the conduction bands is reduced enough to allow thermionic emission.

Tunnel FETs show NDR in forward bias I_D-V_D for gate voltages corresponding to the Esaki diode operation regime. We observe NDR at 77 K in a $WSe_2/SnSe_2$ heterostructure device, as shown in Fig. 4. The tunnel current at 0 V is low, leading to nonlinearity in I_D-V_D. This indicates that the contact resistance in the device is high. The NDR peak-to-valley ratio diminishes with increasing temperature. At 150 K, the drain current flattens out, and NDR can no longer be observed, leaving only a trend towards NDR. The diminishing peak-to-valley ratio of NDR with increasing temperature, and the absence of NDR at room temperature are indicative of an interlayer recombination process that competes with the tunneling process in forward bias.[16,28]

In conclusion, we demonstrate 2D-2D tunneling in a layered materials heterojunction. A close to type III band alignment of WSe_2 and $SnSe_2$ allows the operation of a tunnel FET, with significant I_{ON}/I_{OFF} and steep SS at room temperature. A minimum SS of 100 mV/dec is observed at room temperature. The SS does not vary significantly with temperature, confirming that the current observed is due to band-to-band tunneling at the hetero-interface. NDR observed at

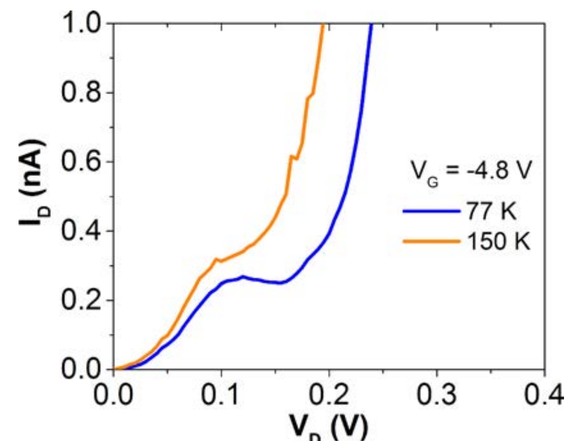

FIG. 4. Negative differential resistance in forward bias I_D-V_D of $WSe_2/SnSe_2$ heterojunction *p*-TFET at low temperatures.

forward bias at low temperatures further serves as evidence towards BTBT. Moving forward, in order to see limits of the device performance in terms of steeper SS and higher on current, improvement of the contacts and improvement of the heterojunction interface quality are critical. For this purpose, doping of the contact regions is essential to achieve the expected performance of the TFETs based on 2D materials. Moreover, material quality in terms of defects, traps, and surface contaminants determines the interface properties. Therefore, the device performance also depends on the quality of the starting material. This work represents an important step towards the realization of steep devices with using 2D-2D heterojunctions.

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