2D-2D tunneling field-effect transistors using WSe$_2$/SnSe$_2$ heterostructures

Cite as: Appl. Phys. Lett. 108, 083111 (2016); https://doi.org/10.1063/1.4942647
Submitted: 01 December 2015 . Accepted: 10 February 2016 . Published Online: 24 February 2016

Tania Roy, Mahmut Tosun, Mark Hettick, Geun Ho Ahn, Chenming Hu, and Ali Javey

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Two-dimensional materials present a versatile platform for developing steep transistors due to their uniform thickness and sharp band edges. We demonstrate 2D-2D tunneling in a WSe₂/SnSe₂ van der Waals vertical heterojunction device, where WSe₂ is used as the gate controlled p-layer and SnSe₂ is the degenerately n-type layer. The van der Waals gap facilitates the regulation of band alignment at the heterojunction, without the necessity of a tunneling barrier. ZrO₂ is used as the gate dielectric, allowing the scaling of gate oxide to improve device subthreshold swing. Efficient gate control and clean interfaces yield a subthreshold swing of \( \sim 100 \text{mV/dec} \) for \( >2 \) decades of drain current at room temperature, hitherto unobserved in 2D-2D tunneling devices. The subthreshold swing is independent of temperature, which is a clear signature of band-to-band tunneling at the heterojunction. A maximum switching ratio \( I_{ON}/I_{OFF} \) of \( 10^7 \) is obtained. Negative differential resistance in the forward bias characteristics is observed at 77 K. This work bodes well for the possibilities of two-dimensional materials for the realization of energy-efficient future-generation electronics.

Scaling the size of transistors has resulted in improved speed, functionality, density, and affordability of microprocessors. However, a monumental increase in power consumption is concomitant with these advancements. The minimum supply voltage of the metal oxide semiconductor field-effect transistors (MOSFET) is governed by the carrier injection mechanism of thermionic emission over the energy barrier at the source. Thus, the Boltzmann limit of 60 mV/dec severely impedes the scaling of supply voltage, in order to obtain a satisfactory \( I_{ON} \) and \( I_{ON}/I_{OFF} \). Tunneling across the energy barrier at the source opens the prospects of reduced supply voltage, since a pure band-to-band tunneling (BTBT) process is not thermally activated. The use of conventional three-dimensional semiconductors in tunnel FETs (TFETs) has shown promise. Reports of sub-60 mV/decade subthreshold swing (SS) have been made in silicon, germanium, and III-V-based TFETs. However, an SS less than 60 mV/dec at room temperature, over several orders of magnitude of drain current, has not been frequently observed. The main reason for the difficulty in obtaining sharp switching along with a high \( I_{ON}/I_{OFF} \) is due to the presence of band-tail states in conventional semiconductors. The tunnel current modulation in most cases is due to the effect of modulation of the tunneling barrier width by the gate field, as opposed to the modulation of available energy density of states. Here, two-dimensional materials come to the forefront with their interesting electronic and optoelectronic properties, including sharp band edges even at a thickness of a monolayer. The optical band edge sharpness of a monolayer WSe₂–monolayer MoS₂ heterojunction is experimentally found to be \( \sim 30 \text{meV/dec} \), despite atomic imperfections and introduction of fabrication-induced impurities. This value is close to that of a perfect crystal of bulk Si, which has a band-edge sharpness of 23 meV/dec. The introduction of dopants, thickness scaling, and heterojunctions would further smear the band-edge and introduce band-tail states in conventional semiconductors. Moreover, incorporating the two-dimensional materials to a device structure that can eliminate doping by using electrostatic gating is advantageous to the preservation of the band edge sharpness. Thus, 2D-2D heterojunctions can theoretically provide switching by turning off the energy density of states using the gate fields.

There have been several reports of tunneling in layered materials. For example, resonant tunneling was previously reported in graphene-insulator-graphene structures. However, the absence of bandgap in graphene prevents the realization of a tunnel transistor with high \( I_{ON}/I_{OFF} \). We reported the direct observation of gate-controlled band-to-band tunneling in transition metal dichalcogenide-based heterostructure devices. Gate-controlled BTBT and negative differential resistance (NDR) were observed at 77 K, and the NDR peak height and position could be tuned by the gate voltage. Tunneling and NDR in epitaxially grown WSe₂/MoS₂ heterostructures were shown using conductive atomic force microscopy. Black phosphorus/SnSe₂ heterojunctions showed band-to-band tunneling induced NDR at room temperature, using a two-terminal device structure without a gate. Very recently, a steep transistor was realized with polymer electrolyte gating of a p+/Ge/MoS₂ 3D-2D van der Waals heterojunction. Bulk Ge, with its 3D density of states, is the p-side of the tunneling junction. The n-side is an atomically thin MoS₂ layer, which has 2D density of states. This device shows a subthreshold swing of sub-60 mV/dec over several decades of drain current at low current levels. However, a steep switch taking advantage of 2D-2D tunneling, where both n and p-sides are realized with 2D layered materials, has not been realized yet.

In our previous report on BTBT of a MoS₂/WSe₂ heterostructure, a large electric field across the heterojunction was
required to form a type III (broken gap) alignment from the initial type II alignment of the heterostack at equilibrium. The necessity for high fields for the inception of BTBT limited the performance of these devices as steep switches. In this paper, we report a vertical heterojunction tunnel FET with WS\textsubscript{2} as the p-layer and SnSe\textsubscript{2} as the degenerate n-layer, which has been theoretically predicted to be close to a type III alignment at equilibrium.\textsuperscript{15–21} Due to degeneracy of SnSe\textsubscript{2}, a single gate is sufficient to control the band alignment of WS\textsubscript{2} and SnSe\textsubscript{2} from type II to type III. In the tunnel FET fabricated, an SS of \(\sim 100 \text{ mV/dec}\) is observed at room temperature for \(\sim 2\) decades, with a minimum SS of 100 mV/dec. The SS is independent of temperature, confirming that the current is due to direct BTBT. NDR is observed at forward bias at 77 K and diminishes with increasing temperature. While maintaining the quality of the gate oxide/WS\textsubscript{2} interface and WS\textsubscript{2}/SnSe\textsubscript{2} interface across all devices, the use of high-\(\kappa\) ZrO\textsubscript{2} as the gate dielectric facilitates gate oxide scaling and allows the reduction of SS.

The process flow for fabrication of WS\textsubscript{2}/SnSe\textsubscript{2} tunnel FETs is shown in Fig. S1.\textsuperscript{22} Heterostacks of SnSe\textsubscript{2} on WS\textsubscript{2} were made by dry transfer method.\textsuperscript{23} The WS\textsubscript{2}/SnSe\textsubscript{2} heterostacks were then dry transferred onto fabricated local bottom gates. Source/drain contacts to SnSe\textsubscript{2} and WS\textsubscript{2} were then deposited. Electrical measurements on the heterostructure device were performed by holding the potential at the source (SnSe\textsubscript{2} side) at 0 V. The potential applied at the WS\textsubscript{2} contact is considered the drain voltage, \(V_D\). The gate voltage applied on the bottom gate (\(V_G\)) modulates the band offset, hence the tunneling current across the SnSe\textsubscript{2}/WS\textsubscript{2} heterojunction. For all measurements, the Si/SiO\textsubscript{2} substrate was kept at ground potential. Measurements reported in this paper were all performed in vacuum at \(10^{-5}\) Torr.

Before delving into the electrical behavior of WS\textsubscript{2}/SnSe\textsubscript{2} heterojunctions, we study the band alignment of WS\textsubscript{2} and SnSe\textsubscript{2}. Bulk SnSe\textsubscript{2} has a bandgap of 1.1 eV.\textsuperscript{24} Monolayer and bulk WS\textsubscript{2} have bandgaps of 1.6 eV and 1.2 eV, respectively.\textsuperscript{25} The 3–6 layers of WS\textsubscript{2} used in our experiments have a bandgap close to 1.6 eV. In order to obtain the band alignment of WS\textsubscript{2} and SnSe\textsubscript{2}, X-ray photoelectron spectroscopy was performed on the bulk SnSe\textsubscript{2} and WS\textsubscript{2} samples. Figure 1(a) shows secondary electron cut-offs of the photoelectron spectra. The workfunction of the materials can be extracted by plotting the kinetic energy from the Al K\(\alpha\) electron spectra. The workfunction of the materials can be extracted by plotting the kinetic energy from the Al K\(\alpha\) electron spectra. The workfunction of the materials can be extracted by plotting the kinetic energy from the Al K\(\alpha\) electron spectra. The workfunction of the materials can be extracted by plotting the kinetic energy from the Al K\(\alpha\) electron spectra. The workfunction of the materials can be extracted by plotting the kinetic energy from the Al K\(\alpha\) electron spectra. The workfunction of the materials can be extracted by plotting the kinetic energy from the Al K\(\alpha\) electron spectra.
the interface and requires a barrier layer to allow the band alignment modulation.27

Figures 2(a)–2(b) show the gated WSe2/SnSe2 heterojunction device structure and optical image of a representative device. Figures 2(c)–2(e) show the electrical characteristics of the WSe2/SnSe2 heterojunction tunnel FET. The bottom gate consists of ∼8 nm thick ZrO2 as the gate dielectric, and the heterojunction area is ∼100 µm². At the extreme negative gate voltage, WSe2 is accumulated with holes, while SnSe2 is still accumulated with electrons, and the heterojunction is at type III alignment. The $I_D-V_G$ at $V_D=-1$ V shows the gate-controlled tunnel current, with an $I_{ON}/I_{OFF}$ of $>10^3$ (Fig. 2(c)), and a minimum SS of 100 mV/decade at room temperature (Fig. 2(d)). The tunneling current reduces as $V_G$ approaches less negative voltages, and the heterojunction alignment goes towards type II from type III turning the tunnel junction OFF. At $V_G \approx -1.45$ V, the current due to tunneling subsides. The current observed at $V_G > -1.45$ V is due to the electron current across the $n$-WSe2–SnSe2 heterojunction. The SS for the $p$-tunnel FET thus obtained is ∼100 mV/dec for >2 orders of magnitude of drain current. The $I_D-V_D$ with varying gate voltage at room temperature shows an inflection close to $V_D=0$ V, indicating the presence of a Schottky barrier at the WSe2 contact (Fig. 2(e)). Figure S5 shows the performance of another WSe2/SnSe2 heterojunction device fabricated on a 20 nm thick ZrO2 gate, with a heterojunction area of ∼140 µm². The $I_{ON}/I_{OFF}$ is ∼10⁷, with an ON current of ∼4 µA, leading to a current density of ∼30 nA/µm². Due to a thicker gate dielectric, the SS of this device is <200 mV/dec for ∼4 decades of drain current, while the minimum SS is 164 mV/dec at room temperature. The SS is strongly dependent on the effective oxide thickness (EOT) of the gate dielectric.

In order to confirm that the current observed across the heterojunction is due to BTBT, we performed temperature dependent measurements of the $I_D-V_G$. The results are shown

![FIG. 2. Device structure and characteristics of WSe2/SnSe2 heterojunction TFET at room temperature (295 K), in vacuum. (a) Cross-section of device (not to scale). (b) Optical image of a representative device (scale bar 5 µm). (c) $I_D-V_G$ at $V_D=-1$ V. The red curve corresponds to linear scale, and the black curve corresponds to log scale. (d) Subthreshold swing vs. $I_D$. (e) $I_D-V_D$ for varying gate voltages. (Note: The inconsistency in the current levels of $I_D-V_G$ and $I_D-V_D$ is due to hysteresis in the measurement.)](image-url)
in Fig. 3(a), using a device different from the one in Fig. 2. The current at large negative gate voltages (p-branch) is due to tunneling, and the slope of the $I_D-V_G$ curve does not vary with temperature. The tunneling threshold voltage of the p-TFET shifts positively owing to the change in Schottky barrier at the WSe$_2$/Pd contacts. On the other hand, the slope of the $I_D-V_G$ for the n-MOSFET, which operates in the higher $V_G$ range, is strongly dependent on temperature. Figure 3(b) shows the weak dependence of SS on temperature for the p-TFET, and a linear variation of subthreshold slope with temperature for the n-MOSFET. The SS of the n-MOSFET as a function of 1000/T can be fitted with two different linear curves – one for temperature range 77 K to 175 K and the other for the range between 175 K and 295 K. First, the subthreshold slope of the n-MOSFET is much larger than 60 mV/dec at room temperature, possibly due to the presence of traps at the interface between WSe$_2$ and the back gate and at the WSe$_2$/SnSe$_2$ interface. The SS of the MOSFET at 77 K is ~67 mV/dec, while that of the p-TFET is ~140 mV/dec. The invariance of SS with temperature for $I_D$ corresponding to $V_G< -2.2$ V confirms the tunnel FET operation of the WSe$_2$/SnSe$_2$ heterostructure device for this gate voltage range. Figure 3(c) shows qualitative energy band diagrams of WSe$_2$ and SnSe$_2$ under three different conditions: when TFET is ON, when both p-TFET and n-MOSFET are OFF and when n-MOSFET is ON. The type III (broken) band alignment when $V_G$ is highly negative allows tunneling of carriers from valence band of WSe$_2$ to conduction band of SnSe$_2$. The tunneling is reduced as $V_G$ is made less negative, and stops when the WSe$_2$/SnSe$_2$ band alignment goes to type II. However, in this situation, the barrier between SnSe$_2$ and WSe$_2$ conduction bands is still large to impede thermionic emission over the barrier. The n-MOSFET operation commences when the barrier at the conduction bands is reduced enough to allow thermionic emission.

Tunnel FETs show NDR in forward bias $I_D-V_D$ for gate voltages corresponding to the Esaki diode operation regime. We observe NDR at 77 K in a WSe$_2$/SnSe$_2$ heterostructure device, as shown in Fig. 4. The tunnel current at 0 V is low, leading to nonlinearity in $I_D-V_D$. This indicates that the contact resistance in the device is high. The NDR peak-to-valley ratio diminishes with increasing temperature. At 150 K, the drain current flattens out, and NDR can no longer be observed, leaving only a trend towards NDR. The diminishing peak-to-valley ratio of NDR with increasing temperature, and the absence of NDR at room temperature are indicative of an interlayer recombination process that competes with the tunneling process in forward bias.

In conclusion, we demonstrate 2D-2D tunneling in a layered materials heterojunction. A close to type III band alignment of WSe$_2$ and SnSe$_2$ allows the operation of a tunnel FET, with significant $I_{ON}/I_{OFF}$ and steep SS at room temperature. A minimum SS of 100 mV/dec is observed at room temperature. The SS does not vary significantly with temperature, confirming that the current observed is due to band-to-band tunneling at the hetero-interface. NDR observed at...
forward bias at low temperatures further serves as evidence towards BTBT. Moving forward, in order to see limits of the device performance in terms of steeper SS and higher on current, improvement of the contacts and improvement of the heterojunction interface quality are critical. For this purpose, doping of the contact regions is essential to achieve the expected performance of the TFETs based on 2D materials. Moreover, material quality in terms of defects, traps, and surface contaminants determines the interface properties. Therefore, the device performance also depends on the quality of the starting material. This work represents an important step towards the realization of steep devices with using 2D-2D heterojunctions.

T.R. was supported by NSF E3S Center, and Entegris and Applied Materials under the i-Rice program. M.T. was supported through the Electronic Materials Program funded by the Director, Office of Science, Office of Basic Energy Sciences, Material Sciences and Engineering Division of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231. XPS characterization was performed at the U.S. Department of Energy under Contract No. DE-AC02-Sciences, Material Sciences and Engineering Division of the Office of Science of the U.S. Department of Energy supported through the Electronic Materials Program funded by the Director, Office of Science, Office of Basic Energy Sciences, Material Sciences and Engineering Division of the U.S. Department of Energy under Contract No. DE-AC02-05CH11231. XPS characterization was performed at the Joint Center for Artificial Photosynthesis, supported through the Office of Science of the U.S. Department of Energy under Award No. DE-SC0004993.

22. See supplementary material at http://dx.doi.org/10.1063/1.4942647 for fabrication process of WSe2/SnSe2 heterojunction tunnel FET, electrical characterization of SnSe2 FET, contact resistance extraction of SnSe2, Electrical characteristics of WSe2 FET, and XPS characterization of bulk SnSe2, and electrical performance of WSe2/SnSe2 heterojunction TFET with 20 nm thick ZrO2 gate.