

Review

## Nanoelectromechanical Switches for Low-Power Digital Computing

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**Abstract:** The need for more energy-efficient solid-state switches beyond complementary metal-oxide-semiconductor (CMOS) transistors has become a major concern as the power consumption of electronic integrated circuits (ICs) steadily increases with technology scaling. Nano-Electro-Mechanical (NEM) relays control current flow by nanometer-scale motion to make or break physical contact between electrodes, and offer advantages over transistors for low-power digital logic applications: virtually zero leakage current for negligible static power consumption; the ability to operate with very small voltage signals for low dynamic power consumption; and robustness against harsh environments such as extreme temperatures. Therefore, NEM logic switches (relays) have been investigated by several research groups during the past decade. Circuit simulations calibrated to experimental data indicate that scaled relay technology can overcome the energy-efficiency limit of CMOS technology. This paper reviews recent progress toward this goal, providing an overview of the different relay designs and experimental results achieved by various research groups, as well as of relay-based IC design principles. Remaining challenges for realizing the promise of nano-mechanical computing, and ongoing efforts to address these, are discussed.

**Keywords:** relay; nanoelectromechanical systems (NEMS); logic switch; low power

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## 1. Introduction

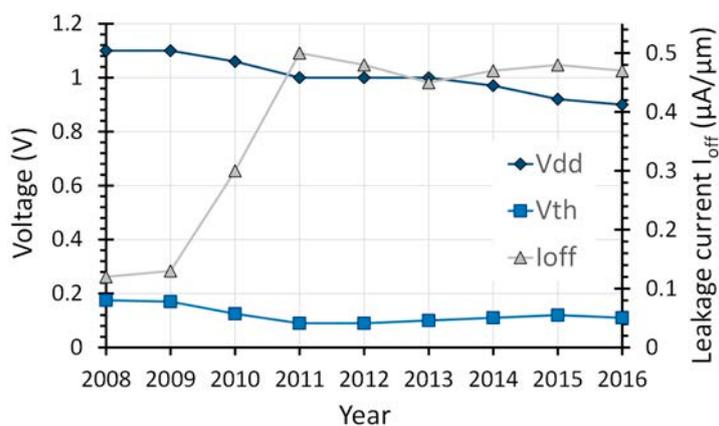
Over the past five decades, steady progress in planar processing technology to manufacture transistors with ever smaller dimensions has provided exponential growth in the number of components (transistors) and, hence, the functionality of integrated circuit (IC) “chips” over time, according to Moore’s Law [1]. In the most recent decade, however, the transistor operating voltage ( $V_{DD}$ ) has not been reduced proportionately with the transistor size (Figure 1) [2]; therefore, as the number and density of transistors on a chip have increased, the peak power density also has increased [3]. Due to limitations of chip cooling technology, either IC blocks must be periodically powered down (disconnected from the power supply) or the digital logic circuits must be operated at slower speeds with parallelism (e.g., multi-core processing) used to achieve improvements in system performance [4]. The root cause of this chip power crisis is transistor OFF-state leakage current ( $I_{OFF}$ ), as explained below.

Figure 2a illustrates the basic metal-oxide-semiconductor field-effect transistor (MOSFET) structure, which is essentially a three-terminal solid-state switch: when a sufficiently large voltage (greater than a “threshold voltage”  $V_{TH}$ ) is applied to the metallic gate electrode, the transistor is in the ON state and electric current can readily flow through the semiconductor channel region between the heavily doped (electrically conductive) semiconductor source and drain regions (Note that the gate electrode is electrically insulated from the channel region by a thin insulating oxide layer so that no direct current flows between the gate and semiconductor). In the sub-threshold regime of operation, the current ( $I_D$ ) decreases exponentially with decreasing gate voltage ( $V_G$ ) below  $V_{TH}$ , reaching  $I_{OFF}$  at  $V_G = 0$  V, as illustrated in Figure 2b; the rate at which the current changes is defined as the subthreshold swing ( $SS$ ), i.e.,  $I_{OFF}$  is proportional to  $10^{-V_{TH}/SS}$ . The static power consumption of a digital logic circuit is proportional to  $I_{OFF}$ ; this has limited  $V_{TH}$  scaling and, hence,  $V_{DD}$  scaling, since the peak MOSFET ON-state current (hence the circuit operating speed) is a super-linear function of  $V_{DD} - V_{TH}$ .

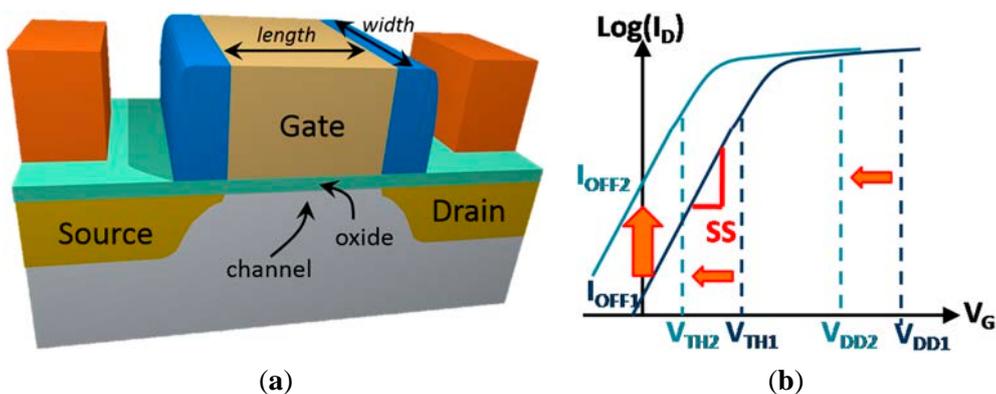
To mitigate the chip power crisis, MOSFET design improvements which provide for high ON-state currents ( $I_{ON}$ ) at a lower  $V_G$  have been adopted in recent years. Strained silicon technology is used to boost the mobility of mobile charge carriers in the silicon channel region and, hence,  $I_{ON}$  [5]. High-permittivity (high- $k$ ) dielectric material is incorporated into the gate-insulating layer [6] to provide for improved capacitive coupling between the gate electrode and channel region, to steepen the subthreshold swing so that  $V_{TH}$  is lower for a given  $I_{OFF}$  specification. Thin-body transistor structures such as the fully depleted silicon-on-insulator (FDSOI) MOSFET [7] and the three-dimensional (3-D) FinFET [8,9] provide for even better gate control and steeper subthreshold swing.  $SS$  is fundamentally limited to be no less than  $\ln(10) \times k_B T/q = 60$  mV/dec at room temperature, however, due to the Fermi-Dirac energy distribution of electrons in the semiconductor source region. Because of this fundamental limitation of the MOSFET, alternative logic switch designs are needed to enable further reductions in chip operating voltage.

Tunneling has been proposed as a current conduction mechanism that can be switched more abruptly than thermionic emission (in a MOSFET) [10,11]. Tunneling FET (TFET) devices have been experimentally demonstrated with sub-60 mV/dec subthreshold swing [12,13], but generally have exhibited relatively poor ON/OFF current ratio for gate voltage swing below 1 V. A mechanical switch is ideal in that it has zero  $I_{OFF}$  and abrupt switching behavior which, in principle, allows  $V_{TH}$  and, hence,  $V_{DD}$  to be scaled down aggressively while maintaining high conductance in the ON state (limited

by the physical contact resistance). The use of mechanical switches for computing is not a new idea, and dates back to the 1930s [14]. Due to advancements in planar processing technology over the past few decades, particularly the development of surface micromachining processes for micro-electro-mechanical systems (MEMS) [15], there has been renewed interest in mechanical computing for ultra-low-power digital logic applications [16,17]. This paper reviews recent work toward the goal of achieving nano-electro-mechanical (NEM) logic switches suitable for low-power computing. The following sections will provide an overview of different relay designs and experimental results achieved by various research groups, and of relay-based IC design principles. Remaining challenges for realizing the promise of mechanical computing, and ongoing efforts to address these, are discussed.



**Figure 1.** Trends for metal-oxide-semiconductor field-effect transistor (MOSFET) threshold voltage ( $V_{TH}$ ) and operating voltage ( $V_{DD}$ ), and corresponding transistor OFF-state leakage ( $I_{OFF}$ ), for high-performance digital logic [2].



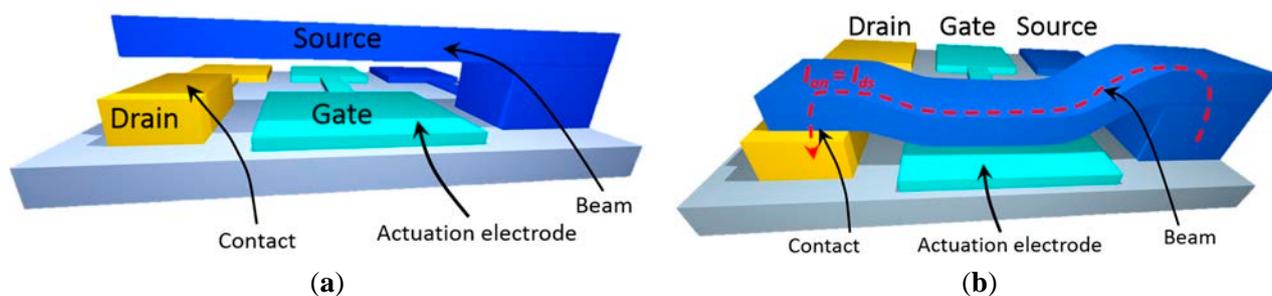
**Figure 2.** Schematic illustrations of the MOSFET (a) structure, (b) transfer characteristics (output current  $I_D$  vs. input voltage  $V_G$ ). If the operating voltage ( $V_{DD}$ ) is to be reduced, then the threshold voltage ( $V_{TH}$ ) should be reduced (*i.e.*, the  $I$ - $V$  curve should be shifted to the left) to maintain the same peak level of ON-state current, but this would result in an exponential increase in OFF-state leakage current ( $I_{OFF}$ ).

## 2. Brief Overview of Logic Relay Technologies

Relays use the mechanical motion of a movable electrode (beam or membrane) to make/break physical contact between two electrically conductive electrodes in order to switch current ON/OFF. The first MEM relay was demonstrated by Petersen in 1979 [18]. In subsequent years, various types of relays have been investigated and can be classified according to their actuation mechanism [19]. Thermal relays use different thermal expansion coefficients of two materials to bend a cantilever under the effect of heating. Magnetic relays use ferromagnetic material in the movable electrode to actuate it with the application of a magnetic field. Piezoelectric relays use the deformation of a piezoelectric material under the effect of an electric field. Electrostatic relays directly use the effect of an electric field to actuate a suspended electrode with an applied voltage. Commercial applications of MEM switches include automated test equipment, wide band systems, and tunable antennas [20].

The need for a very small device footprint and fast switching speed makes thermal actuation and magnetic actuation unsuitable for digital logic applications. Piezoelectric relays have been demonstrated in the works of Zaghoul and Piazza at Carnegie Mellon University. They used a stack of ultra-thin (10 nm) AlN layers sandwiched between metallic electrodes [21–23]. The actuation voltage is around 520 mV and the relay can even switch with voltages as low as 20 mV (by applying a bias voltage to the substrate), which is the smallest pull-in voltage reported for a logic relay to date. However, the footprint is around  $58 \mu\text{m}^2$  for the smallest device. Piezoelectric devices are difficult to scale down to a very small size.

Electrostatic switches of various designs have been reported in the literature, with the number of terminals ranging from two up to six. A minimum of three (one control and two output) terminals is required for a logic relay. Figure 3 shows a schematic of a basic three-terminal (3T) relay in which the input voltage signal is applied to the fixed “gate” terminal and the output current signal flows between the movable “source” terminal and the fixed “drain” terminal. In the following section, the operation and properties of this basic electrostatic relay are described in more detail.



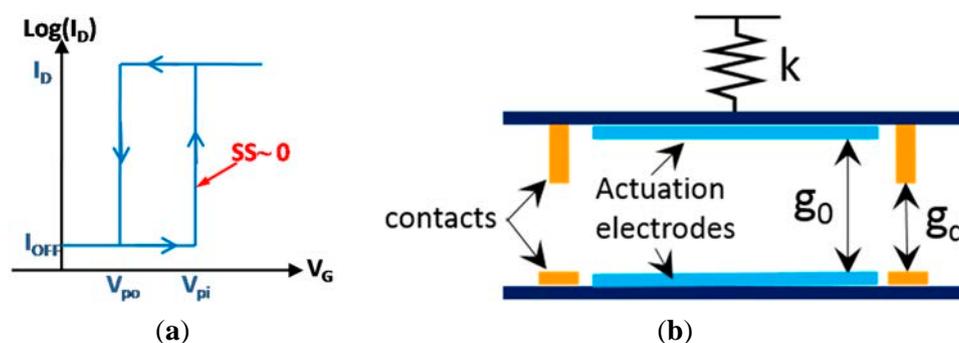
**Figure 3.** Illustration of an electrostatic 3T relay: (a) as fabricated, (b) actuated into the ON state.

## 3. Electrostatic Relay Basics

### 3.1. Benefits for Digital Logic Applications

Compared with the MOSFET, the electrostatic relay offers many advantages. First, there is a significant reduction in standby power consumption, since leakage current is negligible due to the physical separation of the two conductive electrodes in the OFF state. Second, there is abrupt switching behavior, with  $SS \approx 0$  (Figure 4a), which enables very small operating voltage swing,

potentially as low as ~10 mV (determined by the hysteresis voltage) [24]. These two advantages make nano-electro-mechanical (NEM) relay-based circuits potentially more energy efficient than their complementary metal-oxide-semiconductor (CMOS) counterparts [16,17]. Since MOSFETs are superior for high-speed switching, hybrid CMOS/NEM relay circuits show the most promise for achieving a good balance of energy efficiency and information processing throughput. NEM relays are also less sensitive than MOSFETs to radiation, which makes them advantageous for aerospace and military applications.



**Figure 4.** (a) Electrical characteristics of a nano-electro-mechanical (NEM) relay. (b) Spring model of a NEM relay.

### 3.2. Device Operation

Figure 4b illustrates the spring model of a NEM relay, which is comprised of a fixed actuation electrode (often defined as the gate, as in a MOSFET) and a movable electrode (often defined as the source in a 3T relay). Physical contact is established between the movable source electrode and a fixed contact electrode (often defined as the drain) in the ON state to allow current to flow and thereby transmit an electrical signal. The state of the relay depends on the forces applied to the movable structure: the electrostatic actuation force ( $F_{elec}$ ), the mechanical spring force which acts to release the electrode from contact ( $F_{rl}$ ), and the contact adhesive force ( $F_{adh}$ ). As the applied voltage between the actuation electrode and the movable electrode increases, the balance between the electrostatic force and the release force reaches a metastable limit when the distance between them is reduced by  $g_0/3$ , where  $g_0$  is the initial thickness of the air-gap between the actuation and movable electrodes. This point defines the “pull-in” voltage ( $V_{pi}$ ). Once the applied voltage is greater than  $V_{pi}$ , the source “snaps” into contact with the drain and the relay is thereby switched ON. Note that the initial thickness of the air-gap between the source and drain electrodes ( $g_d$ ) is smaller than  $g_0$  to avoid ensure zero gate current. Similarly, the balance between the electrostatic force, the release force, and the adhesion force just before contact is broken defines the “pull-out” voltage ( $V_{po}$ ), which is sometimes also referred to as the release voltage. When the applied voltage becomes lower than the “pull-out” voltage ( $V_{po}$ ), the source electrode is actuated out of contact so that current can no longer flow. The “pull-in” and “pull-out” voltages are given by the following equations:

$$V_{pi} = \sqrt{\frac{8kg_0^3}{27\epsilon_0LW}} \tag{1}$$

$$V_{po} = \sqrt{\frac{2(g_0 - g_d)^2}{\epsilon_0 L w} (k g_d - F_{adh})} \tag{2}$$

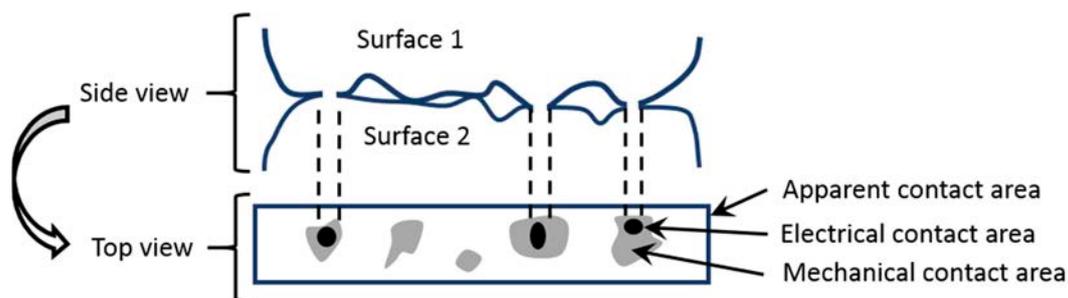
where  $k$  is the effective spring constant (stiffness) of the movable electrode,  $\epsilon_0$  is the dielectric permittivity of air, and  $L$  and  $w$  are the length and the width of the actuation electrode, respectively. (These equations are valid for a “pull-in mode” relay, that is if  $g_d/g_0 > 1/3$ . If  $g_d/g_0 < 1/3$ , then contact is made before the pull-in point and the relay is said to be operating in “non-pull-in” mode.) It should be noted that Equation (1) assumes quasi-static operation. In dynamic operation, the kinetic energy of the movable electrode tends to decrease the value of the pull-in voltage: For a step actuation voltage, the dynamic value of the pull-in voltage can be analytically calculated and is equal to 91.9% of the value calculated by Equation (1) for the case of no damping [25].

### 3.3. Contact Resistance

The primary measure of the quality of an electrical contact is the contact resistance  $R_c$ . The notion of contact resistance is not as trivial as it may first appear. It involves the physics of contact mechanics with electrical conduction. The first model was developed by Holm in 1967 [26] and numerous works have been conducted since then to describe contact physics according to geometry (sphere, flat), material (elastic, plastic), surface roughness, adhesion, *etc.* [27]. A recent review summarized the different models and works in this regard [28]. Due to roughness of the contacting surfaces, only some small parts within the apparent contact area are in physical contact when the relay is in the ON state; these correspond to the points of the highest asperities (Figure 5). Some of those contact points might not be conductive, however. The sum of currents flowing through the conductive contacting points determines the contact resistance. In a NEM relay, the contact resistance is given by the Sharvin model, due to the small dimensions of the contact.  $R_c$  depends on the electrical resistivity  $\rho$ , the electron mean free path  $l$ , and the radius of the contacting asperity  $r$ :

$$R_c = R_{sh} = \frac{4\rho l}{3\pi r^2} \tag{3}$$

In contrast to RF MEM relays for which the contact resistance should be lower than  $1 \Omega$  to achieve low insertion loss, a NEM relay can have contact resistance as high as several  $k\Omega$  because the digital circuit operating speed is limited by the mechanical switching delay of the relay rather than the electrical (“RC”) charging delay. This tolerance for high  $R_c$  allows for more possibilities to find a high endurance contact material.



**Figure 5.** Illustration of the apparent, mechanical, and electrical contact areas.

#### 4. Recent Progress in Electrostatic M/NEM Logic Relay Technology

This section highlights recent work by various research groups that are investigating NEM relays for digital logic applications.

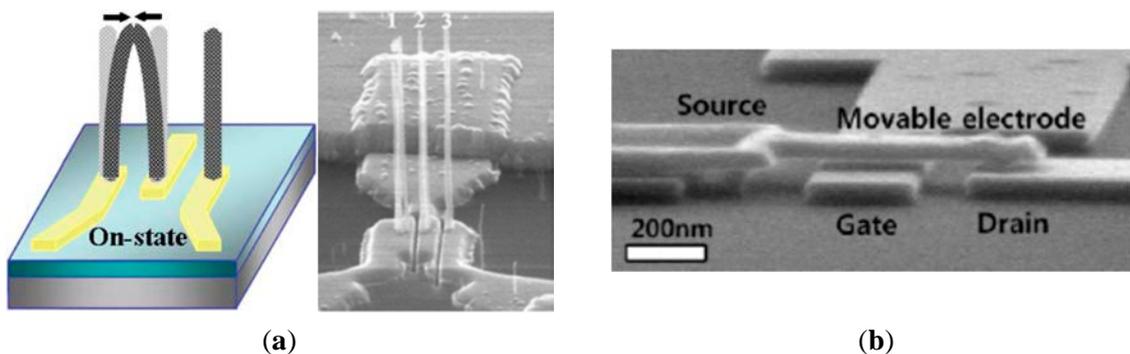
##### 4.1. First Demonstration of a NEM Relay

The article of Jang *et al.* [29] in 2005 is one of the earliest demonstrations of a NEM relay following the work of Rueckes *et al.* [30]. This relay is comprised of three multi-walled carbon nanotubes (MWCNT) whose vertical orientation facilitates higher device integration density. The source and drain CNT electrodes are on the left, whereas the gate CNT electrode is on the right (Figure 6a). By applying a positive voltage to each of the drain and gate electrodes, the drain CNT bends towards the grounded source to establish physical contact. In this first publication, the actuation voltage applied to the gate is around 24 V. A second publication by the same team in 2008 showed a more optimal placement of the gate electrode, at around 30 nm from the CNT drain. This improved design resulted in lower actuation voltage, around 4.5 V [31].

Within the last 10 years, several NEM relays based on CNT [32], graphene, or nanowires have been fabricated [33]. They offer attractive performance characteristics: a high on/off current ratio ( $I_{ON}/I_{OFF}$ ), a high switching speed (approximately 1 ns), and a pull-in voltage that can reach down to a few volts [34,35]. Each of these devices was fabricated using a “bottom-up” approach, which presents challenges for high-volume manufacturing. Manual tools are sometimes needed to manipulate the wires to create the relays [30], however. Another practical challenge for implementing relays with CNTs is a significant decrease (by multiple orders of magnitude) in the conductivity of a metallic CNT upon mechanical bending [36,37]. Additional issues are a relatively large actuation voltage (inherent due to the small actuation area), a large hysteresis voltage [38], and low endurance. A large number of those works have been summarized in the review of Loh and Espinosa [39]. Below, we mainly consider NEM relays fabricated with conventional “top-down” fabrication processes which are more suitable for co-integration with CMOS transistors.

##### 4.2. First Demonstration of a NEM Relay Using a CMOS-Compatible “Top-Down” Fabrication Process

The first demonstration of an electrostatically actuated mechanical switch with nanometer-scale dimensions fabricated using a top-down process was published by Jang *et al.*; however, it is a two-terminal device [40,41], not suitable for logic applications. A nanoscale 3T relay from the same research team was reported soon afterwards (Figure 6b) [42]: the length of the beam is 700 nm and the as-fabricated contact gap thickness is 40 nm. The contact material is TiN. This relay was immersed in a liquid medium (oil) to reduce its pull-in voltage. The pull-in voltage varies substantially from 8 V to 12 V in air and from 4 V to 8 V in oil. The endurance is only a few cycles, both in air and oil ( $V_{DD} = 5$  V,  $I_D = 10$  nA). Another 2T device was presented in 2013 with a “pipe-clip” structure, with a minimum contact gap thickness of only 4 nm (the smallest to date) [43].

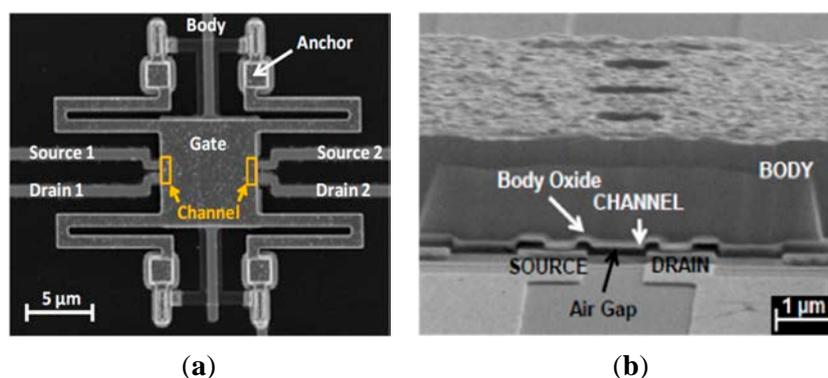


**Figure 6.** (a) First demonstration of NEM relay using MWCNT [29] (Reprinted with permission from [29], copyright 2005, AIP Publishing LLC). (b) Demonstration of “top-down” fabricated 3T relay developed in KAIST [42] (© 2009 IEEE, reprinted with permission from [42]).

### 4.3. Other Relays Fabricated Using CMOS-Compatible Processes

#### 4.3.1. “Out-of-Plane” Actuation Relays

The logic relay developed at UC Berkeley is comprised of a movable body electrode formed in a layer of polycrystalline silicon-germanium to which a conductive strip of metal (the “channel”) is attached via an insulating layer of aluminum-oxide (Figure 7) [44–46]. Two variations of this insulated-body relay design, 4T and 6T, have been reported. The contacting electrode material initially was tungsten (W) and later changed to ruthenium (Ru) and other materials for improved  $R_c$  stability [47,48]. Although the in-plane dimensions of this relay are in the micrometer range, the as-fabricated contact gap thickness ( $g_d$ ) is in the nanoscale range [44]. Operating (gate voltage) lower than 1 V has been enabled by applying a body bias voltage [48] with a turn-on delay below 1  $\mu$ s. Reliability studies have shown that  $R_c$  remains below 10 k $\Omega$  under hot switching conditions for more than  $10^8$  cycles [49]. Circuits designed with such devices are expected to operate with at least one order of magnitude better energy efficiency than their CMOS counterparts, based on a benchmarking study of 32-bit adder performance at the 65 nm technology node [22,50].



**Figure 7.** Scanning electron micrographs of a logic relay fabricated by researchers at the University of California, Berkeley: (a) Plan view of a 6T relay [46] (© 2012 IEEE, reprinted with permission from [46]). (b) Tilted cross-sectional view of the relay along the channel, source, and drain of the relay.

### 4.3.2. “In-Plane” Actuation Relays

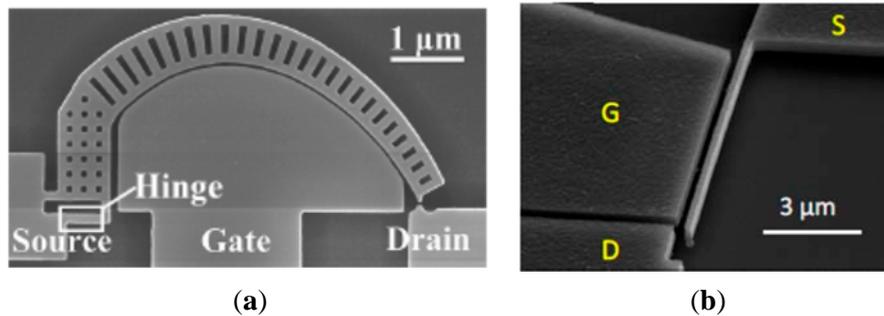
The first relay publication from the research group at Stanford University concerned the design and prospects of NEM relays for logic applications [16,51]. It notes that low-density structural materials (Si or Al) and the presence of a contact “bump” (to reduce the as-fabricated contact gap thickness) can provide switching times to be on the order of nanoseconds. Although logic gates implemented with NEM relays still would operate more slowly (sub-GHz) than logic gates implemented with CMOS transistors, they could have lower energy loss for equivalent areas ( $E_{\text{stat}} < 0.1$  fJ for  $A < 0.03$   $\mu\text{m}^2$ ).

Two subsequent articles published by the same group at Stanford mainly focused on device fabrication. The first one [52] shows the design and the fabrication process for a planar laterally actuated poly-Si relay with Pt as the contact electrode material. Two proof-of-concept devices, simple cantilever or double-clamped beam structures, were reported with actuation voltage  $V_{\text{act}} > 12.5$  V ( $V_{\text{po}} > 3$  V) and  $V_{\text{act}} > 26$  V ( $V_{\text{po}} > 19$  V). The second article [53] goes further by detailing the properties and applications of NEM relays, the advantages of lateral actuation, device simulations, fabrication process development, reliability testing, and the demonstration of a relay multiplexer. The results show improved performance with  $V_{\text{act}} = 10.7$  V ( $V_{\text{pi}} = 7.9$  V),  $R_c \approx 3$  k $\Omega$  with Pt contact coating. Cycling tests under “hot switching” conditions (1 V/1  $\mu\text{A}$ ) demonstrated endurance greater than  $10^8$  cycles.

Recently, European researchers in Switzerland and the United Kingdom (IBM, EPFL, University of Bristol, TEC) have made 3T and 4T NEM relays with an in-plane curved cantilever structure (Figure 8a) [54,55]. Among the physical dimensions are an as-fabricated contact gap thickness of 50 nm and a total surface area estimated to 15  $\mu\text{m}^2$ . An amorphous carbon coating layer (a-C) reduces the contact resistance to  $R_c = 15$  k $\Omega$  and reduces the hysteresis voltage to 0.5 V, four times lower than for Pt contacts [56]. The pull-in and pull-out voltage are about 7 V and 5 V, respectively. Actuation with  $\pm 0.5$  V swing has been achieved by applying a bias voltage [57]. The turn-on delay is about 200 ns.

### 4.3.3. Silicon Carbide (SiC) Relays for Harsh Environments

The robust properties of SiC at high temperatures make this material attractive for outer space and military applications. Various NEM relays using SiC nanowires were fabricated using a top-down approach by a research group at Case Western Reserve University in collaboration with researchers at the California Institute of Technology. They fabricated 2T switches using a very thin beam [58] and, more recently, 3T relays were fabricated [59,60] with a footprint of 1  $\mu\text{m}^2$  and an as-fabricated contact air-gap thickness of 100 nm (Figure 8b). Electrical characterizations of the relay operating at room temperature and at 500 °C demonstrated switching voltages of 15 V and 11 V, respectively. The endurance of this device is better than 14,000 cycles under “hot-switching” conditions (100 mV/150 nA) at 0.125 Hz. Several logic gates (AND, XOR) based on this relay technology were also demonstrated [61–63].



**Figure 8.** (a) NEM relay with a curved cantilever [57] (© 2014 IEEE, reprinted with permission from [57]). (b) SiC relay [59] (© 2013 IEEE, reprinted with permission from [59]).

#### 4.4. Additional NEM Switch Demonstrations

A research team from Sandia National Laboratories also developed a laterally actuated NEM relay [64]. Numerous switches with very small dimensions of actuation gap thickness (30–100 nm) and contact gap thickness (20–70 nm) were fabricated, but only a few were able to be actuated due to a low manufacturing process yield. Their pull-in voltages are higher than 4 V with a turn-on delay of a few hundred ns. Endurance testing at 1 kHz demonstrated more than  $2 \times 10^6$  cycles.

Researchers at Cornell University demonstrated a vertically oriented, laterally actuated 4T NEM relay [65]. The channel electrode is mounted on a Si pillar whose thickness is around 150 nm. The initial distance between the two contacting electrodes (metal material not specified) is estimated to be between 200 nm and 350 nm. Contact is made by bending and torsion of the pillar. However, after the first actuation, only the torsional mode is available, as the channel is definitively stuck to the drain. The pull-in voltage is 15 V for the first actuation and 10 V for subsequent cycles.

A team from the National University of Singapore has made a NEM relay with two torsion bars for a non-volatile memory application [66]. The footprint of the device is in the micrometer range ( $L = 9 \mu\text{m}$ ,  $W = 1 \mu\text{m}$ ) and the as-fabricated contact gap thickness is between 80 nm and 100 nm. The pull-in voltage is  $V_{\text{pi}} = 5.5 \text{ V}$ . The cycling tests do not show promising results, as the relay demonstrates unstable behavior after only a few cycles.

#### 4.5. Summary

Table 1 summarizes key features of the aforementioned NEM relays. The first two rows list devices fabricated with bottom-up processes, but they are included since they were the first demonstrations of NEM relays.

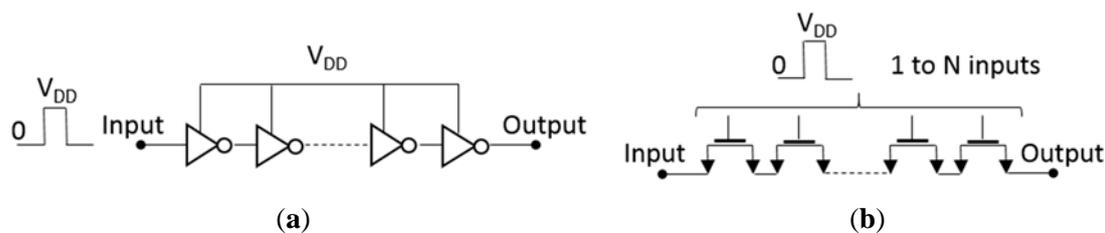
**Table 1.** Summary of reported nano-electro-mechanical (NEM) relays for logic applications (Areas in parentheses are estimated).

Research Group	Type	Area	c-gap	$V_{pi}$	$R_c$	Cycles	Material	Circuit
First CNT [29,31]	3T	-	30 nm	4.5 V	1 M $\Omega$	>1	CNT	No
First Top-Down (KAIST) [40–43]	3T	-	40 nm	4 V	-	>10	TiN	No
Out-of-Plane (UC Berkeley) [44–50]	4T	-	80 nm	<1 V	1 k $\Omega$	>10 <sup>8</sup>	W	Yes
	6T	-	250 nm	10 V	-	>1	Ru	Yes
In-Plane (Stanford University) [51–53]	6T	-	-	10 V	-	>1	TiO <sub>2</sub>	Yes
	5T	-	-	7.9 V	3 k $\Omega$	10 <sup>8</sup>	Pt	Yes
Curved (NEMIAC) [54–57]	3T	15 $\mu\text{m}^2$	50 nm	0.5 V	5 k $\Omega$	>10 <sup>8</sup>	a-C	Yes
	4T							
SiC Relays (CWR University) [58–63]	3T	1 $\mu\text{m}^2$	100 nm	15 V	10 M $\Omega$	>14,000	SiC	Yes
Sandia National Lab [64]	3T	(10 $\mu\text{m}^2$ )	30 nm	>4 V	-	2 $\times$ 10 <sup>6</sup>	Ru	No
Cornell University [65]	3T	(3 $\mu\text{m}^2$ )	200 nm	10 V	10 M $\Omega$	-	-	No
Piezoelectric (CM University) [21–23]	4T	58 $\mu\text{m}^2$	-	10 mV	16 k $\Omega$	-	Pt	No

## 5. Relay-Based Logic Circuit Design

Simple relay-based logic gates (AND, XOR, *etc.*) have been demonstrated in [58–60]. Since the mechanical switching delay (greater than 1 ns) of a relay is orders of magnitude larger than its electrical charging/discharging delay (less than 1 ps for  $R_c$  on the order of k $\Omega$ ), very-large-scale integrated (VLSI) relay circuits should be comprised of single-stage complex logic gates, so that the delay per operation is essentially one mechanical delay [17]. Relay-based ICs following this design methodology were demonstrated in [50].

Since the optimal topology of a relay-based circuit is quite different than a CMOS implementation, a fair comparison of relay *vs.* CMOS energy performance must be made at the circuit (block) level rather than at the device level. Although digital systems comprise a variety of functional blocks, the energy performance tradeoffs for the majority of CMOS gates are similar to that of a CMOS inverter. Therefore, a representative comparison can be made for a relay chain *vs.* a CMOS inverter chain, as shown in Figure 9. Simulation-based studies project NEM relay technology to be able to achieve more than a one order of magnitude improvement in energy efficiency as compared with CMOS technology, for an equivalent area and a mechanical switching delay of 10 ns [17,50].



**Figure 9.** Illustration of digital signal propagation delay in optimally designed (a) complementary metal-oxide-semiconductor (CMOS) logic circuit, (b) NEM relay-based logic circuit.

Hybrid CMOS/NEM technology can potentially achieve the advantages of high-speed CMOS operation together with low-power NEM relay operation [67]. For example, a hybrid NEMS/CMOS static random-access memory (SRAM) cell design for lower static power dissipation and improved cell stability is proposed in [48], and projected to provide a reduction in energy loss of 85%, improvement in write and read times by 60% and 10%, respectively, and an improved static noise margin. As another example, NEM relays can be monolithically integrated with CMOS devices to implement non-volatile SRAM and non-volatile content-addressable memory (CAM) for reduced power consumption [68].

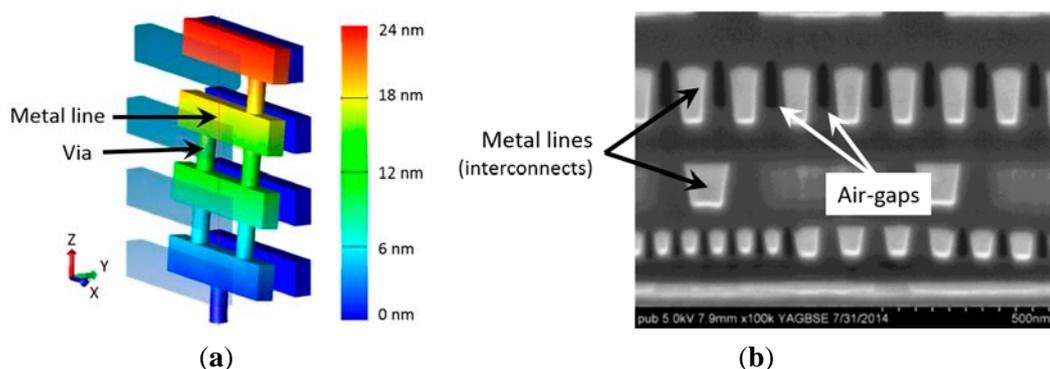
## 6. Remaining Challenges and Pathways to Solutions for NEM Relay Technology

Although MEM relays for RF signal switching have been investigated for several decades, NEM relays for digital logic applications have drawn increasing attention only recently. The works reviewed in the last two sections (even if not exhaustive) are a good indicator: 72% of the referenced articles appeared within the last five years and 50% within the last three years. Further work is needed to address the following remaining challenges and for NEM relays to be practical for low-power digital computing:

- The ability **to achieve high manufacturing yield**. This is especially a challenge for NEM relays incorporating carbon nanotubes, nanowires, or graphene, which are fabricated using bottom-up processes. Well-established top-down planar processing and surface-micromachining techniques should be leveraged for the high-volume manufacture of NEM relays. Ideally, a relay fabrication process should be compatible with back-end-of-line (BEOL) processing to facilitate co-integration with CMOS circuitry [69].
- The ability **to scale down the device footprint**. Most of the NEM relays reported to date have micrometer-scale lateral dimensions. Reducing the size of the relay is particularly constrained by the requirement of low actuation voltage and the fact that the contact air-gap thickness cannot be infinitesimally small. A large area is needed to generate a large enough  $F_{elec}$  to overcome  $F_{ri}$ , which in turn has to be larger than  $F_{adh}$  [70]. To reduce the footprint of a NEM relay to below  $0.1 \mu\text{m}^2$ , researchers at the University of California, Berkeley, have proposed to utilize multiple layers of metal to implement a compact, vertically oriented structure (Figure 10a) [68]. This design is based on the utilization of several layers of air-gap interconnects available in state-of-the-art CMOS technology (Figure 10b) [71], and can achieve a very low pull-in voltage ( $V_{pi} = 1 \text{ V}$  for  $A < 0.1 \mu\text{m}^2$  and 20 ns switching delay). The feasibility of this approach remains to be proven.

- The ability **to operate at a very low voltage** for low active power consumption. Minimization of adhesion at contacting asperities is a challenge for achieving a very low (mV) operating voltage, since  $F_{\text{elec}}$  decreases quadratically with decreasing actuation voltage and must be greater than  $F_{\text{adh}}$ . This sets the fundamental energy efficiency limit for a relay. Adhesion is not fully understood in electrical contacts. However, numerous studies of mechanical contact have emerged in recent years, especially to meet the need in microsystems [72,73].

It should be noted that the actuation area and/or the operating voltage of a 4T relay can be reduced by applying a body bias voltage to reduce the gate voltage swing required to operate the switch. The hysteresis voltage limits the degree to which the gate voltage swing can be reduced in this manner, however, pointing again to the need to minimize contact adhesive force. Several NEM relays have already demonstrated sub-1 V operating voltages using the body-biasing technique [22,48,54].
- The ability **to achieve sufficiently high endurance**. An endurance of  $3 \times 10^{14}$  (*i.e.*, less than one quadrillion) ON/OFF switching cycles is sufficient to guarantee device functionality over a period of 10 years at 100 MHz operating frequency with a duty factor of 1%. To date, the best NEM relay endurance demonstrated is less than  $10^{10}$  cycles. Relay failure modes are well known, as they are similar to those observed for RF MEMS relays: either oxidation of the contact surfaces, which induces a strong increase of the contact resistance at low contact voltages, or material transfer, which results in stiction (welding) [74,75]. Of these two failure modes, it appears that oxidation of the contact surfaces is the main limiting one for logic relays. Indeed, in [76], a reliability model is developed to project the number of switching cycles before welding-induced failure as a function of  $1/V$ , and accelerated lifetime tests indicate that endurance should exceed  $10^{14}$  cycles for operating voltages below 1 V; the projected endurance goes up to  $10^{16}$  cycles at 0.5 V. Therefore, contact welding is not anticipated to be the main reliability issue for NEM relays.



**Figure 10.** (a) New vertical NEM relay structure using BEOL metal layers (adapted from [68]). (b) The most advanced BEOL technology incorporates air-gaps between metal interconnects [71] (© 2014 IEEE, reprinted with permission from [71]).

Contact material selection is key to overcoming the reliability challenge for NEM relays. A larger range of materials can be considered for NEM relays than for RF MEM switches since low contact resistance is not required. The main difficulty is to find a material that is mechanically durable and

electrically stable over  $10^{15}$  switching cycles. Several works have helped to narrow down the material choices. The article of Chowdhury *et al.* [77] deals with the study of contact materials with an atomic force microscope (AFM)-based experiment. The study is performed using a Cr AFM cantilever to make/break contact with several substrate materials (Ir, Pt, W, Ni, Cr, Ti, Cu, Al, and graphite). Best results are obtained with Ti contacts, which show good cycling behavior with relatively low adhesion and low contact resistance (attributed to the rupture of the native Ti oxide) over  $10^5$  cycles. Graphite also shows good results with cycles with a low adhesive force (65 nN) and stable contact resistance. W and Pt have the lowest adhesive forces (<25 nN) but their contact resistances increase over time [49]. Contact oxidation in addition to high adhesion force (>100 nN) is also observed for Al, Ir, and Cu. Cr and Ni have intermediate results as their values of adhesion forces are 62 nN and 65 nN, respectively. Their contact resistances are stable but typically very high (100 to 1000 times higher than other materials). Gold (Au) does not appear to be an appropriate material because of its low hardness. Amorphous carbon has been used in some relays and shows low adhesion (<100 nN) and good  $R_c$  (15 k $\Omega$ ) over  $10^8$  cycles, which makes it a potential candidate for contacts in NEM relays [56].

A promising contact material appears to be Ru and/or its oxide RuO<sub>2</sub>. Indeed, recent studies performed by Czaplewski *et al.* [78] showed that RuO<sub>2</sub> (over Au) contacts could reach more than  $10^{10}$  cycles in MEM relays without failure. Such a performance was obtained by optimizing the design to reduce the impact velocity and, thus, the plastic deformation to the contact, and by using an inorganic sacrificial layer during the fabrication steps. Ruthenium oxide is an electrically conductive material whose electrical resistivity is only seven times higher than that of ruthenium. Therefore, thanks to its electrical conductivity and its resistance to oxidization (as it is a stable oxide), RuO<sub>2</sub> appears to be an intriguing contact material for NEM relays.

## 7. Conclusions

The fundamental limitation in the energy efficiency of CMOS digital logic circuits necessitates new logic switch technology to enable continued improvement in chip functionality within power density constraints. NEM relays are promising candidates for low-power applications as they have negligible OFF-state leakage current ( $I_{OFF}$ ) and abrupt switching behavior which, in principle, enables very low switching voltages. Much progress has been made in recent years (Table 1) toward realizing this promise. Further work is needed to develop compact NEM relays that can be manufactured with high device yield and that can be operated with a very low voltage with sufficient reliability (contact resistance stability) to have a revolutionary impact for future IC technology.

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## Conflicts of Interest

The authors declare no conflict of interest.

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