Effect of Body Biasing on the Energy-Delay Performance of Logic Relays

Chuang Qian, Alexis Peschot, I-Ru Chen, Yenhao Chen, Nuo Xu, and Tsu-Jae King Liu

***Abstract*— The effect of the body bias voltage on logic relay performance is investigated. The switching hysteresis voltage, which sets a lower limit for the relay operating voltage, is experimentally found to decrease with increasing body bias voltage, due to reduced surface adhesive force. It is demonstrated that the switching energy of a relay can be reduced by body biasing, at a tradeoff of increased mechanical turn-ON delay. Simulations of nanoscale relay designs indicate that body biasing can be used to mitigate relay manufacturing challenges, while enabling ultralow-voltage (sub-100 mV) operation with relatively fast switching speed.**

***Index Terms*— Body bias, NEM relay, energy-delay, low-power, nanoelectromechanical systems (NEMS).**

I. Introduction

COMPLEMENTARY metal-oxide-semiconductor (CMOS) technology is fundamentally limited in energy efficiency due to non-zero transistor OFF-state leakage current (I_{OFF}) [1], [2]. That is, the energy required to perform a digital logic operation cannot be decreased to be infinitesimally small, due to a trade-off between dynamic energy consumption and static energy consumption. For ultra-low-power (low frequency) applications, such as distributed sensor networks and the Internet of Things, nano-electro-mechanical (NEM) relay technology is potentially more energy efficient than CMOS technology because mechanical switches have zero I_{OFF} and abrupt switching behavior which in principle enable ultra-low operating voltage [3]. Thus, relays as logic switches have been developed and intensively investigated [4]–[8].

Fig. 1 shows the structure of a fabricated 6-terminal (6-T) micro-electro-mechanical (MEM) logic relay comprising one gate electrode, one body electrode, and two pairs of output (source/drain) electrodes. When the magnitude of the gate-to-body voltage (V_{GB}) is larger than that of the pull-in voltage (V_{PI}), the electrostatic force (F_{elec}) is sufficient to actuate the body downward such that each of the channels (narrow metal strips attached to the underside of the body via an insulating dielectric layer) contacts with its respective pair of source/drain electrodes so that output current (I_{DS}) suddenly can flow. When V_{GB} is reduced below the release voltage (V_{RL}), the spring restoring force (F_{spring}) of the folded-flexure suspension beams actuates the body upward, such that contact between the channels and their respective source/drain electrodes is broken so that I_{DS} suddenly drops to zero.

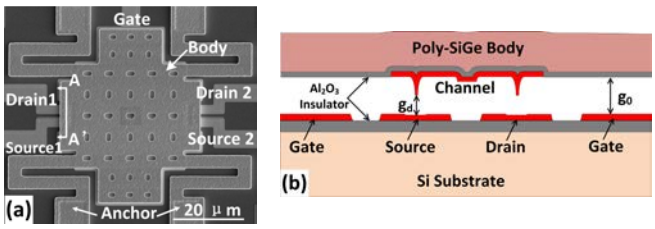

Fig. 1. (a) Plan-view SEM image of the fabricated 6-T logic relay used in this work; (b) Schematic cross-sectional view along the cut-line A-A′.

The minimum switching energy (E_{min}) of the relay is proportional to the contact adhesive force (F_{adh}) [8], because it determines the minimum F_{spring} required to turn OFF the relay; in turn, $F_{elec} \geq F_{spring}$ is required to turn ON the relay. F_{spring} is tuned by adjusting the beam deflection in the ON state, *i.e.* the as-fabricated dimpled contact gap thickness (g_d), and/or the effective spring constant (k_{eff}) of the beams; F_{elec} is tuned by adjusting the actuation area (A_{ACT}) and the as-fabricated actuation gap thickness (g_0). $E_{min} = 2F_{adh}g_d$ when $k_{eff} = F_{adh}/g_d$ and $g_0 = 1.5g_d$ [8]. Reductions in F_{adh} and g_d are constrained by process technology limitations because F_{adh} is dependent on the real contact area (A_C) as well as contact surface material properties. F_{adh} and g_d are sensitive to process-induced variations, which can cause a "stuck-ON" failure if $F_{adh} > k_{eff} \cdot g_d$. Thus, k_{eff} should be designed to be larger than the idealistic value of F_{adh}/g_d to attain high manufacturing yield, resulting in larger operating voltage and energy.

A non-zero body bias voltage can be applied to reduce the gate voltage swing required to operate a relay [4] and hence its switching energy. If $V_B = -V_{RL}$, V_G needs only to swing between 0 V and $V_{PI} - V_{RL}$, which is defined as the hysteresis voltage (V_H). In this letter, the tradeoff between relay switching energy and switching delay is investigated for the first time.

II. Experimental Results

6-T relays were fabricated using the process described in [9], with as-fabricated gap thicknesses $g_d = 135$ nm and $g_0 = 260$ nm. Measured current-*vs.*-voltage (I-V) characteristics are shown in Fig. 2(a). The values of V_{PI}, V_{RL} and V_H

Manuscript received April 8, 2015; revised May 31, 2015; accepted June 1, 2015. Date of publication June 3, 2015; date of current version July 22, 2015. This work was supported by the Directorate for Engineering through the National Science Foundation under Award 0939514. The review of this letter was arranged by Editor M. Tabib-Azar.

The authors are with the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA 94720 USA (e-mail: tking@eecs.berkeley.edu).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2015.2441116

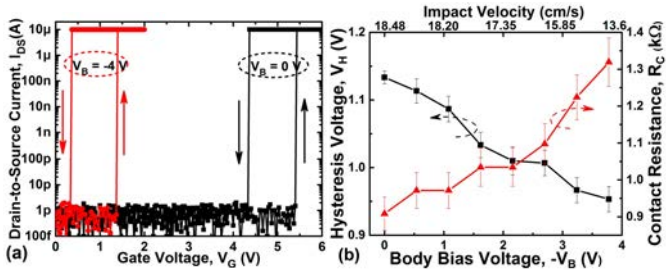

Fig. 2. (a) Measured relay *I-V* characteristics (I_{OFF} is at the noise floor while I_{ON} is limited by a current compliance limit); (b) Hysteresis voltage and contact resistance as a function of body bias voltage.

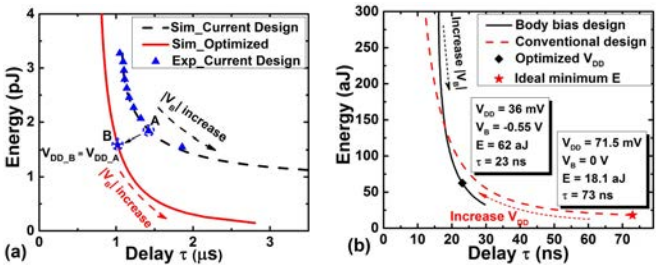

Fig. 3. (a) Energy-delay performance for the fabricated 6-T relay; (b) Simulated energy-delay performance for a scaled relay.

are 5.43 V, 4.3 V and 1.13 V, respectively, so that an applied gate voltage $V_G = 1.13$ V would be sufficient to turn on the relay when a body bias $V_B = -4.3$ V is applied. Interestingly, V_H decreases steadily with increasing $|V_B|$, and is reduced by approximately 0.2 V at $V_B = -4$ V. At the same time, the ON-state resistance, which is dominated by the contact resistance (R_C), was found to increase with $|V_B|$. The dependences of V_H and R_C on V_B are plotted in Fig. 2(b). These results can be explained as follows.

An electrostatically actuated switch can be modeled as a parallel-plate capacitor with a (time-dependent) plate separation gap (g) wherein the movable plate behaves as a simple oscillator [10]. The governing equation of motion is

$$m\ddot{g} + b\dot{g} - k\,(g_0 - g) = \frac{-\varepsilon A_{ACT}(V_G - V_B)^2}{2(g_0 - g)^2}, \qquad (1)$$

where b is the damping factor, m is the mass of the movable plate, and ε is the vacuum permittivity. Since the capacitive charging delay (*i.e.* the "*RC*" delay) of a relay is negligible compared to its mechanical switching delay [3], the input gate voltage signal can be approximated as a step function between 0 V and $V_{DD} = V_{PI} - |V_B|$ to numerically solve for the plate velocity at the moment when contact between the channel and source/drain electrodes is made. The parameter values used in the simulation are extracted from measurements of the fabricated relay: $k_{eff} = 78.5$ N/m, $A_{ACT} = 1584\ \mu m^2$, $m = 7.79$ ng, $g_0 = 260$ nm, $V_{GB} = 5.4$ V and $b = 0$ (in vacuum). The simulated values of impact velocity for various values of $|V_B|$ are indicated along the top of Fig. 2(b), and they show that the impact velocity decreases steadily with $|V_B|$. Higher impact velocity usually results in higher F_{adh} due to both physical and chemical surface changes [11]. Therefore the observed dependence of V_H on $|V_B|$ can be explained by decreasing F_{adh} with increasing $|V_B|$. The relatively small R_C at low $|V_B|$ (high impact velocity) indicates that there are more/stronger charge conduction paths formed in the ON state due to either increased contact area or more metallic bonds, which coincides with larger F_{adh} and V_H.

Since the impact velocity decreases with body bias, it is natural to inquire how the turn-ON delay (τ) of a relay changes with body biasing. Fig. 3(a) shows the relationship between switching energy and delay. The triangular symbols represent experimental data for different values of $|V_B|$ with the same value of V_{GB} (= V_{PI}). As $|V_B|$ increases (and V_{DD} decreases), τ increases because the average velocity decreases more quickly than the initial contact dimple gap thickness. The switching energy is calculated as follows:

$$E = V_{PI}(C_{ON}V_{PI} - C_{OFF}|V_B|) = \frac{\varepsilon A_{ACT}}{g_0 - g_d}V_{PI}^2 - \frac{\varepsilon A_{ACT}}{g_0 - g_x}V_{PI}|V_B|, \qquad (2)$$

where g_x is the top plate displacement for $V_G = 0$ V. The dashed line in Fig. 3(a) is the calculated energy-delay curve, which can be seen to match the experimental results very well. By increasing $|V_B|$ from 0 V to 4.3 V, E decreases by 44% while τ increases by 32%. The maximum value of $|V_B|$ for proper relay operation is equal to V_{RL}. The fact that V_{RL} increases with $|V_B|$ (due to reduced F_{adh}) is beneficial for minimizing the switching energy of a logic relay by body biasing.

III. Discussion

To further improve the energy efficiency of a relay, design optimization is necessary. From (2) it can be seen that E can be reduced by making the OFF-state gate capacitance (C_{OFF}) approach the ON-state gate capacitance (C_{ON}), *i.e.* by reducing the initial ($V_G = 0$) contact dimple gap thickness $g_d - g_x$ to be nearly zero. This is not possible, however, unless the relay is designed to operate in non-pull-in mode, *i.e.* $g_d \le g_0/3$ [12]. The solid line in Fig. 3(a) is the calculated energy-delay curve for a relay that is identical to the fabricated device except with $g_0 = 3g_d = 405$ nm instead of 260 nm. It can be seen that the energy-delay trade-off is significantly improved for this theoretical design, even though it has a larger value of V_{PI} (10.5 V). For comparison, one point on each curve in this figure is highlighted, for the same gate operating voltage ($V_{DD} = 1.1$ V). Although a larger body bias voltage is required for design B, this does not directly affect the dynamic power consumption of a relay-based circuit since the body does not conduct current.

The simulated energy-delay curves for aggressively scaled relays with $g_d = 5$ nm, $A_{ACT} = 1\ \mu m^2$, and structural poly-SiGe layer thickness $t = 30$ nm are shown in Fig. 3(b). F_{adh} is assumed to be 1.81 nN, which corresponds to electrodes coated with an ultra-thin (3 Å) layer of TiO_2 and real contact area $A_C = 1\ nm^2$ [13]. The conventional (idealistic) design for minimum switching energy ($E_{min} = 2F_{adh}g_d$) requires $g_0 = 1.5g_d = 7.5$ nm and $k_{eff} = F_{adh}/g_d = 0.362$ N/m [8]. The energy and delay for minimum voltage operation ($V_{DD} = V_{PI}$) are indicated by the star symbol

TABLE I
NEM RELAY DESIGN PARAMETERS AND ENERGY-DELAY PERFORMANCE

Designs		Design Parameters					Simulated Performance			
		Constraints			Knobs					
		g_d (nm)	F_{adh} (nN)	A_{ACT} (μm^2)	g_0 (nm)	k_{eff} (N/m)	$\lvert V_B \rvert$ (mV)	V_{DD} (mV)	E (aJ)	τ (ns)
Idealistic		5	1.81	1	7.5	0.362	0	72	18.1	73
Relaxed	w/o V_B	5	1.81	1	15	3	0	582	300	16
	w/ V_B	5	1.81	1	15	3	546	36	62	23

in Fig. 3(b). To improve the switching speed, V_{DD} must be increased at a trade-off of increased switching energy, as indicated by the dashed curve in Fig. 3(b).

The body-biased relay design has more relaxed values of g_0 and k_{eff}: $g_0 = 15$ nm is chosen so that the relay operates in non-pull-in mode; $k_{eff} = 3$ N/m is chosen to avoid the possibility of stuck-ON failure. This design eases manufacturing challenges and can provide for reduced device footprint, since shorter suspension beams can be used. The solid curve in Fig. 3(b) shows how the switching energy is reduced by increasing $|V_B|$, at a relatively small penalty of increased switching delay. The maximum value of body bias that can be applied is

$$V_{RL} = \sqrt{\frac{2(kg_d - F_{adh})(g_0 - g_d)^2}{\varepsilon A_{ACT}}} = 546 \text{ mV}. \quad (3)$$

The energy and delay for minimum gate voltage operation ($V_{DD} = V_{PI} - |V_B| = V_{PI} - V_{RL}$) are indicated by the diamond symbol in Fig. 3(b).

The key design parameters and simulated performance parameters for the two nano-electro-mechanical (NEM) relay designs are compared in Table I. The performance of the relay with relaxed g_0 and k_{eff} but without body biasing (*i.e.* for $V_B = 0$ V) is included for comparison. It can be seen that the body-biased relay design provides for the lowest gate operating voltage and better energy efficiency at 23 ns delay, as compared to the idealistic relay design for operation with the theoretical minimum switching energy. Considering that interconnect and parasitic capacitances may be comparable to or even larger than the intrinsic capacitance of a NEM relay, lower-voltage operation ultimately may provide for more energy efficient relay-based integrated circuits. With body biasing, it is possible to maintain a low gate operating voltage while further scaling down A_{ACT} to reduce the device footprint.

IV. CONCLUSION

Body biasing can be used to tune the trade-off between switching energy and turn-ON delay for a logic relay. In comparison with a relay designed for minimum energy operation, a relay designed for low-voltage operation with an applied body bias voltage can relax manufacturing process requirements and provide for improved energy-delay performance.

REFERENCES

[1] S. Hanson *et al.*, "Ultralow-voltage, minimum-energy CMOS," *IBM J. Res. Develop.*, vol. 50, nos. 4–5, pp. 469–490, Jul. 2006.

[2] B. H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in subthreshold circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1778–1786, Sep. 2005.

[3] F. Chen *et al.*, "Integrated circuit design with NEM relays," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design*, Nov. 2008, pp. 750–757.

[4] R. Nathanael *et al.*, "4-terminal relay technology for complementary logic," in *IEDM Tech. Dig.*, Dec. 2009, pp. 1–4.

[5] J. Fujiki *et al.*, "Microelectromechanical relay and logic circuit design for zero crowbar current," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3296–3302, Sep. 2014.

[6] N. Xu *et al.*, "Hybrid CMOS/BEOL-NEMS technology for ultra-low-power IC applications," in *IEDM Tech. Dig.*, Dec. 2014, pp. 28.8.1–28.8.4.

[7] T.-J. K. Liu *et al.*, "NEM relay design for compact, ultra-low-power digital logic circuits," in *IEDM Tech. Dig.*, Dec. 2014, pp. 13.1.1–13.1.4.

[8] H. Kam *et al.*, "Design, optimization, and scaling of MEM relays for ultra-low-power digital logic," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 236–250, Jan. 2011.

[9] R. Nathanael *et al.*, "Multi-input/multi-output relay design for more compact and versatile implementation of digital logic with zero leakage," in *Proc. Int. Symp. VLSI Technol., Syst., Appl. (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 2012, pp. 1–2.

[10] J. C. Blecke *et al.*, "A simple learning control to eliminate RF-MEMS switch bounce," *J. Microelectromech. Syst.*, vol. 18, no. 2, pp. 458–465, Apr. 2009.

[11] H. Xiang and K. Komvopoulos, "The effect of impact velocity on interfacial adhesion of contact-mode surface micromachines," *Appl. Phys. Lett.*, vol. 101, no. 5, p. 053506, 2012.

[12] J. Yaung *et al.*, "Adhesive force characterization for MEM logic relays with sub-micron contacting regions," *J. Microelectromech. Syst.*, vol. 23, no. 1, pp. 198–203, Feb. 2014.

[13] C. Pawashe, K. Lin, and K. J. Kuhn, "Scaling limits of electrostatic nanorelays," *IEEE Trans. Electron Devices*, vol. 60, no. 9, pp. 2936–2942, Sep. 2013.