Dual-Gated MoS_2/WSe_2 van der Waals Tunnel Diodes and Transistors

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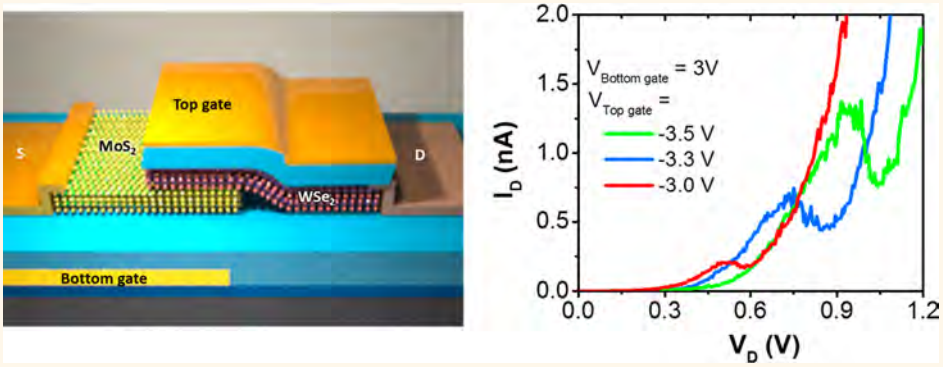
ABSTRACT



Two-dimensional layered semiconductors present a promising material platform for band-to-band-tunneling devices given their homogeneous band edge steepness due to their atomically flat thickness. Here, we experimentally demonstrate interlayer band-to-band tunneling in vertical MoS_2/WSe_2 van der Waals (vdW) heterostructures using a dual-gate device architecture. The electric potential and carrier concentration of MoS_2 and WSe_2 layers are independently controlled by the two symmetric gates. The same device can be gate modulated to behave as either an Esaki diode with negative differential resistance, a backward diode with large reverse bias tunneling current, or a forward rectifying diode with low reverse bias current. Notably, a high gate coupling efficiency of ~80% is obtained for tuning the interlayer band alignments, arising from weak electrostatic screening by the atomically thin layers. This work presents an advance in the fundamental understanding of the interlayer coupling and electron tunneling in semiconductor vdW heterostructures with important implications toward the design of atomically thin tunnel transistors.

KEYWORDS: transition metal dichalcogenide · electron tunneling · negative differential resistance · TFET · steep · 2D

Scaling of the metal-oxide-semiconductor field-effect transistors (MOSFETs) in the IC industry for over 5 decades and 16 technology nodes has been driven in parallel with the reduction of the operating voltage to balance out the power dissipation and consumption of the electronic systems. The inadequate scaling of operating voltage, V_{DD}, with increasingly diminishing technology node, however, has led to power consumption issues recently as the MOSFETs approach their minimal V_{DD}, which is governed by their switching mechanism. Specifically, the carrier injection in MOSFETs is based on thermionic emission over the energy barrier at the source, which theoretically limits the MOSFETs' subthreshold swing to SS ≈ 60 mV/dec at room temperature and places a floor for threshold voltage scaling as well. In order to maintain a minimum I_{ON}/I_{OFF} of ~10^6, the supply voltage is thus limited to about 6 × 60 mV, corresponding to $V_{DD} \approx 360$ mV in the most optimistic case. In reality, SS for state-of-the-art MOSFETs is larger than the theoretical limit, and furthermore, to obtain sufficiently high ON-state currents for fast switching operations, a higher V_{DD} needs to be applied. This supply voltage limitation of MOSFETs represents an important challenge

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facing the IC industry given the continued increase in transistor density. Therefore, exploring new switching mechanisms is of fundamental interest for future energy-efficient electronics. One promising alternative switch to a MOSFET is a tunneling field-effect transistor (TFET), where carrier injection is governed by band-to-band tunneling (BTBT) of electrons, which does not depend on thermal processes.[1] Thus, in principle, SS < 60 mV/dec should be achievable with TFETs. To date, significant progress has been made in exploring a wide range of TFET device architectures using carbon nanotubes[2] and Si,[3] Si–Ge,[4] and III–V semiconductors.[5−7] Both homojunction and heterojunction device configurations have been explored, with the heterojunction devices exhibiting higher ON-state current densities due to the ability to obtain sufficiently small (or even zero) tunneling barrier heights by using materials with proper band alignments.[8] Despite tremendous advancements in the field, to date a TFET with SS < 60 mV/dec over multiple current decades and high ON-state current densities has not been demonstrated experimentally. Various studies have shown that the band edge roughness of the explored semiconductors in combination with the trap states at the surface and heterojunction interfaces are limiting the switching steepness of the experimental devices.[9] Specifically, imperfections at the tunneling interface due to lattice mismatch and spatial inhomogeneity in thickness and composition can reduce the sharpness of the band edges. In addition, doping is known to further reduce band edge sharpness given the random distribution of the dopant atoms in the lattice. To overcome these fundamental limitations, exploration of new material systems is required. For instance, transition metal dichalcogenides (TMDCs), a family of two-dimensional layered materials, show promise toward obtaining steep band edge tunneling devices, since they intrinsically exert atomic level flatness due to their layered crystal structure.[10,11] The ability to stack one two-dimensional material onto another can create an atomically sharp interface, without any unwanted atomic diffusion or dislocation propagation due to lattice mismatch.[12] The absence of dangling bonds and a surface native oxide (for the TMDCs investigated in this work)[13−15] allows for the formation of ultrathin vertical heterostructures with minimal trap states. Sharpness of the band edges in MoS_2 and WSe_2 monolayers as well as MoS_2/WSe_2 heterobilayers has been previously reported by using photoluminescence measurements. A nearly identical inverse slope of 30 mV/dec was reported from the analysis of the band tails of monolayers and heterobilayers, signifying that sharp band edges can be experimentally obtained in van der Waals (vdW) heterostructures.[13] Given this measured optical band edge sharpness, it is feasible to envision that tunneling devices with SS ≈ 30 mV/dec should be, in principle, possible when using vdW heterostructures. However, before the realization of tunnel transistors using TMDC heterostructures, band-to-band tunneling and its fundamental properties in these vdW materials need to be explored.

Electronic and optoelectronic properties of vdW heterostructures, based on graphene, h-BN, and TMDCs have been studied extensively in the recent past. For instance, graphene–insulator–graphene heterostructures have exhibited interlayer tunneling with negative differential resistance (NDR).[16,17] While demonstrating the feasibility of vertical tunneling of electrons in vdW heterostructures, graphene-based tunnel devices cannot be effectively turned off due to the lack of an intrinsic band gap. In the past year, significant research has been carried out on MoS_2/WSe_2 heterostructures.[13,18−21] Artificially stacked exfoliated monolayer MoS_2/WSe_2 heterostructures exhibit a Stokes-like shift in the photoluminescence peak and the lowest absorption peak, suggestive of a spatially direct absorption and spatially indirect emission in a type II band alignment with strong interlayer electronic coupling.[13,21] These heterostructures exhibit rectifying diode behavior, with rectification of 4 orders of magnitude in the forward bias current, which can be gate controlled.[13,21] However, a detailed study to investigate vertical BTBT in TMDC-based heterojunctions has not been reported, and it is yet unknown as to whether an efficient BTBT current density can be obtained in TMDC vdW devices. In theory, by electrostatically tuning the band alignment from type II to type III (broken gap), vertical tunneling of electrons from the valence band of one layer to the conduction band of another can be initiated.[22] Tunneling junctions and the realization of a Zener diode, whose reverse bias breakdown is caused by BTBT, are the first steps toward eventual fabrication of a TFET. In addition to their use as the building block of TFETs, Zener diodes are commonly used in analog circuits due to their high nonlinearity. Thus, exploration and characterization of Zener diodes based on TMDC heterostructures is of tremendous scientific and technological interest.

In this work, dual-gated MoS_2/WSe_2 heterostructure tunnel diodes and transistors are examined experimentally and theoretically. The electrostatic potential and carrier concentration of MoS_2 and WSe_2 layers are independently controlled by two separate gate electrodes. Symmetric dual-gate device architecture is essential, compared to single-gate or asymmetric dual-gate structures, in order to effectively control the band alignment at the vertical heterojunction by independently modulating the electric potential in both top and bottom layers. In the case of single-gate or asymmetric dual-gate structures, the electric field from one gate dominates the potential of both layers, resulting in poor controllability of the heterojunction. Selective electron and hole contacts are made to MoS_2 and WSe_2 layers, respectively. By using this device

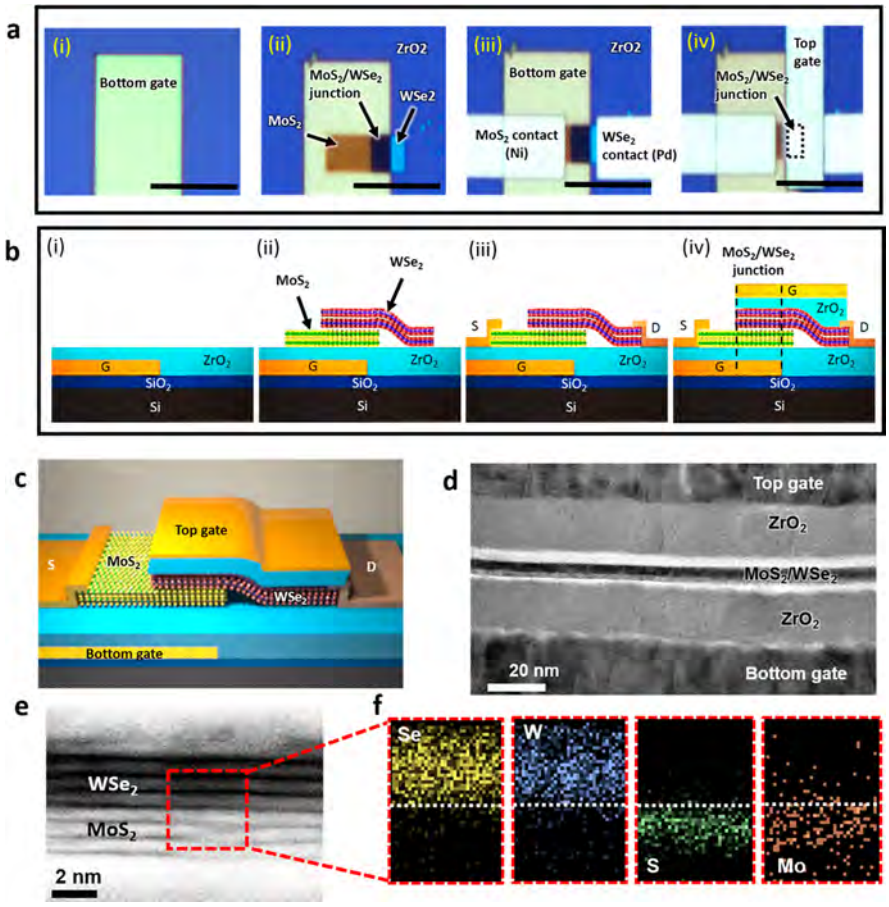

Figure 1. Device structure. (a) Optical microscope images and (b) corresponding schematics (not to scale) for the fabrication process steps of a representative dual-gated MoS_2/WSe_2 diode. (i) Local bottom gate electrode with Ni as the metal electrode and ZrO_2 as the gate dielectric. (ii) MoS_2 and WSe_2 layers dry-transferred onto the bottom gate and etched to form a rectangular heterostructure. (iii) Metal contacts to MoS_2 (Ni) and WSe_2 (Pd) deposited, as source and drain electrodes, respectively. (iv) Top-gate stack with ZrO_2 as the gate dielectric and Ni metal as the electrode. Scale bar = 10 μm in all optical images. (c). Three-dimensional schematic of the device (not to scale). (d) Cross-sectional TEM image of a representative device showing the symmetric dual-gate structure. (e) High-resolution STEM image of the same heterostructure, consisting of 4 layers of MoS_2 and WSe_2. (f) EDS mapping of the heterostructure.

structure, Zener tunneling is observed in the reverse bias, when the two gates are biased at opposite polarities such that the MoS_2 and WSe_2 layers are in strong electron and hole accumulation modes, respectively. Under such a circumstance, the device resembles an n+/p+ diode with a large built-in potential, V_{bi}, operating as a backward diode. Some of the devices also exhibit negative differential resistance in the forward bias, indicative of Esaki diode character and a broken gap (type III) band offset. When the same device is subjected to lower gate fields, the band offset at the heterojunction is changed to a staggered gap (type II), resulting in lower reverse bias tunneling currents and higher forward bias diffusion current due to reduced V_{bi}. Thus, the same device is shown to behave in various diode regimes, merely by tuning the gate voltage, a phenomenon unseen in covalently bonded semiconductor material systems. This controllability of the diode operation regime was observed in six fabricated devices, with nearly identical thickness of MoS_2 and WSe_2 components ranging from 2 to 8 layers. In conventional semiconductor devices, the same device cannot behave as both forward rectifying and backward/tunnel diodes, since they require different chemical doping conditions. Another fundamental difference in the material properties of vdW heterostructures compared to conventional semiconductor heterostructures is in the bonding at the tunneling interface. Heterostructures of III–V compounds and Si–Ge have covalent bonding at the interface that pins the band offsets at the tunneling interface, irrespective of the doping level and the applied voltage, unless an insulator layer is grown in between the layers. In contrast, in the vdW heterostructures, potential can be dropped across the vdW gap, thus allowing the bands of the two material components to freely move with respect to each other at the junction by the applied drain voltage or electrostatic doping by the two gates. Therefore, vdW heterostructures provide a new degree of freedom in terms of modulation of the band offsets at the tunneling interface.

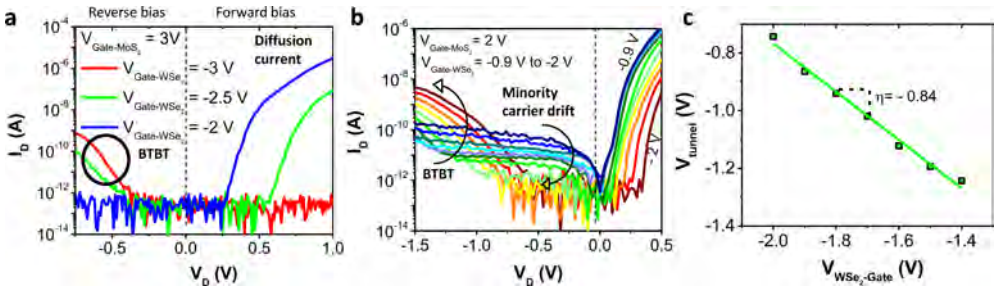

Figure 2. Gate tunability of a representative dual-gated device at 77 K. MoS_2 is 8−10 layers in thickness, and WSe_2 is 6−8 layers thick as confirmed from AFM measurements. (a) I_D-V_D with varying $V_{Gate\text{-}WSe2}$; $V_{Gate\text{-}MoS2}$ = 3 V. (b) I_D-V_D with $V_{Gate\text{-}WSe2}$ varied with 0.1 V increments from −2 V to −0.9 V; $V_{Gate\text{-}MoS2}$ = 2 V. (c) Tunneling onset voltage vs $V_{Gate\text{-}WSe2}$, with the slope representing the gate coupling efficiency η.

Figure 1 shows the fabrication process and corresponding optical images of a dual-gated MoS_2/WSe_2 tunnel diode. A local back gate was fabricated (see Methods), as shown in Figures 1a(i) and b(i). MoS_2 flakes were mechanically exfoliated onto a Si/SiO_2 carrier chip. The carrier chip was spin coated with PMMA. The MoS_2 flake of interest was dry-transferred onto the targeted local back gate using a previously reported pick and transfer process.[23] The sample was annealed at 180 °C for 2 min to ensure proper adhesion of the flake to the substrate. The PMMA layer was removed by using dichloromethane, leaving the flake attached to the local back gate. A WSe_2 flake was transferred on top of the MoS_2 layer using the same transfer method. WSe_2 was aligned over MoS_2 in such a way as to avoid overlap in the edge regions, in order to allow for selective electrical contacts to each layer. The heterojunction (*i.e.*, overlap region) is therefore only in the middle of the flake. The rectangular heterostructure shape was defined *via* electron beam lithography and etched using XeF_2 gas.[24] This shape formation is important for eliminating unwanted current paths such as those from nonoverlapping MoS_2/WSe_2 regions along the width of the device (Figure 1a(ii) and b(ii)). Ni electrodes were patterned as electron contacts to MoS_2. Special attention is drawn to the fact that Ni does not contact WSe_2 or the heterostructure. Pd electrodes were then patterned to act as hole contacts to WSe_2. The fabricated structure with the contacts is shown in Figure 1a(iii) and b(iii). A top gate stack was then patterned on the heterostructure area. The device is designed such that the bottom and top gates overlap the heterostructure area in the middle of the device. The bottom gate also overlaps the electron contact to the MoS_2 layer, while the top gate overlaps the hole contact to WSe_2 in order to minimize the parasitic resistances in the device. Figure 1a(iv) shows the optical image of a representative dual-gate MoS_2/WSe_2 device. The heterostructure area is defined by the overlapped region of the bottom and the top gates, as shown in the schematic of Figure 1b(iv). Figure 1c shows the corresponding three-dimensional schematic of the complete device. A cross-sectional transmission electron microscope (TEM) image of a representative device is shown in Figure 1d, clearly depicting the symmetric dual-gate structure. The high-resolution scanning TEM (STEM) image of the MoS_2/WSe_2 heterostructure (Figure 1e) shows a sharp and clean interface between MoS_2 and WSe_2, with each material being ∼4 atomic layers in thickness. Figure 1f shows the energy-dispersive X-ray spectroscopy (EDS) mapping of the heterostructure. The top 4 layers are composed of W and Se, while the bottom layers are composed of Mo and S. Figure S1 shows the Raman spectra from the MoS_2/WSe_2 heterostructure in a dual-gated device.

RESULTS AND DISCUSSION

The fabricated devices were electrically characterized at different temperatures and under different drain and gate voltages. Figure 2a shows the operation of a dual-gated MoS_2/WSe_2 heterostructure diode at 77 K. The MoS_2/WSe_2 heterostructure for this device consists of 8−10 layers of MoS_2 and 6−8 layers of WSe_2 as measured by atomic force microscopy (AFM). The MoS_2/WSe_2 heterostructure area is 2.8 μm^2. The I_D-V_D of the diode is shown as a function of varying WSe_2 gate voltage, $V_{Gate\text{-}WSe2}$, while keeping the MoS_2 gate voltage, $V_{Gate\text{-}MoS2}$, constant at 3 V (Figure 2a). At $V_{Gate\text{-}MoS2}$ = 3 V, the MoS_2 layer is electrostatically rendered highly n-type, due to strong accumulation of electrons. When $V_{Gate\text{-}WSe2}$ = −2 V, the WSe_2 layer can be assumed to be in a condition of weak accumulation of holes. The device resembles an n+/p diode with a staggered gap band offset. Under this condition, the diode demonstrates the expected rectification in the forward bias due to diffusion current, with low reverse bias current limited by the noise floor of the measurement setup. A forward to reverse current rectification of 7 orders of magnitude is observed. When $V_{Gate\text{-}WSe2}$ is decreased to −2.5 V, the WSe_2 layer is further accumulated with holes. In this situation, V_{bi} of the diode increases, resulting in lower forward bias current for the same drain voltage conditions as in the previous case. A significant reverse bias current arises at V_D < −0.5 V and is due to Zener tunneling of

electrons in the valence band of WSe_2 to the conduction band of MoS_2. Upon further decrease of $V_{Gate\text{-}WSe2}$ to −3 V, the accumulation of holes in WSe_2 increases further. In this case, the device resembles an n+/p+ diode, and the forward bias current diminishes below the noise floor of the measurement setup, due to increased V_{bi}, for the same drain voltage range (1 V) used in the previous two cases. The reverse bias current is increased and is 4 orders of magnitude larger than the forward current, which is at the noise level. The device behaves like a backward diode, where the reverse bias current due to Zener tunneling is larger than the forward bias current for the applied drain voltage range of −0.75 to 1 V. Thus, we demonstrate a four-terminal diode whose operation regimes are highly controllable by its dual gates, without the application of any physical dopant. Similar tunability of operation regimes of a MoS_2 (bilayer)/WSe_2 (bilayer) device is shown in Figure S2.

It is important to understand the efficiency of gate control in moving the band edges of MoS_2 and WSe_2 at the heterointerface. In order to elucidate the gate control electrostatics on the device behavior, Figure 2b shows the tunability of the same device at $V_{Gate\text{-}WSe2}$ varying from −0.9 to −2 V with an increment of 100 mV at 77 K. $V_{Gate\text{-}MoS2}$ is kept at a constant voltage of 2 V, resulting in the accumulation of electrons in MoS_2. The device exhibits Zener tunneling (marked "BTBT" in Figure 2b) in the reverse bias, and the tunneling onset voltage shifts to more negative V_D as $V_{Gate\text{-}WSe2}$ is made less negative. Simultaneously, the minority carrier drift current, often referred to as the reverse bias saturation current, I_0, increases as $V_{Gate\text{-}WSe2}$ is made less negative. This behavior is expected since the minority (majority) carrier concentration in WSe_2 is decreased (increased) as higher gate fields are applied to WSe_2. The device operates like a classical diode when the chemical doping concentrations of the two components are changed. Here, moreover, the same device can be readily modulated to exhibit different carrier concentrations by tuning the two gate voltages. Figure 2c shows the reverse bias tunnel onset voltage (*i.e.*, tunneling breakdown voltage), V_{tunnel}, as a function of $V_{Gate\text{-}WSe2}$. V_{tunnel} is defined as the voltage at which a tunnel current of 10^{-11} A is measured. The slope of V_{tunnel} vs $V_{Gate\text{-}WSe2}$ gives the gate coupling factor or the gate efficiency η (Figure 2c). It signifies that for each volt applied to the gate, the Fermi level can be moved by 0.84 V. This high gate efficiency arises from the use of high-k gate dielectrics and thin MoS_2 and WSe_2 layers. We observe saturation in the reverse bias tunneling current and the forward bias current due to the large parasitic resistance of the contacts, especially for WSe_2, since the contact regions were not doped.[25−27] This large parasitic resistance also lowers the steepness of the BTBT current in our fabricated diodes. In the future, doping of contacts needs to be explored for lower parasitic resistances.

A phenomenological device model is developed to further understand the gate-bias-dependent diode characteristics (Figure 3). Electrostatic potential for each TMDC layer is obtained by solving the carrier statistics equations self-consistently with the Poisson equation in the form of a capacitance model, which is described in a previous work on vertical tunneling transistors.[28] Then, two mechanisms are taken into account in source−drain current calculation for interlayer carrier transport. The first one is an elastic process at the interface, including the direct tunneling and thermionic emission, which is shown as path I in Figure 3b. The current generated by this process can be described by[16]

$$J_e = \frac{\alpha q}{\hbar}\int D_{MoS_2}(E - qV_{MoS_2})D_{WSe_2}(E - qV_{WSe_2}) \times [f_{WSe_2}(E) - f_{MoS_2}(E)]\,dE \quad (1)$$

where D_{MX2} is the density of state (DOS) for each TMDC and f_{MX2} is the source/drain Fermi level. V_{MoS2} and V_{WSe2} are electrostatic potentials of the MoS_2 and WSe_2 layer, which account for both gate and drain bias and can be solved self-consistently as described before. $\hbar$ is the reduced Planck's constant, q is electron charge, and α is a fitting parameter that is related to the elastic transport time as $\tau_1 = \hbar/(\alpha D_{MX2})$. For simplicity, the DOS in the conduction or valence band is assumed to be constant, which is similar to previous studies on tunneling devices.[14] The band tail states whose DOS exponentially decay as a function of the difference between the energy E and the band edge energy are included in the band gap.

Besides this elastic process, there is also an inelastic interlayer carrier recombination process. Different from a conventional PN junction, the atomically thin junction does not have any depletion region in the vertical direction. Thus, the majority of holes in WSe_2 are in direct contact with the majority of electrons in MoS_2, separated by only a vdW gap. As a result, the interlayer majority carrier recombination is pronounced.[13,21] This inelastic process can be either photon or phonon assisted. We refer to this inelastic process as current path II, as illustrated in the schematic of Figure 3b. Simply, we adapted a second transport time of the carrier, τ_2, which is the interlayer recombination lifetime, to account for the inelastic process, so that the current can be estimated by

$$J_{ine} = q\frac{np - n_0p_0}{\tau_2(n+p)} \quad (2)$$

where n and p are the electron and hole density of adjacent MoS_2 and WSe_2 layers, and n_0 and p_0 are electron and hole density at equilibrium conditions. As described in a previous study,[21] eq 2 assumes the

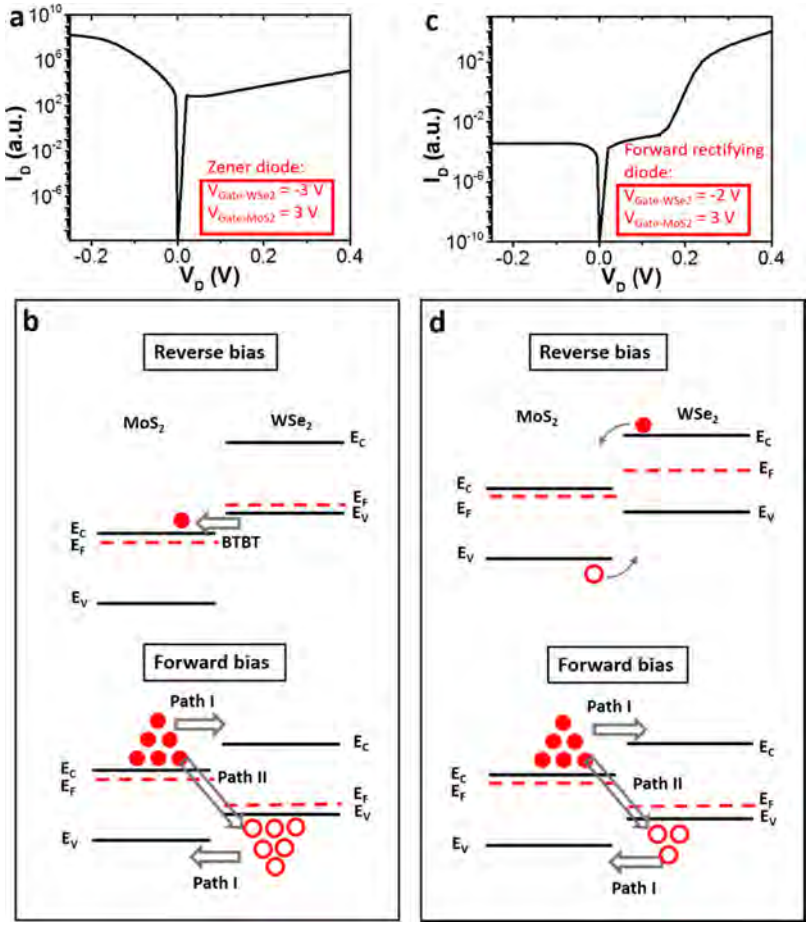

Figure 3. (a) Simulated I_D-V_D characteristics of a MoS_2/WSe_2 (2 layers each) diode at $V_{Gate\text{-}MoS2}$ = 3 V and $V_{Gate\text{-}WSe2}$ = −3 V, at 77 K. (b) Corresponding qualitative band diagrams at forward and reverse biases. (c) Simulated I_D-V_D characteristics of the diode at $V_{Gate\text{-}MoS2}$ = 3 V and $V_{Gate\text{-}WSe2}$ = −2 V, at 77 K. (d) Corresponding qualitative band diagrams at forward and reverse biases.

Shockley Read Hall (SRH) mechanism for interlayer majority carrier recombination, and an assumption of the Langevin mechanism results in a different quantitative equation but does not change the qualitative conclusions. Finally, the total current conducted by the PN junction is the addition of these two processes, $J = J_e + J_{ine}$. Figure 3a and c show the simulated I_D-V_D characteristics of a bilayer/bilayer diode under two different gate voltage conditions, with $\tau_2/\tau_1 = 1$. At high gate overdrive voltages (Figure 3a), both the MoS_2 and WSe_2 layers remain accumulated even when a moderate reverse bias is applied. As a result, Zener tunneling takes place through band edge states or the band tail states in the band gap region very close to the band edge. The reverse bias current is contributed by Zener tunneling and is nonsaturating. In comparison, at a lower top gate overdrive voltage (Figure 3c), the WSe_2 layer becomes depleted as a reverse bias is applied. The depletion leads to a saturated reverse bias current. The results indicate that the operation modes of the diode can be modulated by the applied gate voltage, qualitatively consistent with the experiment. The quantitative difference can be attributed to us ignoring the parasitic resistance and noise in simulations and the uncertainty of the material and device parameters. The following parameters were used in the simualtions: in Figure 3a, $n_0 = 1.01 \times 10^{13}$ m^{-3}, $p_0 = 2.91 \times 10^{11}$ m^{-3}, while in Figure 3c, $n_0 = 3.15 \times 10^{14}$ m^{-3}, with $n_0 \gg p_0$. Figure S3a,b show the simulated band diagrams for a MoS_2 (bilayer)/WSe_2 (bilayer) device, indicating the influence of the gate on each layer.

We measured the diode characteristics as a function of temperature in order to further analyze the dual-gated MoS_2/WSe_2 heterostructure (Figure 4). Here, the device consists of a MoS_2/WSe_2 stack with each material being 2 layers in thickness. The MoS_2/WSe_2 overlap area is 18 μm^2. To obtain backward diode characteristics, the device was biased with $V_{Gate\text{-}MoS2}$ = 3.5 V and $V_{Gate\text{-}WSe2} = -4$ V, and the corresponding I_D-V_D characteristics are shown in Figure 4a. The tunnel current onset voltage shifts positively with increasing temperature, which is a characteristic of the Zener tunneling processing due to the change in the band gap (and band tail states) with temperature. The tunnel current onset voltage, V_{tunnel}, is defined as the voltage with the reverse bias tunnel current of 10^{-13} A. The slope of V_{tunnel} vs T is the temperature

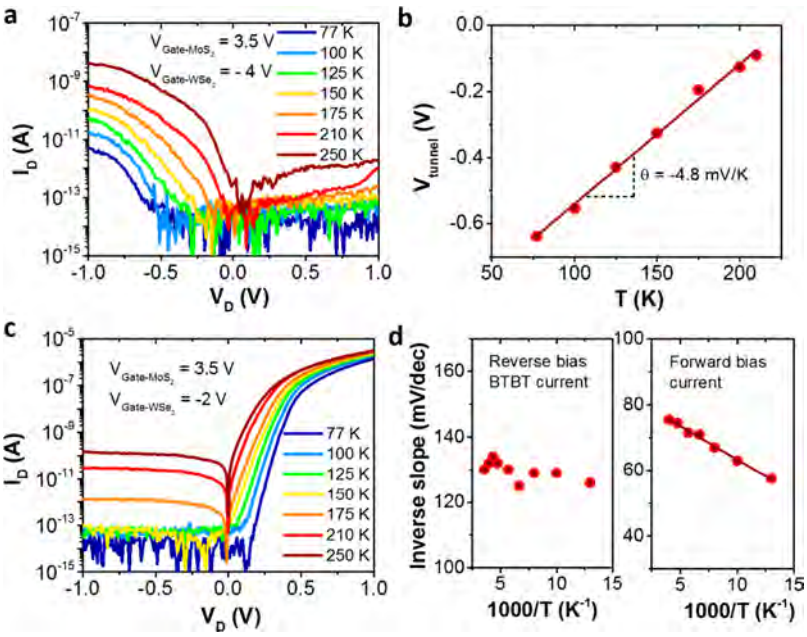

Figure 4. (a) Temperature dependence of the tunnel current at $V_{Gate\text{-}MoS2}$ = 3.5 V and $V_{Gate\text{-}WSe2}$ = −4 V of a device. MoS_2 and WSe_2 are 2 layers each in thickness for this device. (b) Tunneling onset voltage vs temperature at $V_{Gate\text{-}MoS2}$ = 3.5 V and $V_{Gate\text{-}WSe2}$ = −4 V. (c) Temperature dependence of the forward diode current at $V_{Gate\text{-}MoS2}$ = 3.5 V and $V_{Gate\text{-}WSe2}$ = −2 V. (d) Inverse slopes of the BTBT current ($V_{Gate\text{-}MoS2}$ = 3.5 V and $V_{Gate\text{-}WSe2}$ = −4 V) and forward bias current ($V_{Gate\text{-}MoS2}$ = 3.5 V and $V_{Gate\text{-}WSe2}$ = −2 V) vs inverse temperature.

coefficient of tunneling breakdown, θ, in the MoS_2/WSe_2 materials system, which is measured to be −4.8 mV/K (Figure 4b). This temperature coefficient is similar in value to a typical Si Zener diode, which has a reported coefficient of −2 to −3 mV/°C.[29] The temperature dependence of the forward rectifying characteristics, corresponding to lower applied gate fields, of the same device is shown in Figure 4c. The built-in potential, V_{bi}, decreases with increasing temperature, and the slope of the forward bias current decreases slightly with temperature. The reverse bias current for this diode configuration increases with temperature as the recombination−generation current increases. Figure 4d shows the inverse slope, in mV/dec, of the tunnel current for the backward diode configuration and the forward current for the forward-rectifying diode configuration as a function of inverse temperature. The inverse slope of the tunnel current remains nearly constant with temperature, as expected for Zener tunneling. The inverse slope of the forward current decreases slightly with inverse temperature. This is in contrast to a covalently bonded p−n junction, where the forward bias current is dominated by diffusion of majority carriers with its inverse slope changing linearly with T. The lack of strong temperature dependence in the forward bias current suggests that an inelastic current mechanism (path II in Figure 3b) dominates the forward bias current over the diffusion current. This is consistent with previous photoluminescence studies, where the main exciton recombination was shown to be spatially indirect arising from the recombination of electrons in MoS_2 with holes in WSe_2.[13,21]

The carrier transport time, τ_2, described earlier for this inelastic process can vary across samples, due to the quality of the interface during device fabrication. If τ_2 is long compared to τ_1, the elastic tunneling (*i.e.*, BTBT) process can dominate over the inelastic recombination process in the forward bias. Figure 5 shows the electrical characteristics of another dual-gated MoS_2/WSe_2 device. The stack consists of 4 MoS_2 layers and 4 WSe_2 layers, with an overlap area of 4.6 μm^2. When $V_{Gate\text{-}MoS2}$ = 3 V and $V_{Gate\text{-}WSe2}$ = −3 V, the device exhibits negative differential resistance in the forward bias, as shown in Figure 5a, thus behaving like an Esaki diode. Both the NDR peak position and peak-to-valley ratio are controlled by the applied gate voltages. As $V_{Gate\text{-}WSe2}$ is made more negative, the NDR peak position shifts to higher positive voltage and the peak-to-valley ratio increases. The peak of the NDR signifies the position when the conduction band edge of MoS_2 is aligned with the valence band edge of WSe_2. By varying $V_{Gate\text{-}WSe2}$, the drain bias at which the MoS_2 conduction band edge and WSe_2 valence band edge are aligned is varied. Thus, the voltage position of the peak of the NDR as a function of $V_{Gate\text{-}WSe2}$ is an indicator of the gate coupling efficiency. A gate coupling efficiency of ∼80% is obtained (Figure 5b), which is consistent with the previous devices. It is worth noting that no correlation of observation of NDR with the flake thicknesses (for the explored thickness range of up to 10 layers) was observed in our experiments. A detailed investigation of device characteristics as a function of flake thicknesses and the corresponding band structures should be carried out in the future.

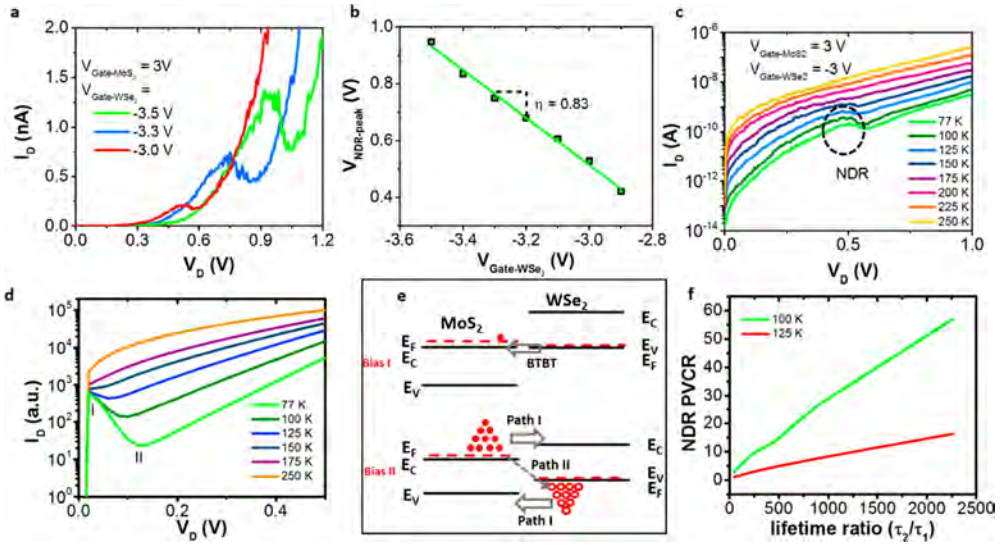

Figure 5. (a) I_D-V_D at $V_{Gate\text{-}MoS2}$ = 3 V and $V_{Gate\text{-}WSe2}$ varied. MoS_2 and WSe_2 are 4 layers each in thickness for this device. Negative differential resistance is observed at forward bias. (b) Voltage at which NDR peak occurs vs $V_{Gate\text{-}WSe2}$. (c) Temperature dependence of the NDR at $V_{Gate\text{-}MoS2} = -V_{Gate\text{-}WSe2}$ = 3 V. (d) Simulated temperature dependence of NDR at $V_{Gate\text{-}MoS2} = -V_{Gate\text{-}WSe2}$ = 3 V, by assuming a lifetime ratio of τ_2/τ_1 = 100. (e) Qualitative band diagrams corresponding to points I (NDR peak) and II (NDR valley) in (d). (f) Simulated NDR peak-to-valley current ratio (PVCR) vs inelastic to elastic carrier transport time ratio (τ_2/τ_1).

Figure 5c shows the temperature dependence of the NDR at $V_{Gate\text{-}MoS2}$ = 3 V and $V_{Gate\text{-}WSe2}$ = −3 V. The NDR diminishes after 175 K due to thermionic current suppressing the tunneling current in the forward bias. Figure 5d shows the simulated I_D-V_D characteristics at different temperatures, under a bias condition of $V_{Gate\text{-}MoS2}$ = 3 V and $V_{Gate\text{-}WSe2}$ = −3 V. A lifetime ratio of τ_2/τ_1 = 100 is assumed. The results show clear NDR behaviors at low temperature. At a low forward bias near equilibrium, an elastic carrier transport path, corresponding to BTBT, contributes to the current. As the applied forward bias increases, the elastic carrier transport path is closed with the overlap of the band edges diminishing, leading to an NDR characteristic. Similar to experiments, NDR is only observed at low temperatures. The simulated NDR is much more pronounced compared to the experimental I_D-V_D, even by considering a nonideal band edge with a decaying band gap state of 30 meV/decade.[13] To explain the lower peak-to-value ratio observed in the experiment, we further examine the role of the inelastic transport denoted as path II in Figure 3b. Decrease of the interlayer recombination time results in a more efficient path II, as shown in Figure 5e and increase of the valley current. As shown in Figure 5f, the simulated peak-to-valley current ratio is sensitive to the ratio of the carrier transport times of the inelastic interlayer transport process, τ_2, and the elastic interlayer carrier transport process, τ_1. A low peak-to-valley ratio of the NDR characteristics in the experimental device is, therefore, due to efficient interlayer majority carrier recombination.

CONCLUSION

In conclusion, we have demonstrated band-to-band tunneling current in vertical MoS_2/WSe_2 heterostructures by using a symmetric dual-gate device architecture. The same device can be operated as an Esaki diode, a backward diode, or a forward rectifying diode by tuning the applied gate voltages, making the device highly versatile. Notably, a high gate coupling efficiency of ∼80% is demonstrated for tuning the band offsets at the MoS_2/WSe_2 vertical interface. Theoretical simulations confirm that the diode operation modes can be easily modulated by the two gates due to weak electrostatic screening by the 2D layers. Both experiments and theory depict the importance of inelastic current transports in vdW vertical heterostructures in the forward bias operation mode, arising from lack of a charge depletion region along the vertical direction. The demonstration of 2D-to-2D tunneling is an important finding in semiconducting layered materials. This work establishes the possibility of using vdW semiconductor heterostructures in tunnel transistors for future low-power electronics.

METHODS

Device Fabrication. The bottom gate was fabricated using electron-beam lithography, with 50 nm Ni contact thermally evaporated, followed by 20 nm ZrO_2 deposited by atomic layer deposition at 110 °C. MoS_2/WSe_2 flakes were patterned next. Ni (50 nm) was thermally evaporated as contact to MoS_2, and 50 nm of Pd was e-beam evaporated as contact to WSe_2. For the

top gate stack, SiO_x (~1 nm) was evaporated as nucleation layer for atomic layer deposition of ZrO_2 (20 nm) deposited at 110 °C as the gate dielectric. Ni (50 nm) was then evaporated as the top gate contact.

Electrical Measurements. The MoS_2/WSe_2 heterostructure devices were electrically characterized under vacuum in a Lakeshore cryo-probe station. Devices were measured using an Agilent B1500A semiconductor parameter analyzer.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Raman spectrum of a MoS_2/WSe_2 heterostructure; simulated band diagrams; and additional experimental device data. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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