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Conductance slope and curvature coefficient of InGaAs/GaAsSb heterojunctions at varying band alignments and its implication on digital and analog applications

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We assess InGaAs/GaAsSb heterojunctions at varying band alignments for applications in both tunnel field effect transistors (TFETs) as well as for nonlinear analog components such as millimeter wave detectors. We use conductance slope measurements as a fundamental figure of merit, as it is not affected by the three-terminal parasitics of subthreshold-slope in a TFET and represents the ideal subthreshold slope intrinsic to the junction in the absence of three-terminal parasitics. We prove that conductance slope/subthreshold slope is not equivalent to curvature coefficient, indicating that it is actually easier to exceed the thermal limit of curvature for analog applications than it is to exceed the subthreshold slope limit for digital applications. In addition, we show that no published heterojunction that exceeds the curvature limit would be capable of exceeding the subthreshold slope limit. We experimentally demonstrate the formation of epitaxial InGaAs/GaAsSb heterojunctions at varying band alignments accomplished using lattice-mismatched epitaxy with graded buffers. We show a dependence of conductance slope on material quality, adding further proof that "steepness" is limited by materials defects and inhomogeneity. We demonstrate that the conductance slope does not depend on temperature for type-II band alignment, adding further proof that TFETs, which show strong temperature dependencies, are dominated by thermal parasitics. Finally, we develop and demonstrate an InGaAs/GaAsSb heterojunction system integrated on an InP platform with a record 76 mV/decade conductance slope and 43 V^{-1} curvature coefficient near zero-bias, with the capability of up to 60 V^{-1} curvature coefficient. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4937921]

I. INTRODUCTION

There are variety of applications in electronic devices that require the device conductance to be sharply modulated by an applied potential. In the area of digital logic, this manifests as a transistor with a steep subthreshold slope: an output current that increases sharply with input gate bias. Physically equivalent, in a two terminal device, this translates to having a high-curvature nonlinear circuit element, useful for analog signal mixing and detectors for millimeter waves. However, for both three-terminal and two terminal devices, there is a conventional limit for classical high performance. For three-terminal devices that utilize a standard MOSFET design, the subthreshold slope cannot be less than the thermal limit of 60 mV/decade at room temperature. In a two terminal device, nonlinearity from a junction results in a curvature coefficient thermal limit of 38.7 V^{-1}. Both of these limits result from the Fermi-Dirac distribution of carriers overcoming an energy barrier.

Tunneling in semiconductors offers the potential to surpass these limits, as devices using tunneling do not rely on carrier emission over a barrier, but rather tunneling through it. As a result, they are not bound by the Fermi-Dirac distribution. Research in the past ten years has developed a strong interest in density-of-states switching in semiconductor heterojunctions with type-II and type-III band alignment for tunnel field effect transistors (TFETs) that could surpass the thermal subthreshold slope limit.[1–21] Such devices rely on band-overlap across the junction in the on-state, where carriers can tunnel from the conduction band of one side to the valence band of the other, while in the off-state, the bands are not overlapping and tunneling is forbidden. Such devices can theoretically obtain conductance slopes as steep as the band edges of the material.[21–24] However, in reality, experimental results have not matched this.[1,3,10,12,15,20,25] For TFETs, the most dominant problem is that they are affected by a variety of parasitics. Most notably, TFETs exhibit a strong temperature dependence,[3,10,12,26] indicative that a thermal carrier promotion mechanism is overpowering the interband tunneling mechanism. In this and previous works,[27,28] we use the method of conductance slope to probe the intrinsic nature of interband tunneling from the band-edges at the interface without convoluting this slope with three-terminal parasitics. We have previously used this method for the specific case of type-III InAs/GaSb heterojunctions and found that there is no temperature dependence of conductance slope,[28] contrasting strongly with the temperature dependence of subthreshold slope in TFETs. This serves as a strong proof of TFETs being limited by thermal parasitics. If these parasitics could be overcome, the devices would then likely become limited by material defects and inhomogeneity, as we have previously shown this to be the dominant effect that limits conductance slope steepness for InAs/GaSb heterojunctions in the absence of three-terminal parasitics.[27] In this work, we expand this study to varying

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band-alignments in order to assess if tailoring the band-alignment across type-II and type-III, including on the transition between both types, offers an improvement in steepness, and if the previous InAs/GaSb conclusions of defects limiting steepness and temperature independence still hold across all band alignments.

We also expand our analysis to analog applications to offer some important insights. While TFETs using the band-edge filtering mechanism have not surpassed the thermal subthreshold limit, there have been examples of backward diodes obtaining curvature coefficients greater than the thermal curvature limit,[29–31] as high as $49.4\,\mathrm{V}^{-1}$.[31] While this could fallaciously be interpreted to mean such material is capable of steeper-than-thermal subthreshold slopes in TFETs under better-optimized conditions, we will show that this is not true. From the physics of interband tunneling, we show that these are two entirely separate limits that do not result entirely from the same physical phenomena. While the conductance slope results only from the physics of tunneling at the band-edges, the conductance slope is actually convoluted with a complicated voltage dependence, and as such, the two thermal limits are actually only equivalent at high bias. In this work, we prove and demonstrate experimentally that it is easier to beat the thermal curvature limit than it is to beat the conductance slope/subthreshold slope limit.

Finally, in undertaking this study, we demonstrate the potential for lattice-mismatched structures in this application area. Backward diode devices to date utilize material that is lattice matched to a binary substrate.[14,29–37] The electron affinity of the material gives a type-II or type-III band alignment, and doping is then used to further tailor the bands, bringing them as close as possible without overlapping. III-V heterojunction TFETs are also primarily lattice matched,[1,3,9–12,14,20,25] with the exception of an MBE-grown InAlAs buffer platform demonstrated by Zhu *et al.*[15] In this work, we allow for this additional degree of freedom using lattice mismatch, allowing us to vary band alignment without using doping and to bring the bands as close as possible. This is done by using compositional control of InGaAs and GaAsSb. We demonstrate the use of GaAsSb and InAsP compositionally graded buffers to grade the lattice mismatch over thickness and varying lattice constant to achieve low defect densities in the device layers, relieving us of the burden to be lattice-matched to a binary substrate. We study in this work how lattice-mismatch can be utilized to optimize conductance slope and curvature coefficient.

This report will begin by comparing the conductance slope to the curvature coefficient. We identify their important differences and establish their nonequivalence. We then proceed to additional experimental analysis to confirm this result, as well as to study the effects of lattice mismatch, band alignment, material quality, and temperature on the two figures of merit for analog and digital applications.

II. CONDUCTANCE SLOPE VS. CURVATURE COEFFICIENT FOR INTERBAND TUNNELING

Figure 1 shows an example of a type-II band alignment InGaAs/GaAsSb heterojunction with no band-overlap at zero-bias (Figure 1(a)), and with an applied bias, giving band overlap that allows for a tunnel current (Figure 1(b)). We define positive applied-bias as a positive voltage applied to the GaAsSb (p-type) side. The tunnel current is described by[38,39]

$$I = C_1 \int^{\Delta E} [F_C(E) - F_V(E)] T_t N_C(E) N_V(E) \boldsymbol{dE}, \tag{1}$$

where $F_c(E)$ and $F_v(E)$ are the Fermi-Dirac distributions on either side of the tunnel junction, T_t is the tunnel probability, and $N_C(E)$ and $N_V(E)$ are the density of states in the conduction band and valence bands, respectively. C_1 is a constant, and the integral is taken over the band overlap ΔE. The origin of subthreshold slope in three-terminals, and curvature in two-terminals, is that the density of states term $N_C(E)N_V(E)$ changes rapidly with voltage as the bands become misaligned. This term takes the $N_C(E)N_V(E)$ form in the band tails because the states are likely to be localized and conservation of transverse momentum will not hold. When the bands overlap, a well-defined energy-momentum dispersion relation exists and the $N_C(E)N_V(E)$ term becomes a single joint density of states term as has been expressed previously.[40] No matter the form, however, this term is the origin of the steepness of the band edges. In reality, it is also possible for the tunnel probability to change with applied voltage and add additional steepness in a TFET, beyond that of the band-edge steepness alone. However, the remaining term, $[F_C(E) - F_V(E)]$, is not a part of the steepness due to tunneling and is not changed by the gate-voltage in three terminals. It is therefore necessary to assess the other terms without convolution from this Fermi-function difference term. It was shown by Agarwal and Yablonovitch[40] that assessing the absolute conductance results in a weighted average of the $T_t N_C(E) N_V(E)$ term

$$\frac{I}{V_A} = C_1 \langle T_t N_C(E) N_V(E) \rangle. \tag{2}$$

Hence, the absolute conductance depends primarily on the density of states and the tunnel probability. By removing the Fermi-function difference, this term better captures the physics of what ultimately gives steepness in three-terminals and curvature in two terminals. It also provides a lower limit on the band-edge steepness—the true falloff in density of states at the band edges without convolution of tunnel probability.[40] While the weighting of the terms still depends on the shape of the $[F_C(E) - F_V(E)]$ term, which can change with applied bias, the shape of this function does not change below an applied bias of 4 kT,[40] which at room temperature corresponds to a bias of 0.1 V. Hence, in a small voltage range about the origin, the steepness resulting from the band edges and tunnel probability can be accurately measured by defining a "conductance slope," CS

$$CS = \frac{-dV_a}{d\log(I/V_A)}. \tag{3}$$

Even beyond the range of 0.1 V, the change in shape of the $[F_C(E) - F_V(E)]$ term is overpowered by the many orders-of-magnitude change in density of states.[40] Therefore,

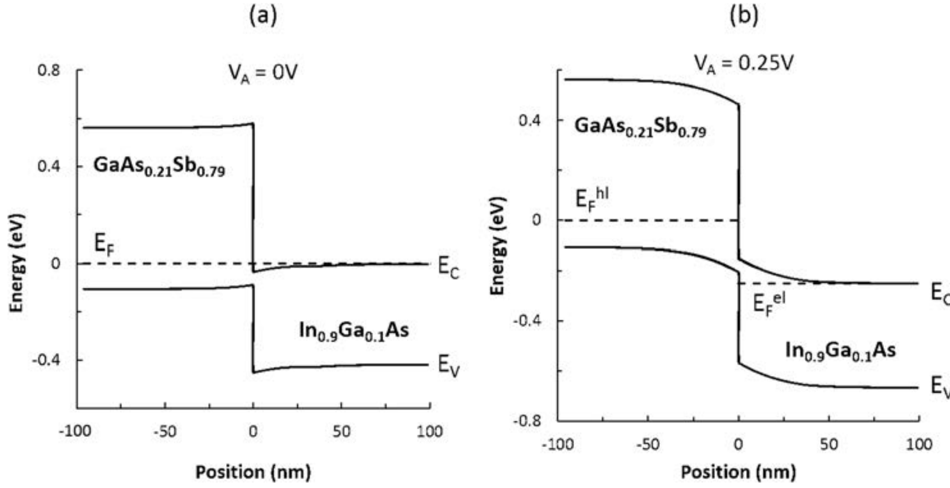

FIG. 1. Band-diagram calculated from a solution to the Poisson equation for a $GaAs_{0.21}Sb_{0.79}/In_{0.9}Ga_{0.1}As$ heterojunction doped p-type $1 \times 10^{17}\,cm^{-3}$ on the Sb-side and n-type $1 \times 10^{17}\,cm^{-3}$ on the As-side. (a) No applied bias. (b) Applied bias of 0.25 V, where bands are overlapped and interband tunneling can occur. The tunnel current direction is shown as the grey arrow.

this definition of conductance slope is valid for all voltage ranges studied in this report. The conductance slope is defined in the above manner so that it can be compared to the subthreshold slope of TFETs: the slope is expressed as mV/decade, and the negative sign ensures the slope is positive, as TFETs define reverse bias across the junction as positive gate voltage. In the ideal case of no three-terminal parasitics, the ideal subthreshold slope of a transistor using a heterojunction should be equal to the conductance slope of that heterojunction. For example, for a TFET to be able to beat the thermal subthreshold slope limit of 60 mV/decade, it must have a conductance slope steepness that is steeper than 60 mV/decade. For this reason, the conductance slope is both a useful fundamental figure of merit that can also be viewed as an application-specific figure of merit when assessed in the context of TFETs.

The curvature-coefficient, on the other hand, is a purely application-specific figure of merit, which is related to the band-edge steepness and tunnel probability, but also convoluted with the applied bias. It is a very well-established figure of merit for a nonlinear component, namely, square-law detectors. It is defined as the ratio of the second derivative of the current-voltage (I-V) curve normalized by the admittance level

$$\gamma = \frac{\frac{d^2I}{dV_A{}^2}}{\frac{dI}{dV_A}}. \tag{4}$$

The reason that this figure of merit is not purely a function of band-edge steepness and tunnel probability can best be seen by recasting the tunnel current from Equation (1) in terms of the conductance slope. Recasting the conductance slope definition into an expression for tunnel current gives

$$I = C_2 V e^{\frac{-V_A \cdot \ln(10)}{CS}}. \tag{5}$$

And then expressing the curvature coefficient in term of this gives a clear link between conductance slope and curvature coefficient

$$\gamma = \frac{-\ln 10}{CS} \times \frac{2 - V_A \frac{\ln(10)}{CS}}{1 - V_A \frac{\ln(10)}{CS}}. \tag{6}$$

This is an important result as it indicates that there is not a simple one-to-one relationship between the curvature coefficient and the more pure band-edge-specific conductance slope. While the first term is a simple conversion between the two figures of merit, it is modulated by a second term that depends on voltage. As a result, the peak curvature coefficient depends on which voltage range has the steepest conductance slope, which depends on the band-alignment. Figure 2 shows a plot of this second term, which we refer to as the "modulation factor." At high forward and high reverse bias, the term converges to one, and there is a simple relationship between conductance slope and curvature coefficient

$$\gamma = \frac{-\ln 10}{CS}. \tag{7}$$

In these high-bias regions, a conductance slope at the thermal limit of 60 mV/decade yields a curvature coefficient at the thermal limit of 38.7 V^{-1}. However, away from these

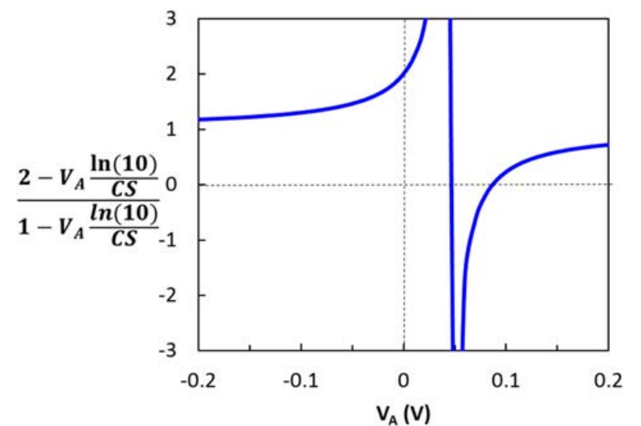

FIG. 2. Plot of "modulation factor" that modulates relationship between conductance slope and curvature coefficient, as a function of applied voltage, for an example case of a 100 mV/decade conductance slope throughout.

regions, the term takes on wildly different values. Most importantly, moving from reverse bias towards the origin, there is an increase of the term, which eventually reaches a value of exactly 2 at the origin, and then diverges in forward bias due to negative resistance. This behavior allows for two important conclusions to be made:

(1) If the composition of a heterojunction is tailored, or if the interface is tailored, to change the band alignment, the peak curvature coefficient should increase as band-alignment is shifted towards type-III, since the voltage range of steepness shifts from reverse bias to forward bias.
(2) It is not necessary to have a conductance slope steeper than the thermal limit to obtain a curvature coefficient steeper than the thermal limit. At the origin, where this modulation factor is equal to two, a conductance slope below only 120 mV/decade is required to yield a curvature coefficient beyond 38.7 V^{-1}. This also means that heterojunctions that have been shown to provide curvature coefficients greater than the thermal limit of 38.7 V^{-1} are not necessarily capable of yielding a TFET that can beat the thermal subthreshold limit of 60 mV/decade, unless the curvature coefficient was greater than 77.4 V^{-1}, which has never been demonstrated in a heterojunction. The current best published curvature coefficient at zero-bias is 49.4 V^{-1},[31] yielding a conductance slope of 93 mV/decade. In this work, we report a conductance slope of 76 mV/decade.

This concept is assessed experimentally in Section IV, where structures with varying band alignment will be explored. We will find that the change in band-alignment is due to both defects and control of composition.

III. EXPERIMENTAL METHODS

Device structures were grown epitaxially via metalorganic chemical vapor deposition (MOCVD) in a custom-designed Thomas Swan/Aixtron low pressure system with a close-coupled showerhead. Devices were grown on p-type (100)-oriented GaSb substrates or n-type (100)-oriented InP substrates. All layers were grown at a total pressure of 100 Torr using TMGa, TMIn, TMSb, AsH_3, and PH_3 as precursors and H_2 as carrier gas. Buffer layers (GaSb, GaAsSb, InP, and InAsP) were grown in a temperature range of 530–650 °C, while all device layers (InGaAs and GaAsSb) were grown at 530 °C. Film compositions were calibrated using high resolution X-ray diffraction (HRXRD) on the [004] and [224] diffraction conditions. No dopant precursors were flowed, allowing device layers to be at the lowest possible level of unintentional doping, which is expected to be n-type in the mid-10^{15} cm^{-3} range for InGaAs at this growth temperature,[41,42] and p-type in the mid-10^{16} cm^{-3} range for GaAsSb.[43,44] Structures were characterized with cross-section transmission electron microscopy (TEM) on the [220] diffraction condition to determine the nature of defects in the structure, as well as with HRXRD on the [004] and [224] diffraction conditions to assess degree of relaxation, and tapping-mode atomic force microscopy (AFM) to determine the structure of steps on the surface. 40 μm-diameter circular mesa diodes were fabricated using electron-beam evaporated Ti/Pt/Au contacts which were used as an etch mask for a self-aligned mesa. Bottom contacts were formed with indium, and for the case of devices with graded buffers, self-aligned side-contact structures were formed using electron beam evaporated Ti/Pt/Au masked by the top contact, in order to ensure that the buffer does not add series resistance. I-V curves were measured in a Faraday cage with an Agilent B1500a semiconductor parameter analyzer with Kelvin connections. As opposed to previous work with type-III band alignment structures,[27] series-resistance correction was not necessary in this study as the conductance in type-II structures was much lower and the series resistance due to the contacts and substrate was insignificant in comparison. For temperature-dependent measurements, the same semiconductor parameter analyzer was used on a Lakeshore Cryogenic probe station, using liquid nitrogen cooling for temperatures down to 77 K.

IV. RESULTS AND DISCUSSION

A. GaAsSb graded buffers

In order to obtain quality device layers on a lattice constant that is not lattice-matched to a binary substrate, it is necessary to begin growth on a binary substrate and then utilize a compositionally graded buffer to slowly introduce the strain towards the desired lattice constant. The first scheme that was utilized in this work was a compositionally graded GaAsSb buffer grown on a GaSb substrate. A schematic of the structure is shown in Figure 3(a). A 0.8 μm GaAsSb graded-buffer was grown at 530 °C to the $GaAs_{0.36}Sb_{0.64}$ lattice constant, giving a strain grade-rate of 3.3% strain/μm. The result is a somewhat effective glide of misfit dislocations relieving the strain, but many residual threading dislocations still visible in cross-section TEM (Figure 3(b)), indicating a high threading dislocation density of likely above 10^7 cm^{-2} in the device layers. There are also defects nucleating from the InGaAs/GaAsSb device interface, and this is somewhat in part due to the fact that the buffer is only 80% relaxed, as can be seen from the [224] X-Ray Diffraction (XRD) reciprocal space map (RSM) in Figure 3(c). Thus, even with attempts to lattice match the composition, there is still lattice mismatch due to the residual strain in the buffer. Furthermore, since the lower layer contains Sb, it is likely that there is strain buildup due to intermixing, as has been reported previously.[15,27]

In light of this, a buffer was grown at 580 °C. The purpose of this was twofold: (1) to allow for greater relaxation of the buffer, and (2) to allow for a potentially lower threading dislocation density via a lower grade rate. This process change is because we expect the Sb-growth to be in the surface-reaction limited regime, and therefore, we should observe an increase in growth rate with temperature, which allows for a lower strain grade rate since more material will be deposited per unit time. Keeping at the same temperature and growing thicker is not as practical, since the growth rate of 6 nm/s results in uneconomically long growth times. 580 °C was chosen since Yang *et al.*[45] determined this

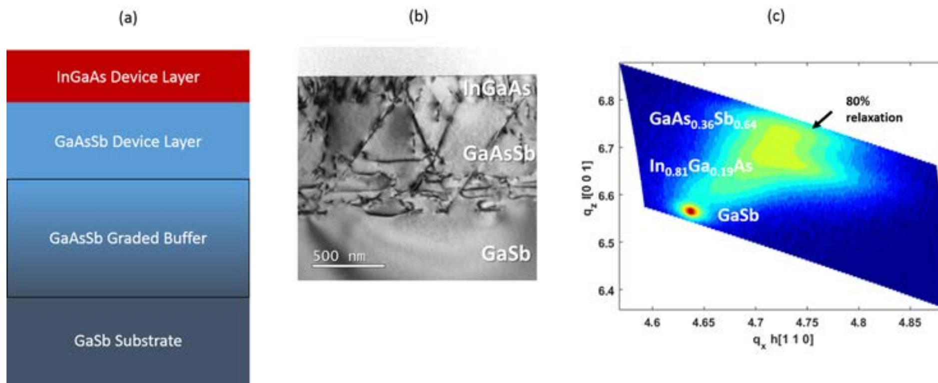

FIG. 3. (a) Schematic of InGaAs/GaAsSb/GaAsSb graded buffer/GaSb structure, (b) cross section TEM image of structure on the [220] diffraction condition, (c) HRXRD [224] reciprocal space map of structure.

temperature to be optimal for GaAsSb graded buffers in MOCVD when graded buffers were graded compressively from a starting GaAs lattice constant. However, Figure 4(a) shows that for the case of beginning on the GaSb lattice constant and grading in the tensile direction, the quality of the buffer is very poor. The thickness of the structure was 2.3 μm, with a growth rate of 17.4 nm/s (a factor of 2.9 increase from 530 °C), giving a strain grade rate of 1.1%. At this grade rate for the case of compressive GaAsSb buffers, Yang *et al*. reported a threading dislocation density of 5×10^6 cm^{-2}.[45] However, the buffer layer in the TEM image is considerably more defective than that and shows an incredibly high dislocation density. This indicates that there is a profound difference when grading from the GaSb lattice constant towards the InP lattice constant when compared to grading from the GaAs lattice constant. Furthermore, it seems that increasing the temperature and decreasing the grade rate has actually resulted in a considerably worse film.

One potential explanation for this comes from examining the very beginning of the buffer. For the 530 °C film in Figure 3(a), all that is seen are a few misfit dislocations at the very beginning of the grade. However, the interface where the grade begins for the 580 °C film is a much more distinct interface, and appears more defective than the rest of the film. Figure 4(b) shows a more magnified image of the interface. There are clear defects, likely stacking faults, originating from the interface. These features are highly indicative of a large misfit strain between the start of the GaAsSb buffer and the underlying GaSb substrate. This behavior is uncharacteristic of a graded buffer, as there should be no large step in strain about an interface if the strain is being graded slowly. This implies that some other effect has occurred to create this strain. This could potentially be caused by an intralayer As-Sb exchange mechanism. Such exchange has been heavily reported between layers for binary InAs/GaSb growth.[27,46,47] In this case, and at this temperature, however, it is likely that since As and Sb are present in the same layer, an exchange mechanism can occur within the layer, resulting in Sb segregating to the surface, leaving a highly strained As-rich GaAsSb region near the interface. It is even possible for bulk diffusion to later correct this difference in composition, but since it is a slower process than exchange, it is possible for many dislocations to form before this correction can occur.

This explanation is consistent with the two key findings for GaAsSb buffers:

(1) The quality is lower at higher temperatures. Higher temperatures enable more surface exchange between Sb and As since more thermal energy is available to overcome the activation energy barrier of exchange.
(2) High dislocation densities are only observed when grading from the GaSb lattice constant, and not from the GaAs lattice constant, even when growing on the same MOCVD system with the same conditions.[45] When starting on GaAs and grading in the reverse direction, the movement of As down into the film and Sb upwards would result in a more As-rich GaAsSb, but since the film is growing on GaAs, higher arsenic concentrations would be less strained than the case of GaAsSb with no exchange. As initial surface exchange from strong gradients dissipates over many layers, the end result is a less steep concentration gradient than the targeted one, which is typically associated with better material quality.

This problem of intra-layer As-Sb exchange as temperature is increased puts a difficult constraint on GaAsSb buffers, since temperature cannot be increased to improve the buffer quality, and the buffer quality is not good enough to obtain low threading dislocation densities or full relaxation at 530 °C. Therefore, we examined an alternate buffer design involving InAsP buffers on an InP platform.

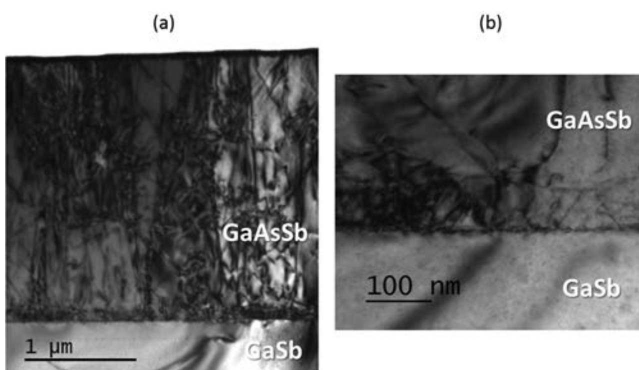

FIG. 4. (a) TEM image on the [220] diffraction condition of a GaAsSb buffer grown at 580 °C on GaSb, showing many defects. (b) A more magnified image of this sample, showing a very high concentration of defects originating right from the interface where the buffer was initiated: a rare observation for a graded buffer.

B. InAsP graded buffers

InAsP graded buffers are likely a better candidate for a graded buffer materials system as a means to achieve the required device lattice constant, because they will not be affected by the Sb-As exchange process as described in Section IV A, and because it can be grown at much higher growth rates, allowing for much thicker graded buffer layers within practical time constraints, and therefore, creating lower strain grade rates. Further, InAsP can begin on InP substrates, which are more economical than GaSb or InAs substrates, and pave the way for heterointegration with other device technologies.

The intended structure is shown in Figure 5(a). InAsP buffers were grown at 650 °C at a grade rate of 0.25% strain/μm. Buffers were capped with 150 nm of InAsP at the device lattice constant, followed by the lattice-matched InGaAs device layer. There was also an initial strain jump of 0.3% strain, accomplished by beginning the buffer with a 250 nm $InAs_{0.09}P_{0.91}$ layer. The reason for doing this instead of grading directly from 0% As is that a small initial amount of strain is needed to act as a driving force to nucleate misfit dislocations that are spatially uniform and have high glide velocities which ultimately lead to low defect densities. If not enough driving force is initially present in this materials system, lower-activation energy dislocations are nucleated instead, which tend to form from wafer edges or particles, and typically do not have as high glide velocities and result in higher defect densities.[48]

For the case of a device composition of $In_{0.79}Ga_{0.21}As$, a TEM image is shown in Figure 5(b). It can be seen that the buffer is of considerably better quality: misfit dislocations can be seen relieving strain throughout the entire structure, with no threading dislocations visible at the top of the buffer or in the top InGaAs layer. The [224] RSM in Figure 5(c) reveals a much higher degree of relaxation, 93%, has been achieved. Hence, overall, this is a considerably better platform for InGaAs/GaAsSb tunnel devices.

C. The GaAsSb/InGaAs interface

Now that a working buffer platform exists, the next step is to deposit a lattice-matched GaAsSb device layer on top of the InGaAs device layer. It was shown in Section IV A that at 580 °C, GaAsSb suffered from a likely intra-layer exchange that degraded quality. However, at 530 °C, this problem was not pronounced. Hence, the GaAsSb layer growth should be deposited at a temperature not greater than 530 °C if possible. This growth temperature was achieved by ramping down the temperature from the 650 °C InAsP buffer layer and InGaAs layer temperature to 530 °C after the InGaAs cap was grown. An additional 100 nm of InGaAs was then grown at 530 °C, and then GaAsSb layer was grown. Following this, an InGaAs layer was grown on top of the GaAsSb, so that both GaAsSb/InGaAs and GaAsSb/InGaAs interfaces could be examined. The [220] TEM image of the $In_{0.76}Ga_{0.24}As$ and $GaAs_{0.3}Sb_{0.7}$ layers is shown in Figure 6(a), and an AFM of the top surface is shown in Figure 6(b), indicating island growth. Both the InGaAs and GaAsSb layers are considerably defective. The defects seem to originate from the GaAsSb/InGaAs interface, where numerous stacking faults can be seen, analogous to the 580 °C GaAsSb/GaSb interface seen in Figure 4(b). These observations indicate that a similar effect may be occurring involving intralayer As-Sb exchange. While this exchange was not observed previously at 530 °C for the GaAsSb/GaSb interface, it is possible that because the layer growth is initiated at a higher As composition (30% As), there is a sufficient As concentration to swap with Sb so that the effect is noticeable. In theory, there should be a composition at which this effect is maximal: As As% in the film is increased, more exchange occurs, although as the lattice constant approaches that of GaAs, the mismatch resulting from this exchange becomes less. It is possible and likely then that $GaAs_{0.3}Sb_{0.7}$ is closer to this maximum composition compared to when GaAsSb first begins grading from the GaSb lattice constant at effectively 0% As.

To test the exchange hypothesis and to attempt to solve this problem, we used the following initiation sequence to initiate GaAsSb growth at this lattice constant:

(1) Bake InGaAs layer in H_2 for 30 s
(2) Flow 12.7 sccm TMSb for 30 s
(3) Switch on all precursor flows

The goal of the first step was to desorb the As from the InGaAs surface, leading to a group-III-rich surface. The second step was then intended to replace the desorbed As with a

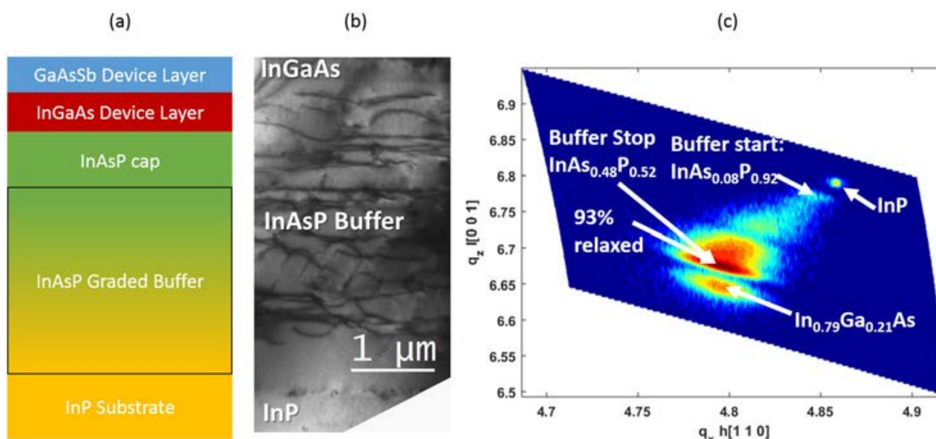

FIG. 5. (a) Schematic of an example GaAsSb/InGaAs device on an InAsP buffer, (b) TEM image on the [220] diffraction condition for an InAsP buffer on InP, with an InGaAs cap. (c) [224] reciprocal space map of the structure.

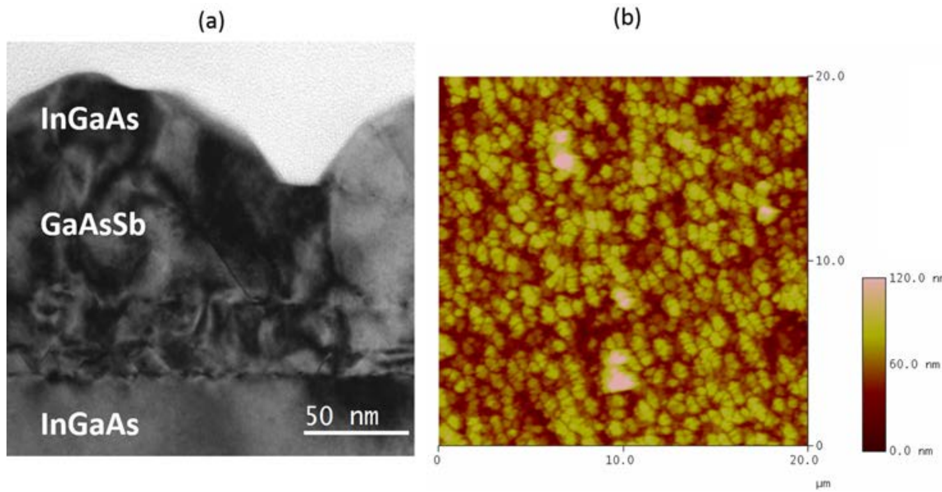

FIG. 6. (a) [220] TEM image of InGaAs/GaAsSb heterojunction grown on the InGaAs-capped InAsP buffer. (b) Corresponding AFM image of the top surface of the top InGaAs layer, indicating high roughness and likely island growth.

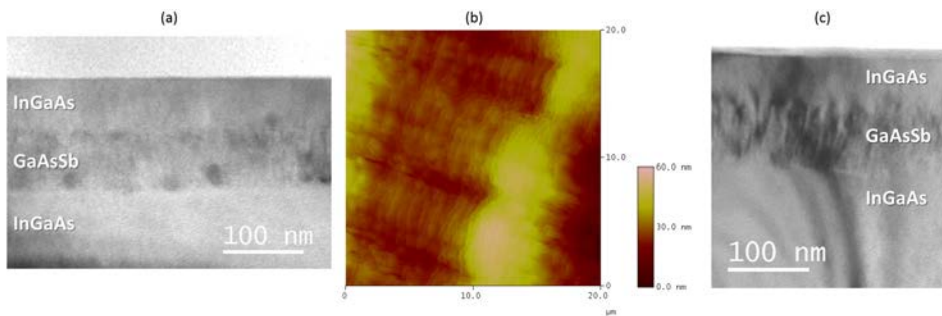

FIG. 7. (a) [220] TEM image of InGaAs/GaAsSb/InGaAs on an InAsP buffer using a 30 s H2 bake + 30 s TMSb flow to initiate the GaAsSb layer. The dark circles are milling-induced defects. (b) AFM image of the top InGaAs showing evidence of step-flow growth. (c) [220] TEM image of a different region of the sample showing evidence of phase separation in the GaAsSb layer.

layer, or multiple layers, of Sb. The Sb layer was intended to passivate the surface to prevent exchange. In other words, with Sb already on the surface, there should be no driving force for Sb in lower planes in the layer to segregate to the surface.

Figure 7(a) shows the result: a higher quality interface without visible defects in cross section TEM. In this particular image, the only visible feature is milling damage from TEM sample preparation. The InGaAs layer above also shows no defects in cross section TEM. Additionally, the AFM image in Figure 7(b), which can also be compared back to Figure 6(b), reveals a regular step structure, indicative that step-flow growth was maintained and no island formation occurred. However, Figure 7(c) shows an image of another region of the sample, where striations can be seen in the GaAsSb layer, indicative of lateral composition variation or phase separation. Since this was not observed before, it is possible that it may have been induced by the Sb on the surface. Nevertheless, a platform for growing good quality InGaAs/GaAsSb layers is established.

D. Conductance slope

Figure 8(a) shows the I-V curve for an $In_{0.8}Ga_{0.2}As/GaAs_{0.3}Sb_{0.7}$ lattice-matched junction on three separate platforms. The first (blue) is grown directly on a GaSb substrate without a graded buffer and is expected to be the most defective as a result. The second (green) is for the GaAsSb buffer of intermediate quality as described previously. The third (blue) is for the junction grown on the InAsP platform, which was shown in Section IV C to be the highest quality, with no visible threading dislocations in the device layer in cross-section TEM. The conductance slope for all three devices is compared in Figure 8(b). For the buffer devices, self-aligned side contact structures were fabricated and compared to the top-bottom contact structures to ensure the buffer layer does not interfere with the I-V characteristic. The I-V curves were identical for both contact-schemes in the region of interest and only deviated at currents above 1 kA/cm^2. In examining the conductance slope of the structures at varying material quality, there is a major improvement in the steepness of the conductance slope as the quality is improved. We have reported similar results previously for the binary InAs/GaSb system,[27] and so this trend is extended to ternary InGaAs/GaAsSb with different band alignment.

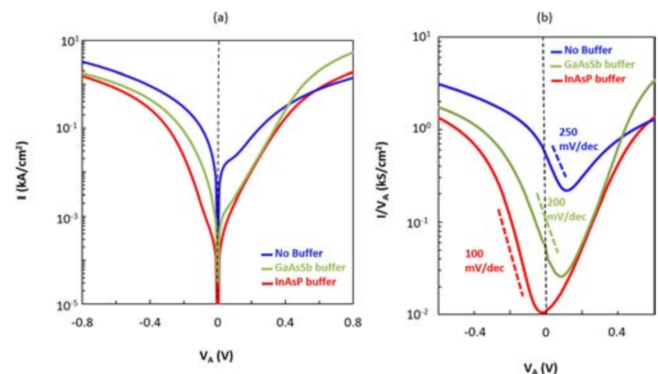

FIG. 8. (a) I-V curves of $In_{0.8}Ga_{0.2}As/GaAs_{0.3}Sb_{0.7}$ heterojunction on no buffer (blue curve), a GaAsSb buffer (green curve), and an InAsP buffer (red curve). (b) Corresponding I/V-V curves.

Additionally, the on/off conductance ratio becomes much larger for higher quality junctions, primarily because the minimum conductance decreases significantly with improving material quality. This is an indication that the off-state current is not a purely thermal process, but rather a defect-assisted mechanism, as was seen previously for type-III structures.[27,28] Further evidence of this will be shown in Section IV F when the temperature dependence is studied.

Finally, there is a noticeable shift of the region of conductance slope steepness to the left as material quality is improved, indicating a shift from type-III band alignment to type-II band alignment. Similar shifts have been seen previously with defects,[18,27] and defects are typically responsible for a shift to greater type-III band alignment. We have described previously how defects and inhomogeneity lead to band alignment shifts in both directions across the tunnel interface.[27] However, the regions that are most type-III will always be the first to turn-on or the last to turn off. Therefore, when assessing conductance on a logarithmic scale, the most type-III regions of the junction will eventually dominate when all other regions cannot tunnel. Therefore, as defects and inhomogeneity increase, there will be regions that reach greater type-III band alignment, and a general shift of the conductance-voltage curve to the right.

Overall, the large improvement in conductance slope steepness with buffer quality is promising. In an attempt to improve steepness further, this same InAsP buffer platform was used to alloy the device further towards type-III, using an $In_{0.9}Ga_{0.1}As/GaAs_{0.21}Sb_{0.79}$ composition. This heterojunction should be very close to the type-II/type-III band alignment crossover. There are two reasons to believe such a device may have better steepness:

(1) The steepness may benefit from being close to the type-II/type-III crossover since lower voltage will create less band-bending in the heterojunction and possibly avoid accessing more interface variability or inhomogeneity.
(2) The heterojunction composition may minimize phase separation or lateral composition variation, thereby minimizing interface inhomogeneity as compared to an interface with slight composition variation.

The result in alloying further towards type-III is shown in Figure 9(a). There is a remarkable increase in conductance slope of 76 mV/decade that close to the thermal limit. For comparison, the device is compared to the same composition without a buffer in Figure 9(b), where an enormous difference in conductance slope is seen as well as the shift discussed previously. The results in the subsequent two sections will prove that this steep conductance slope is due to true interband tunneling and not through a thermally activated mechanism.

The conductance steepness in this device is the highest slope seen to date, and it is a good indication that with the correct control of growth conditions and materials parameters, it is possible to obtain a conductance steepness that approaches the thermal limit. This result is encouraging, as it indicates that with further optimization of some of the finer parameters of the growth, it may be possible to eventually observe steeper than 60 mV/decade switching.

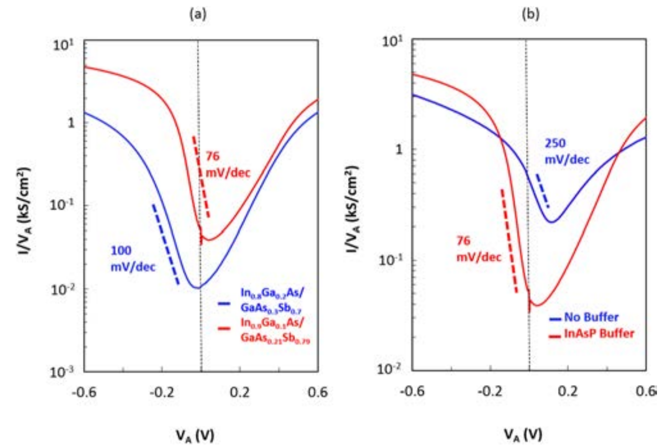

FIG. 9. (a) I/V-V curve of $In_{0.9}Ga_{0.1}As/GaAs_{0.21}Sb_{0.79}$ heterojunction (red) and $In_{0.8}Ga_{0.2}As/GaAs_{0.3}Sb_{0.7}$ heterojunction (blue) on an InAsP/InP platform. (b) I/V-V curve of $In_{0.9}Ga_{0.1}As/GaAs_{0.21}Sb_{0.79}$ heterojunction with an InAsP buffer (red) and without a buffer (blue).

E. Curvature coefficient

While the $In_{0.8}Ga_{0.2}As/GaAs_{0.3}Sb_{0.7}$ heterojunction shows a major improvement in conductance slope as material quality improves, the same behavior is not observed for peak curvature coefficient, as is shown in Figure 10(a). For the case of no buffer (blue), there is a peak curvature of about 30 V^{-1} that occurs at a forward bias of 40 mV. As the material quality improves, there is a shift of the peak curvature to the left, consistent with the shift in effective band alignment described in Sec. IV D. However, the value of the peak curvature does not improve. The reason for no improvement is that the modulation factor, which was shown in Figure 2, decreases with increasing reverse bias. Therefore, the loss of defects and inhomogeneity create two opposing effects: (1) an improvement in conductance slope that increases the peak curvature coefficient, and (2) a band alignment shift to the left that lowers the modulation factor and lowers the peak curvature coefficient.

However, it was shown that when the device on the InAsP platform was alloyed to a slightly more type-III band alignment, there was an improvement in conductance slope steepness. Therefore, this device would be expected to have a considerable improvement in peak curvature coefficient, as it has both effects working in its favor: an improvement in conductance slope and a band alignment shift to the right. Figure 10(b) confirms this by comparing the original composition (type III) to the new composition (near crossover). In shifting to the crossover composition $In_{0.9}Ga_{0.1}As/GaAs_{0.21}Sb_{0.79}$, the peak curvature coefficient improves to 43 V^{-1}. This peak curvature exceeds the thermal limit of curvature, which supports the results of Section II: this heterojunction obtained 76 mV/decade in conductance slope steepness, which is not beyond the thermal limit for conductance slope, but the same heterojunction obtains a curvature coefficient beyond the thermal limit. In fact, the two figures of merit are in near-perfect agreement theoretically: for a conductance slope of 76 mV/decade, with a peak curvature at −40 mV bias, calculations predict a modulation factor of

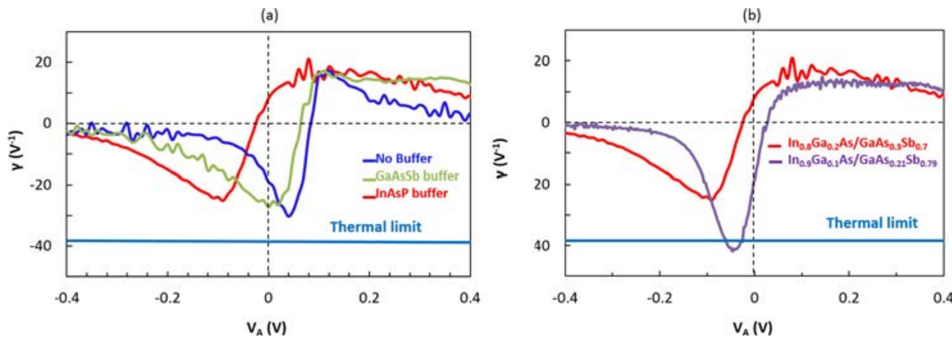

FIG. 10. (a) Curvature coefficient of $In_{0.8}Ga_{0.2}As/GaAs_{0.3}Sb_{0.7}$ junction on three different buffer platforms. (b) For an InAsP buffer platform, the curvature coefficient for an $In_{0.8}Ga_{0.2}As/GaAs_{0.3}Sb_{0.7}$ junction (red) is compared to an $In_{0.9}Ga_{0.1}As/GaAs_{0.21}Sb_{0.79}$ junction (purple), showing demonstration of beyond the thermal limit of curvature coefficient near the origin.

1.45, which predicts a peak curvature coefficient of 44 V^{-1}, which is close to the observed 43 V^{-1}. Under optimized processing conditions, a small tweak in calibration should allow for the correct band alignment such that the curvature coefficient peaks at 0 V. Assuming the conductance slope remains at 76 mV/decade (although it may improve further), the full factor of 2 modulation factor can provide a zero-bias curvature coefficient of over 60 V^{-1}. Such a value for curvature coefficient is higher than any reported heterojunction result to date.

F. Temperature dependence

For the intermediate quality GaAsSb buffer device, the temperature dependence of both the conductance slope and the curvature coefficient was studied from room temperature down to 77 K. Figure 11(a) shows the I-V curve of the device and 11(b) shows the conductance slope. As the temperature is decreased, a negative differential resistance (NDR) begins to develop, confirming tunneling. Consistent with this emergence of NDR, the I/V-V curve shifts towards a type-III band alignment, likely due to shifts in band-alignment with temperature and strain created through lattice expansion and the deformation potentials. The off-current decreases with temperature as was the case with binary InAs/GaSb. But the current change is still not exponential, indicating that it may involve a trap-assisted leakage process. This is consistent with the observation from Section IV D that the minimum conductance decreased in magnitude with improvement in buffer quality, indicative of a trap-assisted process.

Most importantly, the trend of conductance slope remains the same: There is still no temperature dependence. This is similar to what we reported previously for type-III binary InAs/GaSb heterojunctions.[28] The conductance slope probes the steepness of the interface directly, as opposed to extracting a subthreshold slope from a TFET, which convolutes the interface steepness with a variety of three-terminal parasitics. These conductance slope measurements contrast strongly with TFET subthreshold slope measurements, which show a very strong temperature dependence.[3,7,9,10] The fact that we observe no temperature dependence in the absence of these three-terminal parasitics is strong evidence that TFETs using a band-edge filtering mechanism with a heterojunction are likely dominated by thermally activated parasitics: likely either a high conductance parallel leakage pathway or a high resistance series component. To further illustrate this, we combined the subthreshold slope results for published TFETs which use a band-filtering mechanism, and for which a subthreshold slope was reported for at least two temperature points (Figure 11(c)). All results show a linear dependence of subthreshold slope with temperature, similar to what would be expected for a MOSFET. To correct for differences in gate control, we normalized each data point by the 300 K measurement from that set. The results are shown on in Figure 11(d): all points effectively fall along a single line, and the thermal limit also folds into this line. This is a strong indication of thermal parasitics dominating. For comparison, our temperature-independent results from our two-terminal devices in this paper and from our previous work are included on the plot.

While the conductance slope is independent of temperature, the curvature coefficient shows a slight temperature dependence. The curvature coefficient is shown in Figure 12(a) for the same device. For 150–300 K temperature points, there is a general shift to the right and increase of peak curvature coefficient. This behavior is due to the shift in band-alignment that occurs as temperature is cooled, as was seen in Figure 11(b). Consequently, the peak curvature increases due to the modulation factor change. At the 100 K and 77 K temperature points, the band overlap is type-III and large enough that negative resistance occurs, which cause AC oscillations in the test circuit and the sharp peaks in curvature coefficient. At zero-bias, there is also a change with temperature, even with the modulation factor constant at 2. This change is because the conductance slope at zero-bias is varying: the region of steepest conductance slope is shifted to zero bias around 150–200 K. Above this temperature window, the steepest portion of conductance slope is slightly in reverse bias, and below this temperature window, it is slightly in forward bias.

The change in curvature coefficient with temperature, while nonzero, is still incredibly less pronounced than for a Schottky-barrier device or any device that extracts its curvature from a thermal mechanism. This is demonstrated in Figure 12(b), which compares the zero-bias curvature coefficient for this device, normalized by its 300 K value, as a function of temperature. We compare this device behavior to the thermal behavior q/kT. While thermal devices change significantly, the device in this report only shows a slight change due to the shift in band alignment. Thus, the device is quite insensitive to temperature fluctuations, which can allow its operation to be more robust in varying-temperature environments.

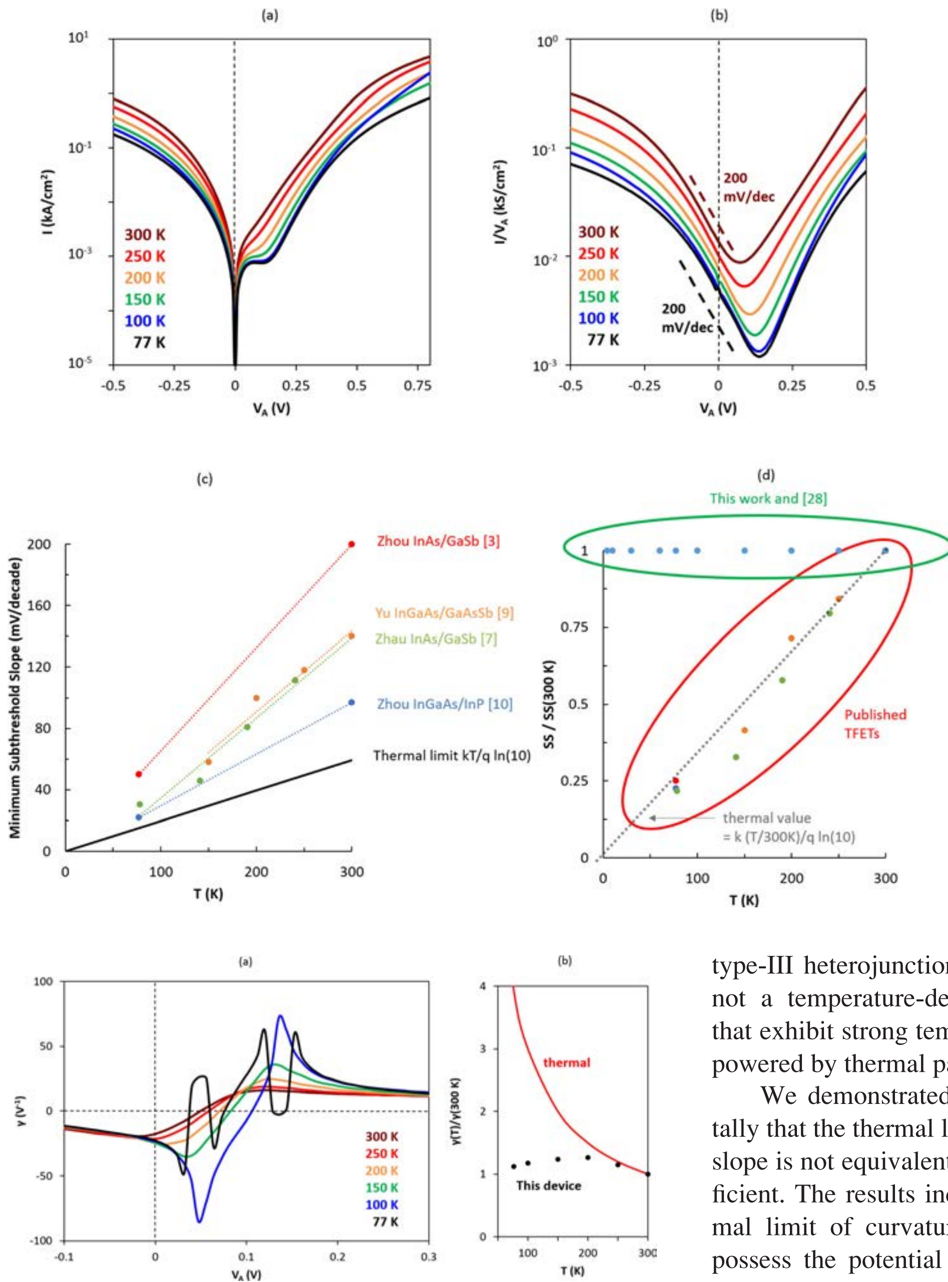

FIG. 11. (a) I-V curve of $In_{0.8}Ga_{0.2}As/GaAs_{0.3}Sb_{0.7}$ on GaAsSb buffer for temperatures varying from 300 K down to 77 K. (b) Corresponding I/V-V curves. (c) Minimum subthreshold slope vs temperature for a variety of published experimental results that have been complied together into this plot. The thermal limit is shown as the black line. (d) Same data from (c), but every data point was normalized by the 300 K subthreshold slope of the set it was collected from. The expected behavior of a thermal device is shown as the grey dotted line. The results of this work and our previous work[28] are included as a contrast.

FIG. 12. (a) Curvature coefficient of $In_{0.8}Ga_{0.2}As/GaAs_{0.3}Sb_{0.7}$ heterojunction device on a GaAsSb buffer as a function of temperature. (b) Curvature coefficient at zero-bias for this device normalized by the value at 300 K, and compared to the thermal trend.

V. CONCLUSIONS

We explored tunneling in InGaAs/GaAsSb heterojunctions with different band alignments and material quality. InAsP graded buffers on InP substrates were key in accommodating the lattice mismatch between the two-terminal heterojunction devices and the substrate. Using the conductance slope from tunneling in the diodes, we showed that heterojunction performance is controlled by material quality. Materials inhomogeneity at an unobservable nm-scale causes the ultimate limit in steepness that can be obtained via interband tunneling at the band edges. The conductance slope does not depend on temperature for these varying-band-alignment interfaces, agreeing with results from previous type-III heterojunctions. In all cases, interband tunneling is not a temperature-dependent phenomenon. TFET devices that exhibit strong temperature dependencies are likely overpowered by thermal parasitics.

We demonstrated both mathematically and experimentally that the thermal limit of conductance slope/subthreshold slope is not equivalent to the thermal limit of curvature coefficient. The results indicate that it is easier to beat the thermal limit of curvature, and also that heterojunctions that possess the potential to switch steeper than 60 mV/decade must have a curvature coefficient greater than $77.4\ V^{-1}$.

Using optimized growth conditions and band alignment, we demonstrate a record conductance slope of 76 mV/decade, with a peak curvature coefficient of $43\ V^{-1}$ near zero bias. These heterojunctions have the capability of achieving $60\ V^{-1}$ curvature if the full factor of 2 in the modulation factor is harvested.

ACKNOWLEDGMENTS

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[1]Y. Lu, G. Zhou, R. Li, Q. Liu, Q. Zhang, T. Vasen, S. D. Chae, T. Kosel, M. Wistey, and H. Xing, IEEE Electron Device Lett. **33**, 655 (2012).
[2]P. Guo, Y. Yang, Y. Cheng, and G. Han, ECS Trans. **50**, 971 (2013).
[3]G. Zhou, R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J. M. Kuo, and T. Kosel, in *2012 IEEE International Electron Devices Meet (IEDM)*, 2012, pp. 32.6.1–32.6.4.

[4]D. K. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu, and S. Datta, Tech. Dig. - Int. Electron Devices Meet. **5**, 781 (2011).
[5]D. K. Mohata, R. Bijesh, Y. Zhu, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, D. Loubychev, A. K. Liu, T. S. Mayer, V. Narayanan, and S. Datta, Symp. VLSI Technol., Dig. Tech. Pap. **2012**, 53.
[6]A. M. Ionescu and H. Riel, Nature **479**, 329 (2011).
[7]X. Zhao, A. Vardi, and J. A. Alamo, Tech. Dig. - IEEE Int. Electron Devices Meet. **2014**, 25.5.1.
[8]A. W. Dey, B. M. Borg, B. Ganjipour, M. Ek, K. A. Dick, E. Lind, P. Nilsson, C. Thelander, and L.-E. Wernersson, in *2012 70th Annual Device Research Conference (DRC)* (IEEE, 2012), pp. 205–206.
[9]T. Yu, J. T. Teherani, D. A. Antoniadis, and J. L. Hoyt, Appl. Phys. Express **7**, 094201 (2014).
[10]G. Zhou, Y. Lu, R. Li, Q. Zhang, Q. Liu, T. Vasen, H. Zhu, J. Kuo, T. Kosel, M. Wistey, P. Fay, S. Member, A. Seabaugh, and H. Xing, IEEE Electron Device Lett. **33**, 782 (2012).
[11]B. M. Borg, K. A. Dick, B. Ganjipour, M. E. Pistol, L. E. Wernersson, and C. Thelander, Nano Lett. **10**, 4080 (2010).
[12]S. Mookerjea and D. Mohata, IEEE Electron Device Lett. **31**, 564 (2010).
[13]A. Seabaugh, in *Proceedings of European Solid-State Circuits Conference* (IEEE, 2011), pp. 34–35.
[14]T. Yu, S. Member, J. T. Teherani, D. A. Antoniadis, J. L. Hoyt, and A. Vertical, IEEE Electron Device Lett. **34**, 1503 (2013).
[15]Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, J. Appl. Phys. **112**, 24306 (2012).
[16]A. C. Seabaugh and Q. Zhang, Proc. IEEE **98**, 2095 (2010).
[17]A. Ajoy, in *2012 15th International Workshop on Computational Electronics* (IEEE, 2012), pp. 1–4.
[18]Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, N. Monsegue, and M. K. Hudait, J. Appl. Phys. **112**, 94312 (2012).
[19]Y. Zhu, D. Mohata, S. Datta, and M. Hudait, IEEE Trans. Device Mater. Reliab. **14**, 1 (2013).
[20]R. Li, Y. Lu, S. D. Chae, G. Zhou, Q. Liu, C. Chen, M. S. Rahman, T. Vasen, Q. Zhang, and P. Fay, Phys. Status Solidi **9**, 389 (2012).
[21]S. O. Koswatta, S. J. Koester, and W. Haensch, in *IEEE International Electron Devices Meeting* (IEEE, 2009), pp. 1–4.
[22]S. O. Koswatta, S. J. Koester, and W. Haensch, IEEE Trans. Electron Devices **57**, 3222 (2010).
[23]J. Knoch and J. Appenzeller, IEEE Electron Device Lett. **31**, 305 (2010).
[24]L. Wang, E. Yu, Y. Taur, and P. Asbeck, IEEE Electron Device Lett. **31**, 431 (2010).
[25]R. Li, Y. Lu, G. Zhou, Q. Liu, S. D. Chae, T. Vasen, W. S. Hwang, Q. Zhang, P. Fay, and T. Kosel, IEEE Electron Device Lett. **33**, 363 (2012).
[26]S. Guha, A. Madhukar, and K. Rajkumar, Appl. Phys. Lett. **57**, 2110 (1990).
[27]R. M. Iutzi and E. A. Fitzgerald, J. Appl. Phys. **115**, 234503 (2014).
[28]R. M. Iutzi and E. A. Fitzgerald, Appl. Phys. Lett. **107**, 133504 (2015).
[29]P. F. Z. Zhang, R. Rajavel, and P. Deelman, IEEE Microwave Wireless Compon. Lett. **21**, 267 (2011).
[30]A. Luukanen, E. N. Grossman, H. P. Moyer, and J. N. Schulman, in *2004 IEEE Lester Eastman Conference on High Performance Devices* (IEEE, 2004), pp. 40–45.
[31]T. Takahashi, M. Sato, Y. Nakasha, and N. Hara, in *2013 International Conference on Indium Phosphide and Related Materials (IPRM)* (IEEE, 2013), pp. 1–2.
[32]T. Takahashi, M. Sato, Y. Nakasha, and N. Hara, in *2012 International Conference on Indium Phosphide and Related Materials (IPRM)* (IEEE, 2012), pp. 95–98.
[33]P. Fay, J. N. Schulman, S. Thomas III, D. H. Chow, Y. K. Boegeman, and K. S. Holabird, IEEE Electron Device Lett. **23**, 585 (2002).
[34]R. G. Meyers, P. Fay, J. N. Schulman, S. Thomas III, D. H. Chow, J. Zinck, Y. K. Boegeman, and P. Deelman, IEEE Electron Device Lett. **25**, 4 (2004).
[35]J. N. Schulman, E. T. Croke, D. H. Chow, H. L. Dunlap, K. S. Holabird, M. A. Morgan, and S. Weinreb, Tech. Dig. - IEEE Int. Electron Devices Meet. **2001**, 35.1.1–35.1.3.
[36]M. Patrashin, N. Sekine, A. Kasamatsu, I. Watanabe, I. Hosako, T. Takahashi, M. Sato, Y. Nakasha, and N. Hara, in *2012 37th International Conference on Infrared, Millimeter, Terahertz Waves (IRMMW-THz)* (IEEE, 2012), pp. 1–2.
[37]T. Takahashi, M. Sato, Y. Nakasha, and N. Hara, Appl. Phys. Express **5**, 094201 (2012).
[38]S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (Wiley-Interscience, 2007).
[39]S. Agarwal, J. T. Teherani, J. L. Hoyt, D. A. Antoniadis, and E. Yablonovitch, IEEE Trans. Electron Devices **61**, 1599 (2014).
[40]S. Agarwal and E. Yablonovitch, IEEE Trans. Electron Devices **61**, 1488 (2014).
[41]C. P. Kuo, J. S. Yuan, R. M. Cohen, J. Dunn, and G. B. Stringfellow, Appl. Phys. Lett. **44**, 550 (1984).
[42]K. W. Carey, Appl. Phys. Lett. **46**, 89 (1985).
[43]B. T. McDermott, E. R. Gertner, S. Pittman, C. W. Seabury, and M. F. Chang, Appl. Phys. Lett. **68**, 1386 (1996).
[44]M. J. Cherng, R. M. Cohen, and G. B. Stringfellow, J. Elecron. Mater. **13**, 799 (1984).
[45]L. Yang, M. T. Bulsara, K. E. Lee, and E. A. Fitzgerald, J. Cryst. Growth **324**, 103 (2011).
[46]Q. Xie, J. E. Van Nostrand, J. L. Brown, and C. E. Stutz, J. Appl. Phys. **86**, 329 (1999).
[47]M. W. Wang, D. A. Collins, T. C. McGill, R. W. Grant, and R. M. Feenstra, J. Vac. Sci. Technol., B: Microelectron. Nanometer Struct. - Process., Meas., Phenom. **13**, 1689 (1995).
[48]A. Jandl, M. T. Bulsara, and E. A. Fitzgerald, J. Appl. Phys. **115**, 153503 (2014).