Nanometer-Scale Vertical-Sidewall Reactive Ion Etching of InGaAs for 3-D III-V MOSFETs

Xin Zhao, *Student Member, IEEE*, and Jesús A. del Alamo, *Fellow, IEEE*

***Abstract*— This letter introduces a novel inductively coupled plasma-reactive ion etching (ICP-RIE) technique based on a $BCl_3/SiCl_4/Ar$ chemistry for fabricating sub-20 nm diameter InGaAs nanowires with smooth, vertical sidewall and high aspect ratio (>10). To mitigate dry-etch damage, RIE is followed by a digital etch method comprised of multiple cycles of self-limiting low power O_2 plasma oxidation and diluted H_2SO_4 rinse. Using these technologies, we demonstrate vertical InGaAs gate-all-around nanowire MOSFETs with 30 nm diameter. Digital etch improves both the subthreshold swing and peak transconductance, indicating enhanced sidewall interfacial quality. The combination of RIE and digital etch techniques proposed here is promising for future 3-D III-V MOSFETs.**

***Index Terms*— Digital etch, InGaAs, MOSFET, nanowire, reactive ion etching, top-down, vertical channel.**

I. Introduction

FUTURE CMOS scaling requires novel 3-D architecture devices, trigate and nanowire MOSFETs with structural features in the few nanometer regime [1]. Recently, InGaAs has emerged as a promising high-mobility channel material candidate to extend the CMOS roadmap [2]. In future 3-D III-V MOSFETs fabricated via top-down techniques, a dry etch process capable of defining nanometer-scale fins and nanowires (NW) in InGaAs-based heterostructures is essential Additional needs are sidewall verticality and sidewall MOS interface quality. Vertical-sidewall FinFETs are shown to have better short-channel effects than those with tapered-sidewalls and also deliver superior performance [3] Good sidewall MOS interface quality demands a smooth surface with minimum dry etch damage [2].

Dry etch of indiumcontaining III-V materials, mostly InP/InGaAsP, has been studied extensively for optical device applications [4]–[6]. High verticality and high aspect ratio have been demonstrated in a variety of chemistries including those based on CH_4/H_2 [7], Cl_2 [4], [5], [8], BCl_3 [9], [10], $SiCl_4$ [11], and HBr [6]. However, we are not aware of any demonstration of sub-20 nm features with vertical sidewalls fabricated by RIE in In-based heterostructures.

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The authors are with Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: xinzhao@mit.edu).

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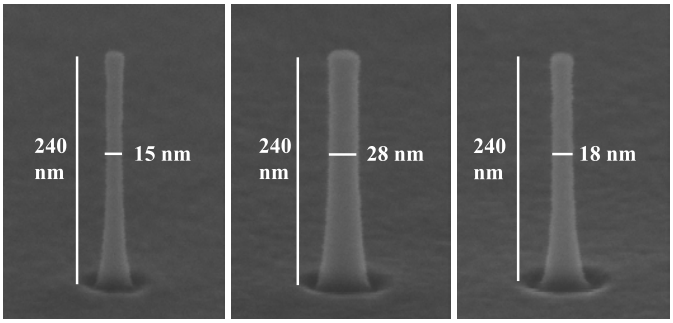

Fig. 1. (a) 15 nm diameter (D = 15 nm) InGaAs NW defined by optimized RIE technique with an aspect ratio greater than 15. (b) D = 28 nm InGaAs NW fabricated by RIE. (c) Same NW as in (b) after 5 subsequent cycles of digital etch.

In this letter, we present a novel inductively coupled plasma-reactive ion etching (ICP-RIE) technique utilizing a $BCl_3/SiCl_4/Ar$ chemistry. We choose chlorinebased gases over CH_4/H_2 or HBr based chemistries to avoid hydrogen passivation of near-surface dopants and extensive hydrocarbon polymer contamination to the chamber [7], [10]. We combine for the first time directional BCl_3/Ar plasma [10] with low-anisotropy $SiCl_4$ chemistry [11] to obtain a vertical etching profile. We demonstrate sub-20 nm diameter nanowires with vertical sidewalls and an aspect ratio greater than 10. To mitigate dry etch damage, we apply a digital etch (DE) method [12] after RIE. This combination of techniques has enabled us to demonstrate vertical nanowire InGaAs MOSFETs with 30 nm diameter (D = 30 nm) [13]. The use of DE is shown to yield improved charge control and transport Bottom-up techniques for III-V nanowire formation have been demonstrated that enable direct integration on Si substrate [14], [15]. Some of these techniques require the use of Au-seed particles [15]. Our proposed top-down approach opens the door to III-V nanowire and trigate transistors with flexible heterostructure designs fabricated using eminently manufacturable processes.

II. Experiment

The starting heterostructure consists of a 80 nm undoped $In_{0.53}Ga_{0.47}As$ channel region sandwiched between two $n+-In_{0.53}Ga_{0.47}As$ contact regions (Si-doped, $N_D = 6\times10^{19}$ cm^{-3} as measured by SIMS), grown by MOCVD on InP. The process starts with the deposition and electron-beam definition of 50 nm of hydrogen silsesquioxane (HSQ)

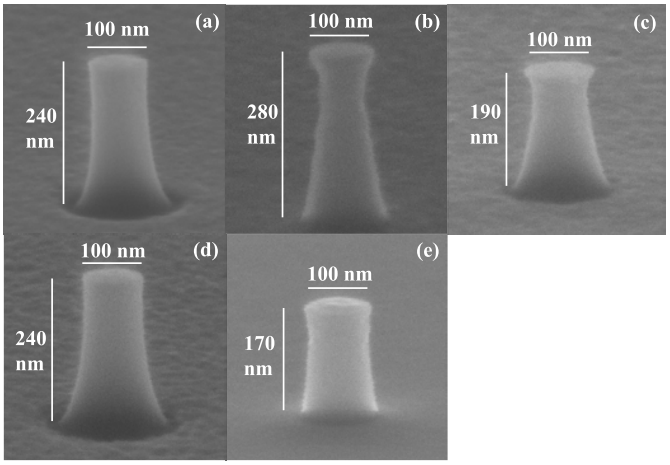

Fig. 2. InGaAs pillars etched under different RIE conditions: (a) optimum parameters (see text); (b) through (e) one parameter different from (a). (b) Chamber pressure = 0.8 Pa (vs. 0.2 Pa), (c) RF platen power = 50 W (vs. 160 W, with substrate bias voltage of 120 V vs. 280 V), (d) $SiCl_4$ flow rate = 0.25 SCCM (vs. 0.55 SCCM), (e) BCl_3/Ar flow rate = 2/12 SCCM (vs. 7/7 SCCM).

which serves as RIE mask. Dry etch is performed using $BCl_3/SiCl_4$/Ar in a SAMCO RIE-200iP ICP system with a heated chuck and backside He cooling. Samples cut into small pieces are loaded on a 6-inch ceramic carrier wafer without thermal grease. To avoid loading effects, samples with a total area of 1 cm × 1 cm are placed around the test pieces. A systematic study was performed by varying substrate temperature, gas flows, chamber pressure and RF platen power.

After nanowire formation via RIE, a digital etch process is used to eliminate near surface material that is likely to have been damaged by RIE. Unlike conventional III-V wet etch, DE method can be well-controlled because of its self-saturating nature [12]. In our approach, a DE cycle is a two-step process consisting of self-limiting low-power O_2 plasma oxidation followed by diluted H_2SO_4 rinse for oxide removal. Several cycles of DE are employed to remove the damaged material from the sidewall. The combination of RIE and DE has been used to fabricate vertical InGaAs nanowire MOSFETs [13].

III. Results and Discussion

Fig. 1(a) and (b) show D = 15 and 28 nm NWs with aspect ratio greater than 10 fabricated by optimized RIE conditions: 20 W ICP power, 160 W RF platen power (resulting in 280 V substrate bias voltage), 0.2 Pa chamber pressure, 250 °C substrate temperature and gas flows of 7/0.55/7 SCCM for BCl_3, $SiCl_4$ and Ar, respectively. The etching rate is about 1.8 nm/s (total etching time is 135 s) and the selectivity to the HSQ mask is approximately 8:1. Both NWs feature very smooth sidewalls and nearly vertical profiles. A slight footing behavior towards the bottom of the nanowire and some degree of trenching is present [5]. Further process development is needed to address these issues. Fig. 1(c) shows the same NW as in (b) after 5 cycles of DE. Each DE cycle reduces the NW diameter by ∼2 nm while preserving its overall shape.

The results shown in Fig. 1 are obtained after systematic optimization of RIE conditions. For the purpose of illustrating the role of each etch parameter, we compare InGaAs pillars etched with optimal conditions in Fig. 2(a) and non-optimal conditions in Fig. 2(b) through (e). All samples are etched for 135 s. When pressure is increased from 0.2 to 0.8 Pa in Fig. 2(b), we see a clear undercut. This is partially due to the less directional ion bombardment that results from enhanced ion collisions in the plasma under higher pressure [10]. Enhanced chemical etching also contributes to the undercut since more reactive species are produced at higher pressure [4]. A similar undercut appears when the RF platen power is decreased from 160 to 50 W (substrate bias voltage reduced from 280 to 120 V) as in Fig. 2(c) as a consequence of less directional ions. Trenching around the sidewall is greatly reduced in (b) and (c), indicating that this is related to bombarding ions bouncing off the sidewall at an angle.

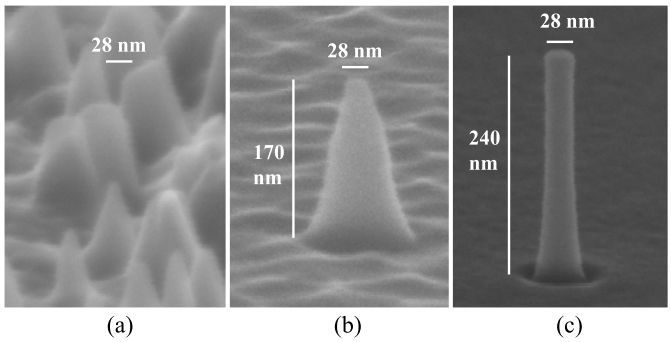

Fig. 3. Impact of substrate temperature on etching rate, profile, and surface roughness of InGaAs NWs: (a) 100 °C, (b) 175 °C, (c) 250 °C.

The BCl_3/Ar plasma alone is highly directional and causes little lateral etching [10]. Introducing $SiCl_4$ into the plasma offers more lateral etching due to its low anisotropy at low ion density [11]. This changes the profile from tapered to vertical. Without $SiCl_4$ we only obtain tapered sidewalls. This can be seen in Fig. 2(d) that features a reduced flow of $SiCl_4$.

The balance between BCl_3 and Ar affects the surface roughness and etching profile. With a higher Ar to BCl_3 ratio as in the case of Fig. 2(e), the surface roughness is decreased because of more balanced removal rates of difference elements in InGaAs due to enhanced physical sputtering. However, this enhancement leads to lower selectivity to HSQ mask (4.5:1). The etching profile also develops a slight undercut.

We show the impact of substrate temperature in Fig. 3. As the temperature is increased from 100 °C to 250 °C (other conditions unchanged), the surface roughness is greatly reduced and the sidewall becomes vertical. The rough surface and positive sloped sidewall at low temperature is caused by the residual $InCl_x$ that cannot be removed as fast as $GaCl_x$ and $AsCl_x$ due to its low volatility [8]. Increasing substrate temperature results in more balanced removal rate of In with respect to Ga and As. The overall InGaAs etch rate rises at higher substrate temperatures.

To demonstrate the suitability of the RIE+DE process to yield high aspect ratio 3D devices, we have fabricated vertical nanowire gate-all-around InGaAs MOSFETs. The process was described in [13]. We use 4.5 nm Al_2O_3 (EOT = 2.2 nm) deposited by ALD as gate oxide. The nominal channel

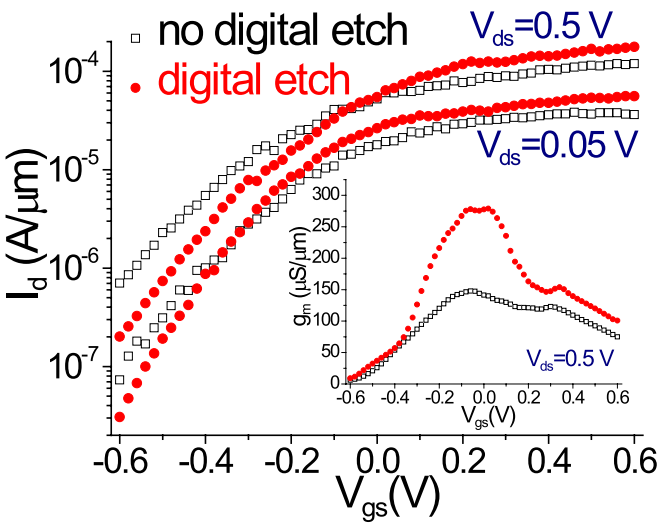

Fig. 4. Impact of digital etch on subthreshold and transconductance (inset) characteristics of D = 30 nm gate-all-around InGaAs NW-MOSFETs. 30 nm is the final device diameter.

length is 80 nm, which is set by the undoped InGaAs layer thickness.

Fig. 4 shows subthreshold and transconductance (g_m) (inset) characteristics of D = 30 nm devices with and without digital etch. I_d and g_m are normalized by the NW circumference (πD). The NW diameter after RIE is different (50 vs. 30 nm) so that after 10 cycles of DE on the thicker one, their final diameters are, within experimental uncertainty, identical and equal to 30±3 nm, as measured by SEM on pieces cleaved from the device samples. Except for DE, both samples went through the same process simultaneously, including a diluted H_2SO_4 dip prior to ALD.

The digital etch is seen to improve the interface quality as evidenced by a significant reduction in subthreshold swing (S) (at V_{ds} = 0.05 V) from 190 to 150 mV/dec. While both devices have a similar ON resistance (R_{on}) of about 760 $\Omega \cdot \mu$m, the peak g_m at V_{ds} = 0.5 V increases from 155 to 280 μS/μm indicating a significant reduction in sidewall damage by DE. ON current (I_{on}, extracted at V_{ds} = 0.5 V and gate overdrive of 1 V) with and without DE is 205 and 130 μA/μm respectively. Measurements on 10 working devices of each kind show consistent improvement in average S (155 vs. 185 mV/dec at V_{ds} = 50 mV) and g_m (150 vs. 255 uS/um at V_{ds} = 0.5 V).

As benchmarked in [13], NW-MOSFETs fabricated via the top-down etch techniques presented here match the performance of devices fabricated by bottom-up techniques [14], [15] in terms of the balance between short-channel effects and transconductance. However, g_m is still low compared to planar III-V MOSFETs [2]. This is attributed to large EOT of the gate dielectric and high series resistance (reflected in high R_{on}) that is dominated by the contact resistance. The subthreshold swing is also limited by a relatively thick gate dielectric and interface state density. Further process optimization and more aggressive device design should be instrumental in addressing the issues.

IV. Conclusion

A novel ICP-RIE process with $BCl_3/SiCl_4$/Ar is reported. Sub-20 nm InGaAs nanowires with vertical and smooth sidewalls are demonstrated under optimized etching conditions. Digital etch after RIE is shown to controllably thin nanowire diameter while preserving its general shape. To illustrate the usefulness of these techniques, we have fabricated vertical nanowire gate-all-around InGaAs MOSFETs with diameter as small as 30 nm. Digital etch improves both charge control and transport by reducing RIE damage.

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References

[1] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012.

[2] J. A. del Alamo *et al.*, "InGaAs MOSFETs for CMOS: Recent advances in process technology," in *Proc. IEDM*, 2013, pp. 24–27.

[3] A. Dixit *et al.*, "Impact of fin sidewall taper angle on sub-14 nm FinFET device performance," in *Physics of Semiconductor Devices*, V. K. Jain and A. Verma, Eds. New York, NY, USA: Springer-Verlag, 2014, ch. 2, pp. 5–8.

[4] J. S. Parker *et al.*, "High verticality InP/InGaAsP etching in Cl_2/H_2/Ar inductively coupled plasma for photonic integrated circuits," *J. Vac. Sci. Technol. B*, vol. 29, no. 1, pp. 011016-1–011016-5, Jan. 2011.

[5] S. Park *et al.*, "InGaAsP-InP nanoscale waveguide-coupled microring lasers with submilliampere threshold current using Cl_2-N_2-based high-density plasma etching," *IEEE J. Quantum Electron.*, vol. 41, no. 3, pp. 351–356, Mar. 2005.

[6] Y. S. Lee *et al.*, "Smooth, anisotropic etching of indium containing structures using a high density ICP system," in *Proc. Int. Conf. Indium Phosphide Rel. Mater.*, 2003, pp. 78–79.

[7] I. Adesida *et al.*, "Nanostructure fabrication in InP and related compounds," *J. Vac. Sci. Technol. B*, vol. 8, no. 6, pp. 1357–1360, Jul. 1990.

[8] D. J. Thomas *et al.*, "High density plasma etch processes for the manufacture of optoelectronic devices based on InP," in *Proc. Int. Conf. Compound Semicond. Manuf. Technol.*, 2001, pp. 172–174.

[9] J. Hong *et al.*, "Comparison of ECR plasma chemistries for etching of InGaP and AlGaP," *J. Electron. Mater.*, vol. 26, no. 11, pp. 1303–1309, Nov. 1997.

[10] T. Maeda *et al.*, "Inductively coupled plasma etching of III-V semiconductors in BCl3-based chemistries: II. InP, InGaAs, InGaAsP, InAs and AlInAs," *Appl. Surf. Sci.*, vol. 143, nos. 1–4, pp. 183–190, Apr. 1999.

[11] J. Etrillard *et al.*, "Anisotropic etching of InP with low sidewall and surface induced damage in inductively coupled plasma etching using $SiCl_4$," *J. Vac. Sci. Technol. A*, vol. 15, no. 3, pp. 626–632, May 1997.

[12] J. Lin *et al.*, "A novel digital etch technique for deeply scaled III–V MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 440–442, Apr. 2014.

[13] X. Zhao *et al.*, "Vertical nanowire InGaAs MOSFETs fabricated by a top-down approach," in *Proc. IEDM*, 2013, pp. 695–698.

[14] K. Tomioka, M. Yoshimura, and T. Fukui, "A III-V nanowire channel on silicon for high-performance vertical transistors," *Nature*, vol. 488, no. 7410, pp. 189–192, 2012.

[15] K. M. Persson *et al.*, "Vertical InAs nanowire MOSFETs with IDS = 1.34 mA/μm and gm = 1.19 mS/μm at VDS = 0.5 V," in *Proc. 70th Device Res. Conf.*, 2012, pp. 195–196.