Microelectromechanical Relay and Logic Circuit Design for Zero Crowbar Current

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***Abstract*— A compact microelectromechanical (MEM) switch design and associated family of logic gates, memory cells, and other basic very-large-scale integration (VLSI) digital circuit sub blocks are proposed to ensure zero crowbar current in addition to zero leakage current while minimizing mechanical delay. The circuit design methodology introduced in this paper also provides for lower device count and hence lower operating power consumption. A prototype of the MEM switch design is demonstrated.**

***Index Terms*— Complementary logic, crowbar current, microelectromechanical (MEM) relay, pass-gate logic, zero leakage.**

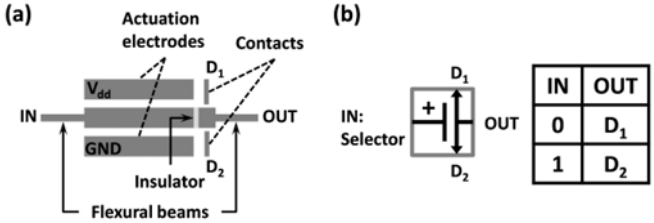

Fig. 1. MEM logic switch. (a) Schematic illustration showing the biasing scheme. (b) Circuit symbol used in this paper and truth table.

I. Introduction

MICROELECTROMECHANICAL (MEM) switches (relays) recently have attracted considerable attention [1], [2] because they have the ideal characteristics of zero off-state leakage current and perfectly abrupt current-versus-voltage characteristic (i.e., zero sub-threshold swing, $SS = 0$), so that they potentially can overcome the energy efficiency limit of complementary metal–oxide–semiconductor (CMOS) transistor technology [3], [4]. In light of trends toward multiple-core architectures and 3-D integration for microprocessor unit (MPU) and System-on-Chip (SoC) products [5], [6], relays also have been proposed for heterogeneous integration with CMOS to gate power supply [7] and to improve the performance-area trade-off [8]. Since they require only metallic structures/electrodes and air gaps, they can, in principle, be fabricated with an advanced back-end-of-line (BEOL) process [9].

Because of their abrupt switching behavior, process-induced variations in switching voltage and/or switching time can temporarily result in a direct current path (short circuit) between the power supply and ground, if a relay-based digital circuit is implemented using the conventional complementary logic circuit topology in which there is at least one pull-up device connected between the output node and power supply and at least one pull-down device connected between the output node and ground [10]. The resultant crowbar current results in a component of dynamic power consumption that can be much larger than that for a CMOS implementation since transistors have gradual switching behavior [11]. It should be noted that the turn-OFF time for a relay is highly dependent on contact adhesion [12]; the greater the contact adhesion, the longer the turn-OFF time and hence the greater the likelihood of crowbar current during active circuit operation. A dielectric coating can be applied to the contacting electrode surfaces [13] to assuage this issue at the tradeoff of increased on-state resistance (degraded circuit operating speed).

To address this fundamental issue for relay-based digital logic circuits, an alternative design methodology that eliminates the possibility of crowbar current while maintaining good performance and zero standby power consumption is described herein. This work codifies the techniques presented in [14] and includes memory cell designs as well as additional VLSI digital circuit sub blocks. The MEM switch design and associated family of logic gates, combinational logic circuits, and memory cells are introduced in Section II. Fabrication and characterization of a prototype switch are described in Section III. Conclusions from this paper are summarized in Section IV.

II. MEM Logic Technology and Circuit Design

The MEM logic switch design is an electrostatically actuated single-pole/double-throw (SPDT) relay with an insulated input electrode, shown in Fig. 1(a).

The single-pole structure is suspended by flexural suspension beams at its two ends and comprises an input electrode, thin insulator, and output electrode. The two actuation

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TABLE I
MEM LOGIC CIRCUIT CONFIGURATION RULES

#	TERMINAL	RULE
R1	Actuation electrodes	One of each must be biased at V_{dd} and GND so that *OUT* is always connected to a data terminal in steady state.
R2	*IN*	Must be driven to either V_{dd} or GND to avoid indeterministic *OUT*, *i.e.* cannot be floated.
R3a	*OUT*	Must not be connected to a voltage source (V_{dd} or GND) when either D_1 or D_2 is connected to a voltage source. Can be connected to the output terminal of another switch **only** when one of D_1, D_2 is floated and the two switches operate in a complementary manner (such that only one switch is charging/discharging *OUT* at a time).
R3b	*OUT*	Can be connected to *IN*, D_1 or D_2 of a switch.

electrodes located on either side of the suspended input electrode (IN) are biased at the supply voltage (V_{dd}) and ground (GND), respectively; the output electrode (OUT) contacts one of two data electrodes (D_1 and D_2), depending on the input voltage. V_{dd} must be sufficiently large to cause OUT to come into contact with D_1 when the voltage applied to IN is GND. The circuit symbol and truth table (wherein "0" $\equiv$ GND and "1" $\equiv V_{dd}$) for this switch are shown in Fig. 1(b); the actuation electrode biased at V_{dd} is denoted by "+" in the circuit symbol. Note that the MEM logic switch implements the multiplexer function; $\mathrm{OUT} = \overline{\mathrm{IN}} \cdot D_1 + \mathrm{IN} \cdot D_2$. The circuit configuration rules for this device are summarized in Table I.

A. Basic Logic Gates and Combinational Logic Designs

Fig. 2 shows how the MEM logic switch can be used to implement any basic logic function. One of the requirements for combinational logic is single-stage operation, i.e., the operation should be carried out within one clock cycle (one mechanical switching delay [15]). Examples are shown in Fig. 3(a) and (b) for multiple-input AND and OR functions, respectively, in which intermediate results are carried out by OUT terminals each connected to a D_1 or D_2 (rather than IN) electrode of another switch. A 2^N:1 multiplexer (MUX) is easily implemented using $N(N+1)/2$ switches, by feeding OUT of the previous stage into D_1 or D_2 of the next stage, as shown in Fig. 3(c). An N-bit decoder can be implemented using $2^{N+1} - 2$ relays, by alternating the polarity of the actuation electrodes for a 0 versus 1 input bit and then feeding OUT into D_1 or D_2 of the next lower bit, as shown in Fig. 3(d). As shown in Fig. 4, a single-stage carry-generation and adder circuit suited for a carry-look ahead adder [16] can be realized with only four and eight MEM switches, respectively, by multiplexing AND, OR, XOR and XNOR outputs.

Since each of these logic gates is single-stage, their mechanical switching delay does not depend on the number of inputs. Their electrical (capacitive charging/discharging, or *RC* delay increases with N, however. Due to the relatively large mechanical switching delay (>0.1 ns), the insertion of buffers (BUF) to reduce the electrical delay is only beneficial if N is very large (>100) [17], since an additional mechanical switching delay would be incurred.

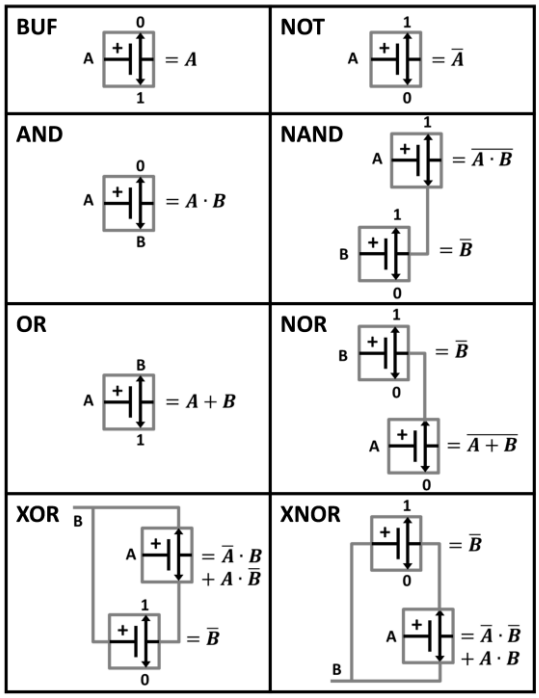

Fig. 2. Basic MEM logic gates.

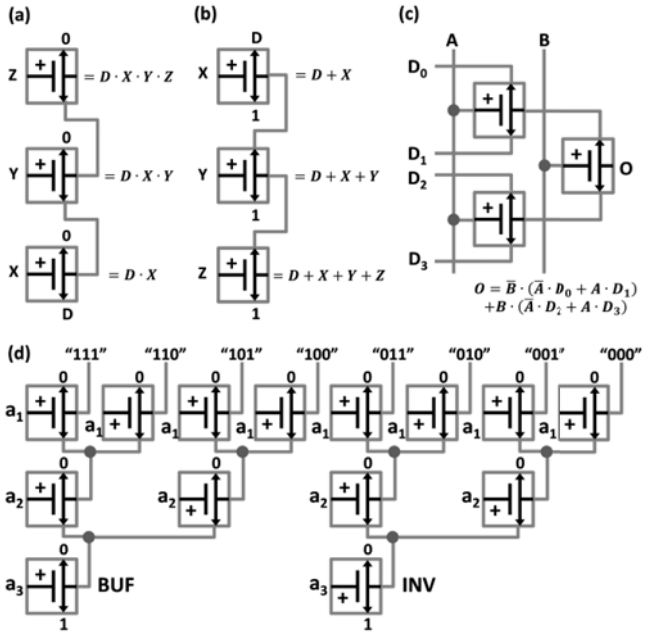

Fig. 3. MEM-based combinational logic gates. (a) 3-input AND. (b) 3-input OR. (c) 3-to-1 MUX. (d) 3-bit decoder.

Table II compares the number of switching devices used to implement various logic functions, for CMOS versus relay technologies. It can be seen that the circuit design methodology introduced in this paper provides for the lowest device count, and therefore, potentially the lowest active power consumption. It also avoids the need to generate complementary signals, in contrast to the pass-gate logic design methodology used in [16].

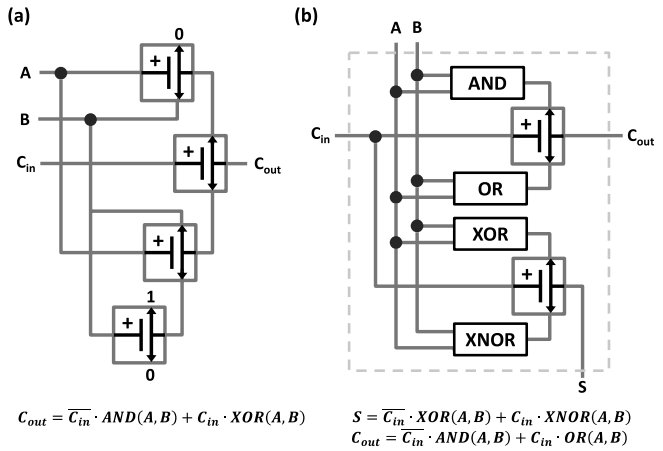

Fig. 4. MEM-based (a) carry-generation, (b) full-adder circuit, with AND, OR, XOR, and XNOR referring to Fig. 2.

TABLE II
DEVICE COUNT COMPARISON

FUNCTION	CMOS	RELAYS [16]	THIS WORK
BUF	4	2	1
NOT	2	2	1
NAND	4	4	2
XOR	6	6	2
MUX	8	8	1
Carry-gen.	8	8	4
Full-adder	24	12	8
SRAM/bit	6-8	4	2-3
DRAM/bit	1	3	3

B. Memory Cell Designs: SRAM and DRAM

In a conventional six-transistor (6T) SRAM cell design, an inverter (which provides the feedback necessary to latch data) and a pass-gate switch (which is used to write data into the latch) share an output terminal; this is in conflict with MEM circuit configuration rule R3a. The relay-based static latch design presented in [16] also violates this rule, since it connects output terminals together at the data node. To avoid the possibility of a direct current path between V_{dd} and GND, the feedback (FB) loop must be disconnected while the storage node (SN) is being driven through the pass-gate (PG). Only when the FB output is guaranteed to be the same as the PG output, can these be connected together. A cell design that meets these requirements, operated with two word-lines (WL) and one bit-line (BL), is presented in Fig. 5(a). As can be seen from the timing diagram, it takes five clock cycles (disconnect FB loop; turn ON PG to drive SN; propagate data through FB device; connect FB loop; turn OFF PG) to write and one cycle to read. In contrast, it takes two/one clock cycles for write/read operation of a CMOS 6T-SRAM cell.

If the voltages applied to the actuation electrodes of an MEM switch are equal (intentionally violating configuration rule R1), then the output electrode will float in between D_1 and D_2 if the structure is designed such that the spring restoring force of the suspension beams is greater than the contact adhesive force plus any difference in electrostatic force between the two actuation electrodes. (Ordinarily, OUT is in contact with either D_1 or D_2, so that the actuation gap sizes are not equal; this results in net electrostatic force when the voltages applied to the actuation electrodes become equal.) Thus, this device can be made to function as a tri-state switch, if one of the actuation electrodes is used as an additional input terminal. This enables an SRAM cell to be realized with only two relays, as shown in Fig. 5(b). As can be seen from the timing diagram, it takes four clock cycles (float SN; turn ON PG to drive SN; latch data; turn OFF PG) to write and one cycle to read.

MEM-based DRAM cells have been demonstrated in a NAND-style column configuration that leverages series resistance to reduce short-circuit current and utilizes gate (switch input) capacitance to store charge [16]. An alternative MEM-based DRAM cell design that avoids large *RC* delay, consisting of three relays operated with two WLs and one BL (also utilizing switch input capacitance to store data), is presented in Fig. 5(c). The second WL (WL_1) is required to read out data from the selected cell and to isolate the unselected cells sharing the same BL. It should be noted that the storage node can be completely isolated by a mechanical switch (with zero off-state leakage current), so that very long retention time is expected.

Table III summarizes the read and write times for the MEM-based memory cells, in comparison with CMOS-based memory cells.

III. EXPERIMENT

In this section, MEM logic switch design considerations are firstly discussed. Then the fabrication process and measured characteristics of a prototype MEM switch are presented.

A. Switch Design Considerations

To guarantee that the state of the switch is determined solely by the voltage on the input electrode, the actuation electrodes should have fixed bias voltages (V_{dd} and GND) and should be much longer than the data electrodes in the contacting regions (i.e., the actuation area should be much larger than the apparent contact area) so that the voltages on the data electrodes do not exert significant electrostatic force on the movable structure.

A simple linear spring model of the beam (with effective spring constant k_{eff} and maximum deflection g_d) elucidates two minimum requirements for the operating voltage V_{dd}, as shown in Fig. 6: 1) the voltage must be sufficiently large so that the electrostatic force is greater than the contact adhesive force minus the spring restoring force ($k_{eff} \cdot g_d$) of the deflected beam, to pull the output electrode out of contact with a data electrode and 2) the voltage must be sufficiently large so that the electrostatic force is sufficient to pull the output electrode into contact with the other data electrode. Clearly, there is an optimum value of $k_{eff} \cdot g_d$ for minimum V_{dd}.

The actuated portion of the input electrode should be significantly wider (i.e., stiffer) than the flexural-beam portion, as shown in Fig. 7(a) so that it does not bend into contact with an actuation electrode, to ensure an insulated input electrode. Simulation results show that the voltage needed to pull-in the output electrode to a data electrode depends on the width of only the flexural-beam portion if it is narrower than the actuated "plate" portion [Fig. 7(b)]. k_{eff} can be tuned across

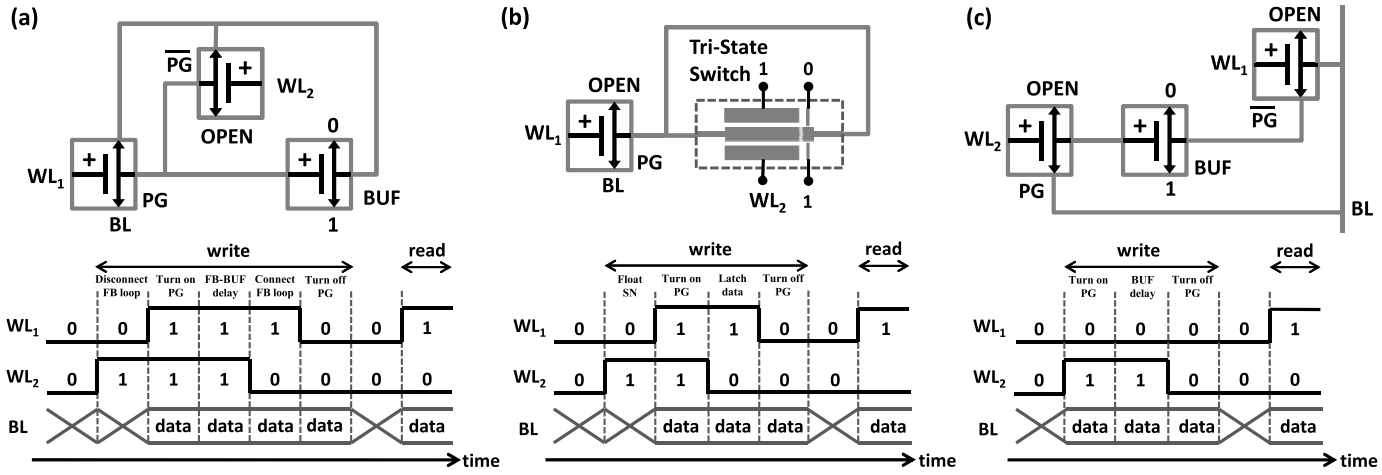

Fig. 5. MEM-based memory cells, each operated with two word-lines (WL) and one bit-line (BL). (a) 3-relay-SRAM cell. (b) 2-relay-SRAM cell (one of the relays is operated in tri-state which enables floating output) and (c) 3-relay-DRAM cell. The supplemental pass-gate ($\overline{\text{PG}}$) is used (a) to connect/disconnect FB loop and (c) to read out data, respectively.

TABLE III
MEMORY CELL OPERATION CLOCK CYCLES

DEVICE	CELL	WRITE	READ
SRAM	6-transistor(T)	2	1
	3-relay	5	1
	2-relay	4	1
DRAM	1T-1C	1	1
	3-relay	3	1

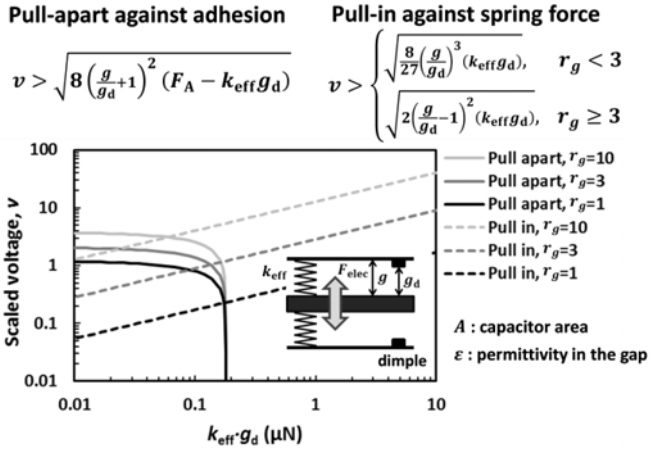

Fig. 6. Scaled actuation voltage $v = V_{dd}/\sqrt{g_d^2/\varepsilon A}$ required to pull the output electrode out of contact with the data electrode (solid lines) or to actuate the beam into contact, against the spring force (dashed lines), as a function of $k_{\text{eff}} \cdot g_d$, where $r_g = g/g_d$. Adhesion force of 1.8 nN/nm^2 for TiO_2-coated surfaces [18] with apparent contact area of 100 nm^2 is assumed.

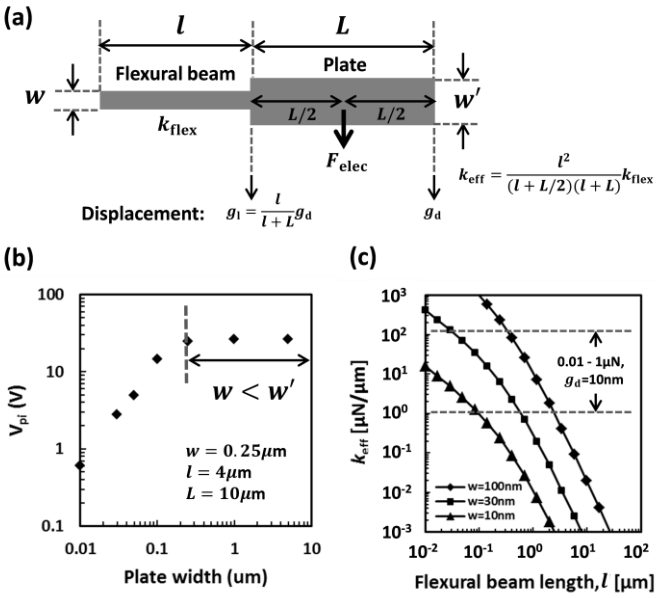

Fig. 7. (a) Schematic illustration of the input electrode beam design. (b) Simulated pull-in voltage as a function of plate width (w), for an actuation gap $g = 0.55$ μm. (c) Impact of flexural-beam design parameters on k_{eff}, with plate length $L = 0.5$ μm, layer thickness $= 0.2$ μm, Young's modulus $= 411$ GPa (corresponding to Tungsten).

a wide range of values by adjusting the dimensions of the flexural-beam portion [Fig. 7(c)], to achieve the optimal value of $k_{\text{eff}} \cdot g_d$ for minimum operating voltage (Fig. 6).

Two prototype MEM switch designs are shown in Fig. 8, representing two approaches to routing the output signal. If the output signal is directly routed through the suspended output electrode as shown in Fig. 8(a), a long (very compliant) suspension beam is needed so that it does not substantially increase k_{eff}. To eliminate the need to doubly clamp the structure, the output signal can be routed via an additional set of contacts to a fixed output electrode as shown in Fig. 8(b). For example, when the voltage applied to IN is GND, the suspended output electrode will be deflected into contact with both D_1 and the fixed output electrode (OUT). It should be noted that this switch design is a variant of the laterally actuated 6-T relay design in [14], which is identical in function to the vertically actuated seesaw relay design introduced in [19] and experimentally demonstrated to perform basic logic functions in [20] consistent with Fig. 2.

B. Prototype Switch Fabrication

The schematic cross section in Fig. 9(a) shows the layers used to fabricate prototype MEM switches in this paper. The key steps of the 2-mask fabrication process are as

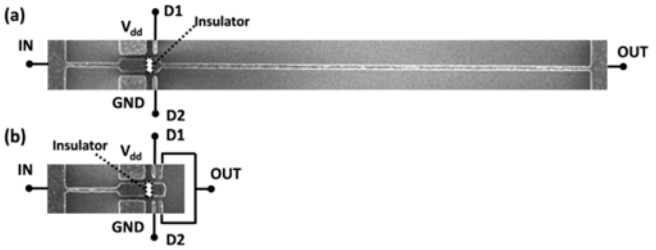

Fig. 8. Plan-view scanning electron micrographs of fabricated prototype SPDT MEM switch designs comprising two actuation electrodes biased at V_{dd} and GND. (a) Single-contact design which requires a flexural connection to the output electrode. (b) Double-contact design which eliminates the need for a flexural connection to the output electrode. The location of the insulator is highlighted in white.

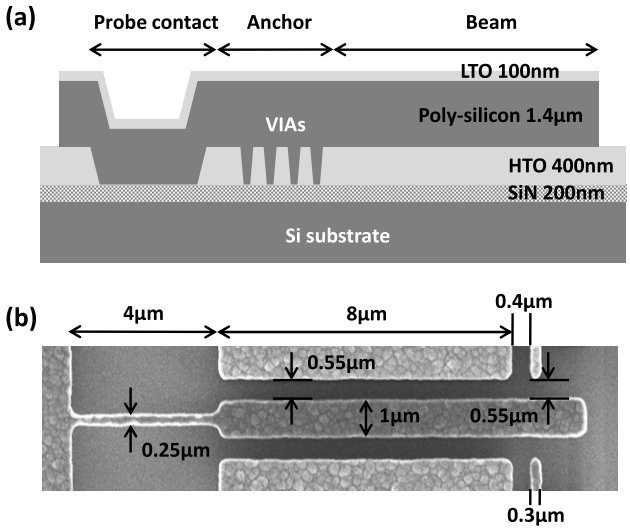

Fig. 9. (a) Schematic cross section of the beam structure prior to removal of the oxide layers (HTO and LTO) in diluted HF solution. (b) SEM plan-view image of the beam area of the fabricated MEM switch.

follows: 200 nm of silicon nitride (SiN_x) was deposited to form an insulating substrate coating that is resistant to the wet etch process (20 min. in 25:1 diluted HF solution) used to release the structure; structural anchor regions were defined by etching contact holes 0.25 μm in diameter through the 400-nm-thick layer of sacrificial high-temperature-deposited oxide (HTO), which is sufficiently small to be filled by low-pressure chemical vapor deposition of 1.4 μm-thick phosphorus-doped polycrystalline silicon (poly-Si) to achieve a planar surface topography; 100 nm of low-temperature-deposited oxide (LTO) was used as a hard mask to etch the poly-Si with better selectivity and hence to achieve more vertical sidewalls (which are important for achieving uniformly small actuation gap sizes), and was selectively removed together with the HTO during the release etch process.

Fig. 9(b) shows a plan-view scanning electron microscopy (SEM) image of a fabricated device with plate dimensions 10 μm-length and 1 μm-width, flexural beam dimensions 4 μm-length and 250-nm-width, and actuation gap size 550 nm. The insulator between the input and output electrodes was omitted in this initial experiment, but can be easily incorporated by forming a trench in the structure (using an additional mask) and filling it with an HF-resistant dielectric material such as SiN_x.

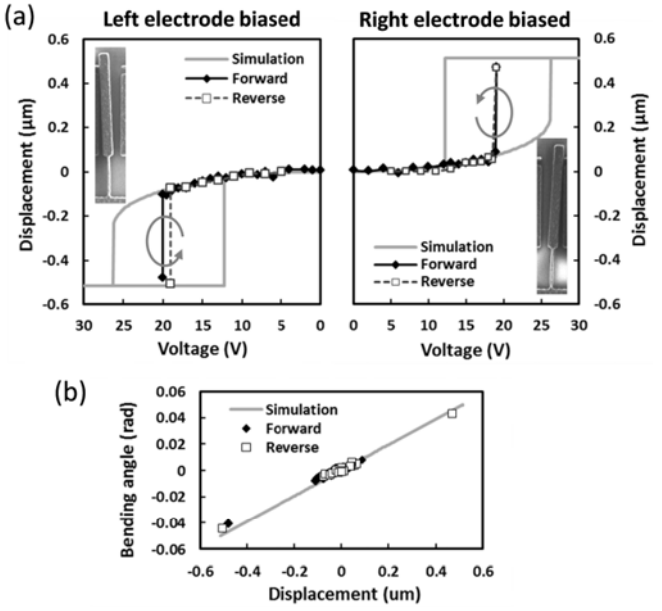

Fig. 10. Comparison of simulated and measured results. (a) Lateral beam displacement as a function of the voltage applied between the beam (biased at GND) and an actuation electrode and (b) bending angle as a function of beam displacement.

C. Results and Discussion

Aluminum wires were bonded to the probe pads to allow voltages to be applied to the device (specifically, the input electrode and one actuation electrode) while under observation in an SEM chamber to monitor the displacement of the beam. Fig. 10(a) shows that pull-in occurs when the voltage applied between the beam and actuation electrode is increased to 20 V and that pull-out occurs with unexpectedly low hysteresis, when the applied voltage is reduced to below 19.5 V. The experimentally observed pull-in/pull-out voltages are intermediate to their simulated values; this may be explained by electron beam charging (by up to 5 V) of the sample in the SEM chamber. Note that structural bending occurs primarily in the narrow flexural beam portion, so that the measured bending angle well matches the simulated bending angle [Fig. 10(b)].

The electrical measurements shown in Fig. 11(a) for a device with 0.25 μm actuation gap show symmetric and abrupt switching behavior, as required for proper circuit functionality with zero crowbar and leakage currents. (Unfortunately, the switching was not repeatable due to contact welding which occurred when the native oxide was broken down by applying 2.5 V between the beam and the data electrode, as shown in Fig. 11(b). To mitigate this problem, an ultrathin TiO_2 coating can be applied by atomic layer deposition after the structure is released, as was done in [13]).

D. 3-D Switch Design for Reduced Footprint

Ideally, the lateral dimensions of the MEM logic switch should be proportionately scaled down to reduce its footprint. Lithographic limits make it difficult to scale down the width of the flexural beam and the gap sizes, however, which in turn limit the extent of beam-length scaling [21]. One approach

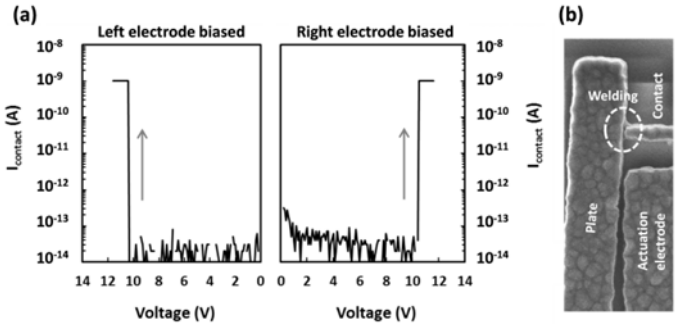

Fig. 11. (a) Measured I–V curves for a device with actuation gap size 0.25 μm, for voltage applied to the left or right actuation electrodes (with compliance current set at 1 nA). (b) SEM image showing welding at the contact biased at 2.5 V to break through the native oxide.

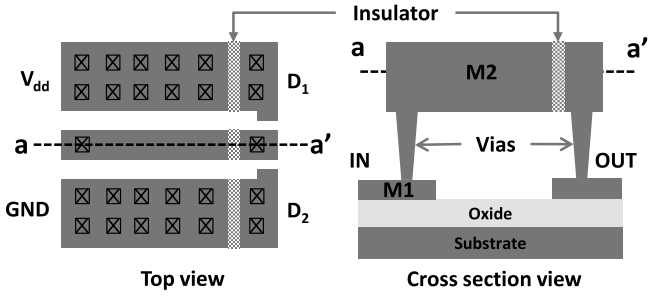

Fig. 12. Optimum beam structure using the stiffness of the via using two metal layers (M1, M2).

to overcome this challenge is to use a 3-D structure that leverages the BEOL process. As shown in Fig. 12, the vias used to form electrical connections to the input electrode and the output electrode can serve as torsional/flexural elements. As in the planar switch design, the output terminal is actuated into contact with one of the data electrodes by applying a voltage to the input electrode located between two biased actuation electrodes. The effective spring constant of this structure is determined by the via material and dimensions.

IV. Conclusion

Due to the abrupt switching characteristic of MEM relays, a direct current path can be temporarily formed between power supply and ground as a result of variations in relay turn-ON/turn-OFF voltages and/or delays if a conventional complementary logic circuit topology is used. To eliminate this issue, a compact MEM switch design and logic circuit design methodology is proposed to ensure zero crowbar current as well as zero leakage current with minimal mechanical delay. A complete family of basic logic gates and combinational logic units, as well as SRAM and DRAM memory cells, can be implemented with the MEM switch design following the methodology described herein. A prototype MEM switch is demonstrated with the key characteristic of symmetric actuation. Evolution to a 3-D switch design leveraging the BEOL process can facilitate reductions in footprint.

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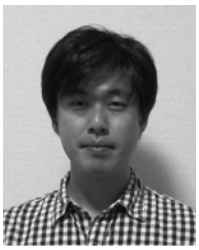

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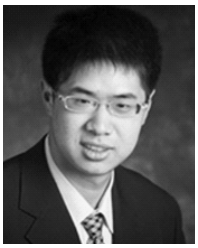

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