High-Gain Inverters Based on WSe_2 Complementary Field-Effect Transistors

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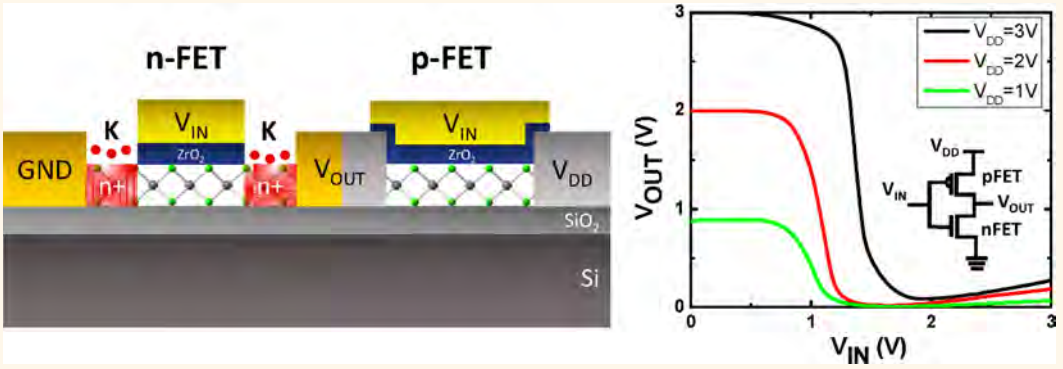
ABSTRACT



In this work, the operation of n- and p-type field-effect transistors (FETs) on the same WSe_2 flake is realized,and a complementary logic inverter is demonstrated. The p-FET is fabricated by contacting WSe_2 with a high work function metal, Pt, which facilities hole injection at the source contact. The n-FET is realized by utilizing selective surface charge transfer doping with potassium to form degenerately doped n+ contacts for electron injection. An ON/OFF current ratio of $>10^4$ is achieved for both n- and p-FETs with similar ON current densities. A dc voltage gain of >12 is measured for the complementary WSe_2 inverter. This work presents an important advance toward realization of complementary logic devices based on layered chalcogenide semiconductors for electronic applications.

KEYWORDS: transition metal dichalcogenides · digital circuits · monolayer semiconductors · complementary logic · CMOS electronics

Continued scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) has enabled lower operating voltages, faster switching speeds, and enhanced computation power. However, as the channel length of MOSFETs approaches the sub-10 nm regime, severe short channel effects deteriorate the switching performance of the planar devices. In this regard, multiple device architectures have been proposed for enhanced gate coupling and reduced short channel effects. One approach involves the use of an ultrathin-body semiconductor, where the entire thickness of the active channel is in close proximity to the gate electrode, thereby enhancing the gate control of the channel.[1,2] As a rule of thumb, the thickness of the semiconductor should be kept to ~<1/3 of the gate length for effective gate coupling of the device. For ultrashort channel devices, this corresponds to a semiconductor thickness on the order of only a few atomic layers. This aggressive scaling possesses significant challenges since at such thicknesses any variation of the thickness, at the atomic scale, yields severe surface potential variation and thereby enhanced surface roughness scattering of the carriers. Layered transition metal dichalcogenides (TMDCs), such as MoS_2 and WSe_2, have been investigated as a promising material class for future scaled devices, owing to their inherent thickness uniformity and control down to a monolayer.[3−5] TMDC FETs have exhibited excellent metrics such as ON/OFF current ratios of up to 10^8,[3] subthreshold swings of 60 mV/dec,[4] and electron and hole

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mobilities of >100 $cm^2/(V\ s)$.[4,6] To date, both n- and p-type transistors have been demonstrated on different flakes of MoS_2 and WSe_2 through contact engineering by using either low/high work function metals and/or surface charge transfer doping.[4,6−9] TMDC logic gates have also been demonstrated based on n-type MoS_2 FETs[10−12] and resistor-loaded WSe_2 devices.[13] Moving forward, the demonstration of n- and p-type transistors on the same substrate is needed to enable low-power complementary MOS (CMOS) logic circuits given their performance advantage over unipolar logic circuits. Building on the recent advancements described above, here, we report the first operation of n- and p-FETs on the same WSe_2 flake, thereby enabling the realization of TMDC CMOS logic gates.

The polarity of a MOS transistor is determined by the type of carriers (*i.e.*, electrons *versus* holes) that the source contact can supply to the semiconductor channel. In conventional MOSFETs, this is achieved through formation of degenerately doped n+ and p+ S/D contacts for n- and p-type operation, respectively. On the other hand, in Schottky barrier (SB) MOSFETs, where metal contacts are fabricated directly on top of the channel, the polarity is governed by the Schottky barrier height (and width) for electrons and holes at the source electrode. A low SB height to the conduction band yields electron injection into the channel, thereby resulting in n-type device operation. Similarly, a low SB height to the valence band yields p-type characteristics. Heavy doping of the semiconductor region in the proximity of the contacts can reduce the SB widths, thereby enabling efficient electron or hole injection through the SBs by a tunneling process. This results in a device configuration that resembles the conventional MOSFETs. Note that in all cases the effect of channel doping is to simply control the threshold voltage of the device along with the contact electrostatics for short channel effects.

The most commonly utilized device configuration for TMDCs is the SB-MOSFET structure, with the two most explored materials being MoS_2 and WSe_2. Given the low conduction band edge position (*i.e.*, large electron affinity) of MoS_2 and the Fermi level pinning near the conduction band edge at the metal interfaces, most MoS_2 SB-MOSFETs fabricated to date have been n-type. On the other hand, the high valence band edge position of WSe_2 readily results in p-type operation. Thus, to achieve robust CMOS operation based on a single channel material system, the contacts need to be degenerately doped, at least for one polarity depending on whether MoS_2 or WSe_2 is utilized. In this work, we focus on WSe_2 as the semiconductor material. We achieve p-FETs by using high work function Pt contacts configured in a SB-MOSFET geometry. On the other hand, n-FETs are obtained by degenerate doping of the underlapped contact regions. This configuration provides us with a platform to fabricate WSe_2 CMOS devices and logic gates.

Chemical doping of TMDCs, up to the degenerate level, has been previously reported by our group using surface charge transfer processes. Given the molecular thickness of TMDCs, by simply placing electron-donating or -withdrawing species on their surfaces, n- and p-type doping can be obtained, respectively, at degenerate carrier concentrations.[4,8] This principal is similar to the doping process that has been extensively explored in the past for organic semiconductors,[14] carbon nanotubes,[15−17] graphene,[18] and nanoscale III−Vs.[19] Surface charge transfer doping is distinct from substitutional doping since there is no replacement of lattice atoms, which is of advantage for nanoscale materials, where substitutional doping can lead to large stochastic variation given the small number of atoms involved. Our previous work has shown that NO_2 and potassium serve as efficient electron-withdrawing and -donating species for WSe_2, respectively.[4,8] By patterning the surface of TMDCs prior to exposure to the dopants, doping profiling along the length of TMDCs can be readily obtained, thereby enabling fabrication of p- or n-FETs with degenerately doped contacts. Here, we utilize patterned K doping for selective n+ doping of the contacts of the n-FETs.

Contacting the conduction band of WSe_2 with elemental metals is challenging;[7] hence we used surface charge transfer doping to form degenerately doped *n*+ contact regions. To achieve patterned doping of the n+ contacts, a gate structure underlapping the S/D electrodes is fabricated for the n-side, which acts as a mask for the subsequent doping process. On the other hand, an overlapped gate structure is formed on the p-side. The overlapped top gate structure of the p-FET protects the integrity of the p-side channel during potassium doping. On the other hand, the exposed WSe_2 regions near the metal electrodes of the n-side are exposed to K atoms, leading to the formation of n+ contacts on either side of the gate. The heavy n-doping of the contacts yields low resistance contacts to the conduction band of WSe_2 for electron injection.[8] The false color SEM image of the fabricated CMOS inverter and the device schematic are shown in Figure 1a and b, respectively. The measurements of the devices are subsequently performed *in situ*, without breaking vacuum since K doping is not air stable. In the future, exploration of air-stable dopants or encapsulation techniques are needed to enhance the stability of the devices to air exposure.

RESULTS AND DISCUSSION

Device schematics for the WSe_2 p- and n-FETs used in this work are shown in Figure 2a and b, respectively. Figure 2c shows the drain current, I_D, *versus* gate voltage, V_{GS}, curve at a drain voltage of $V_{DS} = -1$ V for a WSe_2 p-FET fabricated on a ~10 nm thick flake with Pt contacts. The channel length is $L = 2\ \mu$m and the gate electrode overlaps the S/D contacts. The device

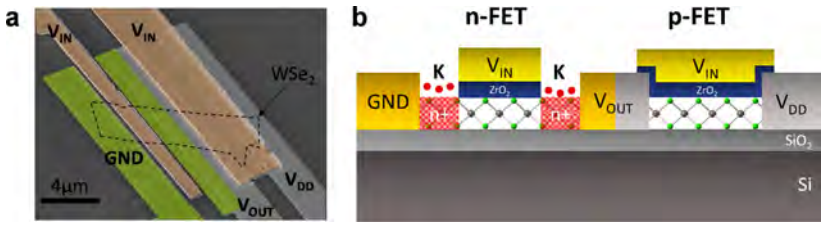

Figure 1. (a) False-color SEM image of a fabricated CMOS inverter on a single WSe_2 flake. (b) Schematic of the CMOS inverter, depicting the n- and p-FET components.

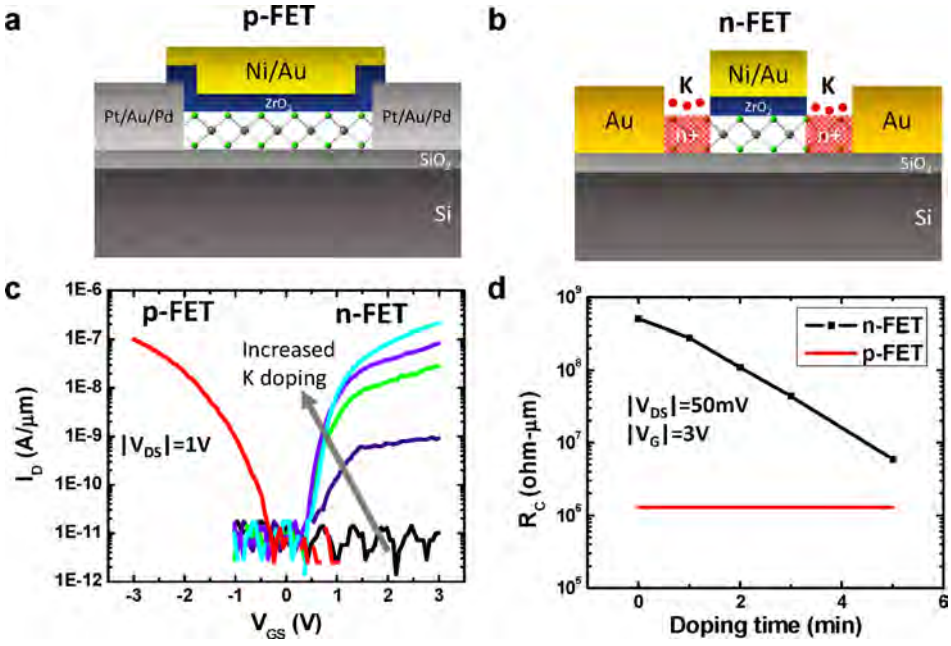

Figure 2. (a and b) Device schematics (not drawn to scale) of the WSe2 p- and n-FETs, respectively. (c) Transfer characteristics at $V_{DS} = |1\ V|$ of a WSe_2 p-FET and n-FET fabricated on the same flake as a function of potassium doping time (1, 2, 3, and 5 min). The transfer characteristics of the p-FET remain unchanged after doping due to the gate overlap structure. For clarity, only the data before doping are shown for the p-FET. (d) Extracted contact resistance, R_c, as a function of K doping time for p- and n-FETs.

exhibits clear p-type behavior with an ON/OFF current ratio of $>10^4$. The transistor has a threshold voltage (V_T) of -2 V, as extracted by the linear extrapolation of the I_D-V_{GS} curve. The negative V_T of this p-FET makes it an enhancement mode device (*i.e.*, OFF at V_{GS} = 0 V), which is desired for CMOS logic circuit fabrication. The ON-current density of this long channel device at $|V_{GS} - V_T|$ = 1 V is 0.1 μA/μm, as normalized by the width of the WSe_2 flake. This ON current, while sufficient for proof-of-concept CMOS operation demonstrated in this work, is limited by the SB to the valence band of WSe_2 at the source contact. As shown previously by our group, the ON current can be further improved by contact doping to reduce the thickness of SBs.[4] Furthermore, channel length and gate dielectric thickness down-scaling is needed to further enhance the ON-state drive currents.

The transfer characteristic of an n-type FET fabricated on the same flake as the one used for the p-FET device above is also shown in Figure 2c. Here, the I_D-V_{GS} curves at V_{DS} = 1 V are shown as a function of K doping time, up to 5 min. The channel length is 1 μm, and as discussed earlier the gate electrode underlaps the metal S/D contacts. Since the entire gate stack, including the dielectric layer, was patterned by a lift-off process, there is no dielectric layer on the surface of the underlapped WSe_2 regions, making them directly exposed to the K vapor during the doping process. The measurements are performed *in situ* under vacuum since K doping is not air stable. From Figure 2c it is clear that the n-channel conduction increases as the doping time is increased due to the thinning of the SBs to the conduction band of WSe_2. Note that, without doping, the ungated WSe_2 regions on each side of the gate exhibit high sheet resistivity due to the low carrier concentrations. In addition, in the absence of K doping, the high Schottky barrier height and width at the metal/WSe_2 junction further limits electron injection. As a result, without doping, the underlapped device delivers no current drive (limited by the instrument

noise baseline). After 5 min of exposure to K vapor, the doping was stopped by turning off the current to the potassium dispenser. At this K doping level, the ON current density is 0.2 μA/μm at $|V_{GS} - V_T| = 2$ V, approximately matching that of its p-FET counterpart. Notably, the threshold voltage remains unchanged as a function of doping time, which indicates that the doping concentration of the channel (*i.e.*, WSe_2 region underneath the gate) is not being modulated. The results suggest that the top gate stack used here serves as an effective mask and is protecting the channel from the dopants, with only the exposed underlapped regions being exposed to K. Desirable for CMOS logics, the device operates in the enhancement mode with $V_T = 1$ V. It should be noted that the transfer characteristics of the p-FET device with overlapped gate structure remained unchanged during the doping process.

A figure of merit that is often used to analyze long channel MOSFETs is the carrier mobility since it dictates the ON current drives for a given gate field in the absence of parasitic resistances. However, in the devices reported here, the contact resistances are large due to the Schottky-like nature of the metal/WSe_2 interfaces for both p- and n-FETs. This is clearly evident in the I_D-V_D curves (Figure 3), where a nonlinearity is observed at the low V_D regime, indicative of the nonohmic contacts. The total resistance of a device is given as $R_{tot} = 2R_c + R_{ch}$, where R_c is the resistance of each contact and R_{ch} is the channel resistance, which depends on the channel mobility and the charge density at a given gate voltage. In our devices, the total resistance in the ON-state, especially at high V_G where the channel charge density is large, is dominated by R_c. That is, at high V_G-V_T, $R_{tot} \approx 2R_c$. In such a case, the mobility of the device cannot be correctly extracted from the experimental $I-V$ curves. Instead, a more proper figure of merit for these Schottky devices is R_c. We have extracted the R_c of our p- and n-FETs as a function of K doping time by calculating the resistance at $V_G = |3$ V| from the transfer curves (Figure 2d). The p-FET transfer characteristics remain unchanged with doping since the channel is protected with a gate that overlaps metal contacts. The extracted R_c for the p-FET is ~1 Mohm-μm, independent of K doping. On the other hand, the R_c of the n-FET is drastically reduced from ~0.5 Gohm-μm to ~5 Mohm-μm after 5 min of K doping. At this doping level, the contact resistances of both p- and n-FETs are on the same order of magnitude, which makes the design of a CMOS circuit feasible.

Figure 3 shows the output characteristics of the same p- and n-FETs discussed above. The current densities for the two polarities are on the same order of magnitude, with that of the n-FET being ~2× higher for the same gate voltage drive. As discussed earlier, the ON currents for our devices are limited by the contact resistances. In fact, the I_D-V_{DS} curves depict a small nonlinearity in the low-voltage regime for both

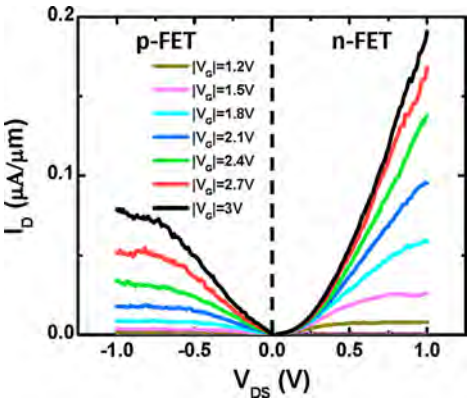

Figure 3. Output characteristics of p- (on the left) and n-FETs (on the right) fabricated on the same WSe_2 flake.

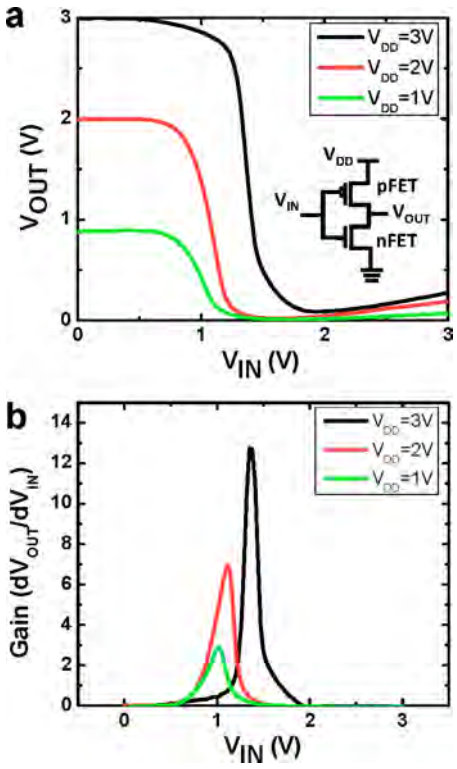

Figure 4. (a) Voltage transfer characteristics of a WSe_2 CMOS inverter at different supply voltages. (b) Direct current voltage gain of the inverter at different V_{DD}.

devices, which is indicative of Schottky contacts. The K doping time for the n-FET, which corresponds to the electron doping concentration, was chosen such that the two devices would have similar current values, needed for the design of CMOS logic gates. In the future, the p-contacts ideally need to be doped as well with a complementary surface dopant to reduce the contact resistance of the p-FET. To date, the most successful p-doing of WSe_2 has been achieved through surface charge transfer doping with NO_2. However, neither NO_2 nor K are stable dopants, thereby making it difficult at this stage to perform complementary doping. Future development of stable dopants for TMDCs

is required, which can further enhance the performance of CMOS devices.

Next, we focus on configuring the complementary n- and p-FETs into CMOS logic circuits. As a proof of concept, an inverter gate (*i.e.*, NOT logic gate) is demonstrated using one n- and one p-FET connected in series. In a conventional manner, the n-FET is grounded and the supply voltage V_{DD} is applied to the p-FET. Both p- and n-FETs are controlled by the same top gate electrode that serves as the input voltage (V_{IN}) electrode. Output voltage (V_{OUT}) is measured using the common source electrode of the p-FET and n-FET. If a small input voltage is applied, the n-FET is OFF and p-FET is ON; therefore V_{OUT} is connected to V_{DD}. In other words, V_{OUT} is pulled up to logic 1. On the contrary, at high input voltages, the n-FET is ON and the p-FET is OFF; therefore V_{OUT} is connected to ground (0 V). In other words, V_{OUT} is pulled down to logic 0. The circuit schematic of a CMOS inverter is shown in the inset of Figure 4a, with the false color SEM image of the fabricated device shown in Figure 1a. The transfer characteristics (V_{OUT} *versus* V_{IN}) of the CMOS inverter as a function of V_{DD} are shown in Figure 4a. Clear signal inversion is observed with high V_{OUT} and low V_{IN} and *vice versa*. The peak dc voltage gain of the CMOS inverter, $|\partial V_{OUT}/\partial V_{IN}|$, is measured to be >12 at a supply voltage V_{DD} of 3 V (Figure 4b). The gain of the inverter is high despite the nonoptimal transistor currents. Noise margins are evaluated by extracting the maximum low input voltage V_{IL}, minimum high input voltage V_{IH}, minimum high output voltage V_{OH}, and maximum low output voltage V_{OL}. V_{IL} and V_{IH} are the input voltages at which the slope of the voltage transfer curve in Figure 4a is -1 (unity gain), whereas V_{OH} and V_{OL} are the corresponding output voltages, respectively. The high- and low-state noise margins (NM_H and NM_L, respectively) are then calculated by using the expressions $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$. The noise margins are found to be $NM_H = 0.35V_{DD}$ and $NM_L = 0.32V_{DD}$ for $V_{DD} = 3$ V.

CONCLUSION

In conclusion, a CMOS inverter on the same TMDC flake, WSe_2, is realized for the first time. The operation of the p-FET is realized by high-workfunction Pt contacts and overlapped top-gate device structure, whereas the n-FET is enabled by potassium doping of the contact regions using an underlapped top-gate structure as a self-aligned mask. The results depict that through proper contact engineering, both transistor polarities can be obtained using the same TMDC on a single substrate. Moving forward, further optimization of the contacts and especially developing air-stable electron and hole dopants are needed to explore the performance limits of TMDC CMOS circuits.

METHODS AND EXPERIMENTAL SECTION

The fabrication process of WSe_2 CMOS devices is as follows. WSe_2 flakes were deposited on Si/SiO_2 (thickness, 260 nm) substrates using a micromechanical exfoliation technique. The transferred flakes were mapped in terms of location, dimensions, and thickness using an optical microscope. Three electron-beam (e-beam) lithography steps were performed in order to define the p- and n-contacts as well as the top-gate stack. Specifically, a Pt/Au/Pd (10/30/20 nm) metal stack was deposited by e-beam evaporation for the p-side source−drain (S/D) contacts followed by lift-off in acetone. Subsequently, the devices were annealed in O_2 ambient at 250 °C for 1 h to further improve the contact resistance. This metal stack was chosen for the p-FETs due to the high work function of the Pt bottom layer, which provides a low Schottky barrier height for hole injection into the valence band of WSe_2. As a result, WSe_2 p-FETs are realized as shown here. Au (60 nm) contacts were then formed for the n-side S/D electrodes by e-beam evaporation and lift-off in acetone. The gate stacks are formed by e-beam lithography, atomic layer deposition (ALD) of ZrO_2 (thickness, ∼20 nm) at 120 °C, evaporation of Ni/Au electrodes (30/30 nm), and lift-off of the entire gate stack in acetone. Note that the low-temperature ALD used here allows for the use of the lift-off process for the entire gate stack using poly(methyl methacrylate) (PMMA) as the resist. Subsequently, potassium doping is performed in a vacuum at a pressure of 4×10^{-5} mbar by evaporating potassium from a commercially available dispenser filament (SAES Getters) by applying a 5 A dc current through it. The doping setup, which resembles a conventional thermal evaporator in terms of operation principles, is designed such that at a sample distance of ∼3 cm from the potassium dispenser the deposition of potassium is uniform over a 2 cm × 2 cm area, which is a typical chip size. The doping concentration is controlled through K evaporation time. Notably, the devices are electrically measured *in situ* during the K evaporation process, and once a desired doping level is reached, as confirmed from the electrical measurements, the current flow to the dispenser is stopped.

Conflict of Interest: The authors declare no competing financial interest.

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