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Room-Temperature Negative Capacitance in a Ferroelectric–Dielectric Superlattice Heterostructure

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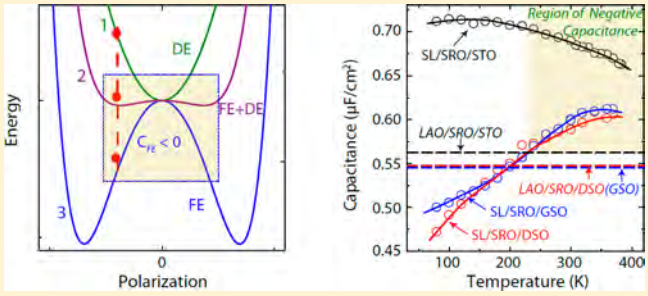
Supporting Information

ABSTRACT: We demonstrate room-temperature negative capacitance in a ferroelectric–dielectric superlattice heterostructure. In epitaxially grown superlattice of ferroelectric BSTO ($Ba_{0.8}Sr_{0.2}TiO_3$) and dielectric LAO ($LaAlO_3$), capacitance was found to be larger compared to the constituent LAO (dielectric) capacitance. This enhancement of capacitance in a series combination of two capacitors indicates that the ferroelectric was stabilized in a state of negative capacitance. Negative capacitance was observed for superlattices grown on three different substrates ($SrTiO_3$ (001), $DyScO_3$ (110), and $GdScO_3$ (110)) covering a large range of substrate strain. This demonstrates the robustness of the effect as well as potential for controlling the negative capacitance effect using epitaxial strain. Room-temperature demonstration of negative capacitance is an important step toward lowering the subthreshold swing in a transistor below the intrinsic thermodynamic limit of 60 mV/decade and thereby improving energy efficiency.



KEYWORDS: *Room-temperature negative capacitance, ferroelectric, superlattice, epitaxial strain*

Traditionally a ferroelectric (FE) material is modeled using a double well energy landscape (Figure 1a, FE trace). In equilibrium, the ferroelectric resides in one of the wells providing a spontaneous polarization. The capacitance of the material is determined from $[d^2U/dQ^2]^{-1}$, which due to the positive curvature of U vs Q at the wells, is positive. On the other hand, around $Q = 0$, this curvature is negative. This means that it is possible to obtain a negative differential capacitance around $Q = 0$. Nevertheless, this state of negative capacitance is unstable; if a ferroelectric material is left at this state, it will eventually fall back to one of the wells where its capacitance is positive.

It is, however, in principle, to stabilize the state of negative capacitance. If a paraelectric or dielectric material is added to the ferroelectric material, the combined energy of the ferroelectric–dielectric (FE-DE) heterostructure could be such that it is minimized around $Q = 0$ (Figure 1a, FE + DE trace). In this case, the ferroelectric material is stabilized in a state where its own capacitance is negative.[1,2] It is important to note, however, that the overall capacitance of the composite structure is still positive but this capacitance is larger than the constituent dielectric capacitance.[1,2] This is completely opposite to the classical situation when a dielectric capacitor is added in series to another dielectric capacitor and the composite capacitance becomes lower than that of the constituent capacitors. Stabilization of negative capacitance in a ferroelectric material thus makes it possible to achieve a capacitance enhancement, otherwise impossible to obtain with traditional means. In doing so, it could reduce the subthreshold swing in a conventional transistor below the otherwise minimum limit of 60 mV/decade at room temperature.[1−4]

Because of the potential application for low power switching devices, the negative capacitance effect and its applicability in transistors have been studied significantly in the recent years.[1−11] Early work demonstrated <60 mV/decade subthreshold swing in a Si transistor using a polymer ferroelectric layer as the gate dielectric.[5,6] By using an internal electrode,[5,6] an S-like charge-voltage characteristic for the ferroelectric was also measured. In a two-terminal configuration, capacitance enhancement was demonstrated in an epitaxially grown single

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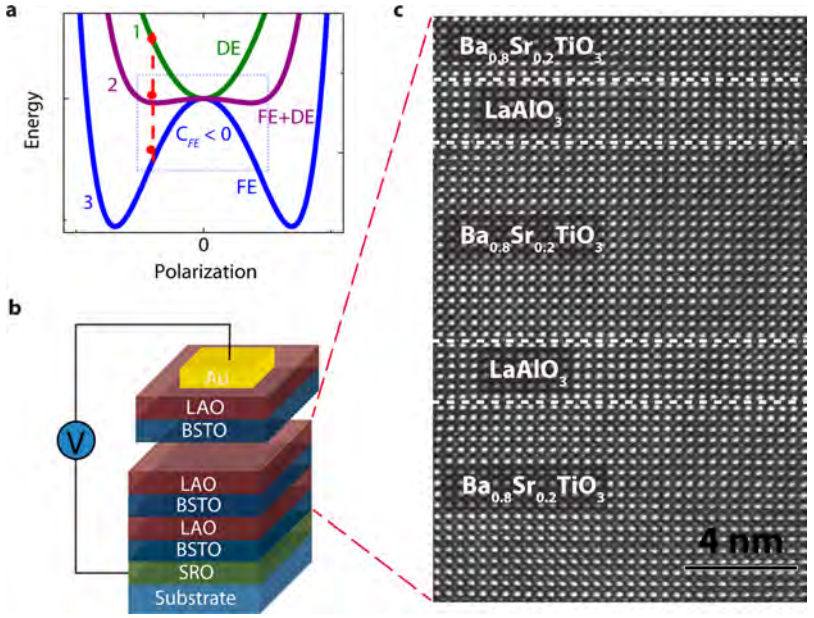

Figure 1. Energy landscapes, schematic diagram, and TEM of FE-DE superlattice stack. (a) Energy landscapes of FE, DE, and their series combination. The negative capacitance region of FE energy landscape is shown inside the dotted rectangular box. The unstable FE negative capacitance state is stabilized by putting a DE capacitor in series with it. (b) Schematic diagram of a FE-DE superlattice stack and the measurement configuration. The artificial superlattice of LAO/BSTO is grown on the SRO buffered substrates. An Au electrode is used for capacitance measurement. (c) STEM image of $LaAlO_3/Ba_{0.8}Sr_{0.2}TiO_3$ superlattice stack grown on the $SrRuO_3$(10 nm)/$SrTiO_3$(001) substrate.

crystalline bilayer consisting of strontium titanate (STO, $SrTiO_3$) as the dielectric and lead zirconate titatnate ($Pb_xZr_{1-x}TiO_3$) as the ferroelectric.[7] However, the negative capacitance was only achieved above 573 K due to the compressive strain from the STO substrate that increases the Curie temperature of PZT. More recently,[11] capacitance enhancement and thereby negative capacitance has been demonstrated at room temperature by using an epitaxially grown single crystalline bilayer of STO and barium titatnate (BTO, $BaTiO_3$). While the ultimate objective is to achieve the negative capacitance effect in a transistor, the capacitance enhancement studies in a two-terminal configuration provides a simple way to study the effect itself and thereby gain insight into the material optimization that will be needed to obtain the effect controllably. From that point of view, room-temperature demonstration of negative capacitance is of significant importance. Here, we demonstrate stabilization of negative capacitance leading to capacitance enhancement at room temperature in a $LaAlO_3/Ba_{0.8}Sr_{0.2}TiO_3$ (LAO/BSTO) superlattice heterostructure.

The material combination chosen for the superlattice is guided by the following considerations: (i) $Ba_xSr_{1-x}TiO_3$ is a ferroelectric where by changing the mole fraction of Ba and Sr, the Curie temperature (T_c) can be controlled over a significant range; in principle from very low temperatures to the Curie temperature of $BaTiO_3$ that is ~110 °C. This is much smaller than PZT where the T_c is ~430 °C in the bulk. Note that in the thin film form, the Curie temperature may vary to some extent. In particular, for compressive strain from the substrate it may go up by some amount.[12] We believe that this is why in our previous work[7] the negative capacitance effect was only seen at elevated temperatures. From that point of view, low and controllable Curie temperature in the BSTO provides an excellent material for potential room-temperature operation. Even if the compressive strain enhances the Curie temperature over the bulk value, it should still be much lower than what happens to PZT thin films and should remain reasonably close to room temperature. For all our work reported here, we have used $x = 0.8$ for which a $T_c \sim 292$ K has previously been measured.[13] (ii) The dielectric LAO is chosen first because its permittivity remains reasonably constant over a large range of thicknesses. For STO, which has been used as a dielectric in previous studies,[7,11] change in the permittivity as a function of thickness adds a significant uncertainty. STO is also an incipient ferroelectric. Indeed it has been shown that strain can make STO a ferroelectric at the room temperature.[14] Thus, use of LAO makes the ferroelectric−dielectric combination much simpler to analyze. For experimental study, superlattice samples of $[(LAO)_6/(BSTO)_{18}]_{11}$ were grown by Laser-MBE on the STO(001), DSO($DyScO_3$)(110,) and GSO($GdScO_3$)(110) substrates using a ~10 nm SRO buffer layer. High-resolution cross-sectional scanning transmission electron microscopy (STEM) image of representative BSTO/LAO superlattice samples is shown in Figure 1c. The contrast of structural and chemical interface between LAO and BSTO is not obvious because of closeness in the atomic mass between Ba (56) and La (57). However, LAO and BSTO sublayers can be distinguished by strain distribution which is shown in Supporting Information Figure S1.

The crystal structure and unit cell lattice parameters have been quantitatively studied by high-resolution X-ray diffraction, including θ–2θ spectrum and reciprocal space maps (RSMs). Figure 2a show the RSMs around the pseudocubic (103) reflection of superlattice grown on SRO-buffered STO (left), DSO (middle), and GSO (right) substrates, respectively. Consistent with the STEM analyses, the RSMs show that the superlattice is epitaxial and presents an in-plane lattice parameter very close to the substrate. In order to get a better insight, the (00L) truncation rod was investigated in more detail for the three strain scenarios following ref 15. The spectra collected are shown in Figure 2b (light trace). The data do not display the characteristic sharp and symmetric arrangement of

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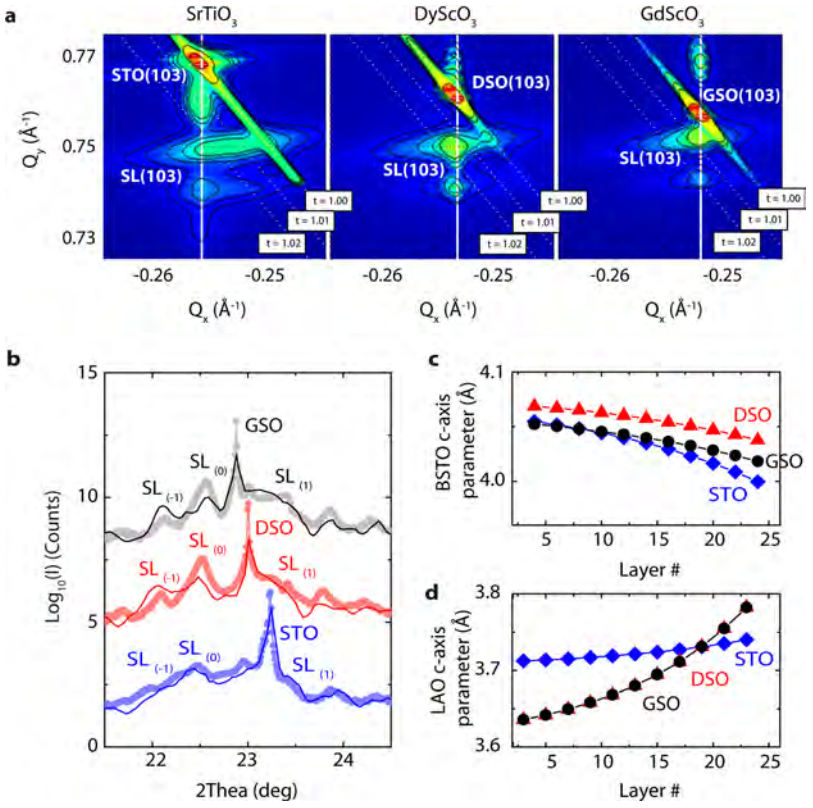

Figure 2. X-ray diffraction of superlattice grown on the SRO-buffered substrates. (a) Reciprocal space maps and diffraction patterns for the heterostructures mapping the diffracted intensity around the STO (left), DSO (middle), and GSO (right) pseudo cubic (103) reflections. The most intense peak corresponds to the substrate. In all cases, a substantial amount of the diffracted photons present the same in-plane momentum transfer thus indicating that the heterostructure mostly preserves the in-plane lattice parameter of the substrate. The remaining intensity corresponds to the BSTO/LAO superlattice. Also plotted in panel a are the constant tetragonality (t) lines corresponding to t = 1, 1.01, and 1.02. We observe that as the substrate is changed from STO to DSO and then to GSO, the SL peaks move closer to a smaller tetragonality line. (b–d) Fitting of the crystal truncation rods around the (00L) reflection for investigating each sublayer lattice parameters. The measured X-ray intensity (light) and the fit (strong) are shown for the three strain scenarios. Broadening of the calculated diffracted intensity traces is obtained by randomly varying the nominal thickness of each sublayer by as much as one unit cell and adding the resultant waves incoherently. The asymmetry is introduced by strain gradients across the heterostructure. The layer (LAO or BSTO) closest to SRO is referred to as Layer 1 in panels c and d.

an ideal superlattice. Instead two features are immediately noticed: the substantial broadening of the peaks and the asymmetry in the intensity corresponding to the multilayer stack. We addressed these two issues quantitatively by fitting (strong trace) the spectra under the assumption that the effective thickness of each BSTO and LAO sublayer randomly oscillates across the 11 nominal repetitions with amplitude of, at most, one unit cell. Up to 100 different ideal diffraction curves were generated using the same seed for the three substrates and were added incoherently.[16] In order to capture the asymmetry of the scattered intensity, exponential strain gradients were introduced and were identical for all 100 different ideal traces generated. An optimization algorithm renders the best match that correspond to the gradients shown in Figure 2c,d for BSTO (top) and LAO (bottom), respectively. On STO, the LAO layer can best sustain the stress while BSTO is rapidly relaxed toward the bulk value. In contrast, on DSO and GSO the LAO layer shows an abrupt relaxation from the out-of-plane values corresponding to unit cell volume conservation toward the fully relaxed value while the BSTO sublayers show a less pronounced relaxation.

Capacitor structures were fabricated by patterning a top Au electrode on the superlattices. Figure 3a,b shows the capacitance and admittance angle as functions of voltage and frequency for a superlattice where LAO(6 ML)/BSTO(18 ML) repeated 11 times were grown on the SRO(10 nm) buffered STO substrate at room temperature. Also plotted here is the capacitance of an LAO capacitor with a thickness of 66 (6 × 11) monolayers. The capacitance of superlattice is found to be larger than the constituent LAO capacitance over the entire voltage and frequency range. It means that the ferroelectric BSTO layer contributes an effective negative capacitance to the superlattice heterostructure. For clarification, throughout this letter, by using the term "constituent LAO capacitance" we mean the capacitance of an isolated LAO capacitor whose total thickness is the same as the sum of thicknesses of only the LAO layers in the superlattice keeping the same cross sectional area. Figure 3c–e show results for average capacitance values of the superlattices from different samples on three different substrates. For plotting this data, we used the value of the capacitance for which the two branches of the C–V hysteresis cross each other (therefore, not the highest value of the C–V characteristic). Each data point reflects averages taken over many devices coming from three different samples for each substrate type. The scatter in the values obtained is also shown in the data. It is observed that over multiple samples and devices and over three different substrates, the superlattice capacitance is larger than the constituent LAO capacitance. This demonstrates the robustness of the observed effect. Note that the LAO capacitance is slightly different on different

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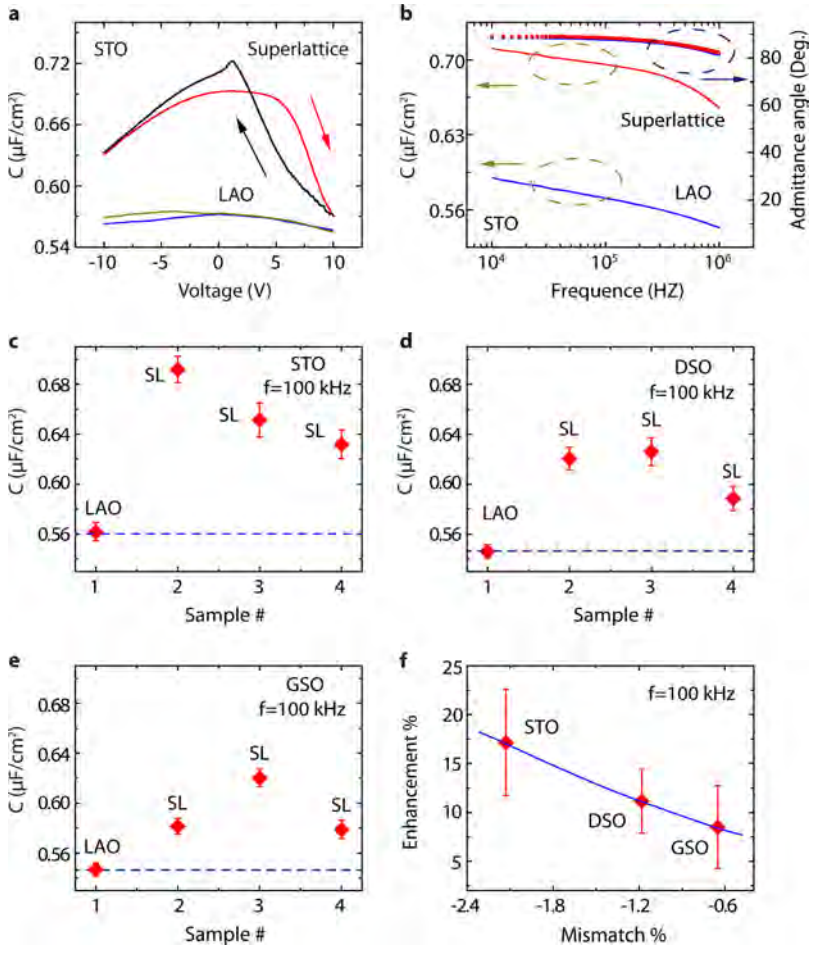

Figure 3. Room-temperature ferroelectric negative capacitance in FE–DE superlattice heterostructure. (a,b) Voltage (a) and frequency (b) dependence on the capacitance of the superlattice grown on the STO and constituent LAO on STO at room temperature. Capacitance enhancement is observed at room temperature for both branches. (c–e) Capacitance of the superlattice in comparison to constituent LAO capacitance for different samples grown on STO (c), DSO (d), and GSO (e), respectively. The plotted values correspond to the point where the two branches of the hysteresis in the $C-V$ sweep cross each other. (f) Capacitance enhancement as a function of substrate strain.

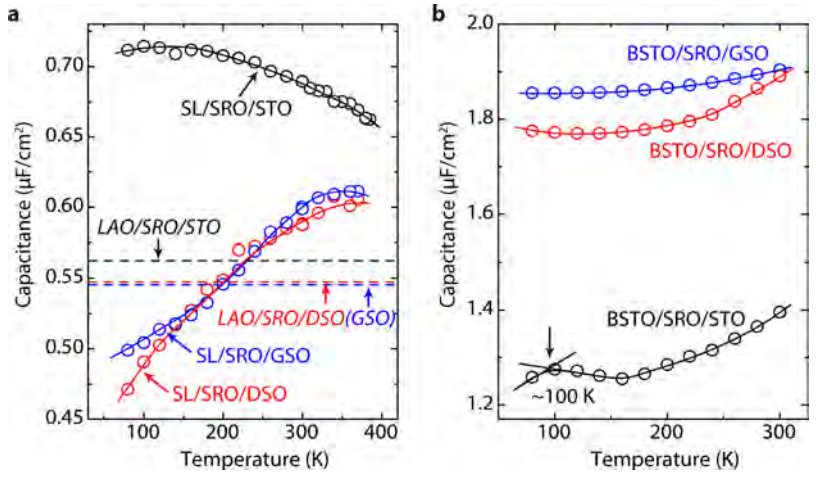

Figure 4. Temperature dependence of the superlattice capacitance. (a) Superlattice capacitance as a function of temperature grown on STO, DSO, and GSO substrates. For comparison, room-temperature capacitance of constituent LAO is also shown. (b) Temperature dependence of BSTO capacitance grown on the same substrates showing that T_c is above the room temperature.

substrates. This variation can be seen in Figure 3c–e. Finally, Figure 3f shows the average extent of enhancement in capacitance as a function of substrate strain. The values have been averaged over multiple samples and devices as shown in Figure 3c–e. It is observed that the largest compressive strain (on STO) provides the largest enhancement. Comparing with the X-ray diffraction analysis as discussed previously (see Figure 2), one observes that the largest enhancement is found when

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the strain on BSTO has relaxed rapidly to its bulk value. Notably, strain relaxation can lead to dislocations, which in turn can increase permittivity.[7] However, in this case the strain relaxation in BSTO alone cannot be responsible for the capacitance enhancement. This is because even if the permittivity of BSTO increased due to dislocations, the overall capacitance of the series combination should still be lower than the LAO capacitance, without the BSTO being in a state of negative capacitance.

Next we explored how the superlattice capacitance varies as a function of temperature. Figure 4a shows the capacitance of the superlattices on different substrates. For comparison, room-temperature value of LAO capacitance on these substrates is also plotted. It is observed that the capacitance of the superlattice on STO goes up for decreasing temperature while the capacitance for the other two substrates goes down. For comparison, the capacitance of BSTO of the same thickness as the superlattice grown on the same three substrates is shown as a function of temperature in Figure 4b. Note the peak around 100 K for the BSTO grown on the STO substrate. This is associated with orthorhombic-to-tetragonal phase transition.[17] This peak is not clearly visible for BSTO grown on DSO and GSO substrates. Notably, the permittivity of thin ferroelectric films often show a very diffused dependence on temperature,[18] making it difficult to pinpoint the Curie temperature from such measurement. In the superlattice samples as well, the overall variation of capacitance over a large range of temperature is very small. This is also a signature of strain gradient present in the superlattices as discussed before, which leads to a diffused T_c. Nonetheless, the opposing trends of superlattice capacitance increasing for STO substrate and decreasing for DSO and GSO substrates, starting from low temperature to room temperature, is very clear.

To qualitatively understand the temperature dependence of the capacitance, we note that the potential energy density of the FE-DE heterostructure can be written as

$$U = \alpha_0(T - T_c)P^2 + \beta P^4 + \frac{P^2}{2C_{DE}} \quad (1)$$

where α_0 and β are material parameters for the FE,[19] T_c is the Curie temperature of the ferroelectric material, C_{DE} is the capacitance of the dielectric layer, and we have assumed polarization $P \sim Q$. It is possible to combine the coefficients of P^2 to write

$$U = \alpha_0(T - T_c')P^2 + \beta P^4 \quad \text{where}$$
$$T_c' = T_c - \frac{1}{(2\alpha_0 C_{DE})} \quad (2)$$

Equation 2 shows that the FE−DE combination can be mathematically thought of as a single FE with a reduced T_c. This reasoning shows that for an appropriately chosen FE (and therefore T_c), and dielectric (C_{DE}), it is possible, in principle, to obtain $T_c' = T$ and therefore achieve an extremely large enhancement of capacitance ($[d^2U/dQ^2]^{-1}$) around $Q \sim P = 0$. In practice, however, the polarization switching is affected by the ability to nucleate domains, inhomogeneous strain present in the film, substrate clamping, and so forth. As a result, it is not possible to quantitatively predict the exact amount of downward shift in the T_c for a FE−DE configuration from eq 2. However, qualitatively the results should still be valid and therefore we can use it to gain insight into the observed temperature dependence. The increasing capacitance of BSTO grown on all three substrates shown in Figure 4b indicates that the T_c of BSTO is above the room temperature. In comparison, the decreasing capacitance of the superlattice grown on STO indicates that the effective reduction in T_c is large enough that T_c' goes below the room temperature. In addition, the increasing trend of the superlattice capacitances grown on DSO and GSO show that the effective reduction in T_c is much smaller for those samples. As described above, it is difficult to know the exact reason for the differences in the reduction of T_c. However, comparison with the XRD data shows that BSTO goes through rapid strain relaxation in the superlattice grown on STO. This superlattice also shows the largest downward shift of T_c'. Two different reasons could be responsible for this observation. First, due to strain relaxation the starting point T_c for BSTO on STO can be smaller than the BSTO on the other two substrates. Second, it is possible that the depolarization field from the dielectric layer[7,20] and therefore the downward shift is more effective on a strain relaxed and therefore more polarizable ferroelectric material. It is likely that both factors contribute to the observed behavior and an exact understanding will require more detailed studies from both structural and modeling view points especially on the effect of strain on the formation of domains and polarization switching in these superlattices. Nonetheless, the results show that substrate strain may be used to control negative capacitance in such heterostructures.

In summary, we have demonstrated stabilization of negative capacitance at room temperature using a LAO/BSTO superlattice. An enhancement of capacitance is observed in the superlattice in comparison to constituent LAO capacitance over a large range of substrate strain. As the ability to integrate epitaxial ferroelectrics on conventional semiconductors advances,[21] these results could be useful for optimizing material stack for negative capacitance transistors. Before concluding, it is also important to note that the concept of negative capacitance goes beyond ferroelectric materials and can be applied in general to a two state system separated by an intrinsic barrier (stored energy).[22−27] By adding a series positive capacitance, it might be possible to stabilize the state of negative capacitance in these alternate systems as well, leading to completely new applications.

■ ASSOCIATED CONTENT

Supporting Information

Details of deposition of the superlattice stacks, structural characterization, temperature-dependent measurement and details of models used are presented. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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