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Effects of substrate leakage and drain-side thermal barriers in In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.5}$Sb$_{0.5}$ quantum-well tunneling field-effect transistors

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The device leakage current and the ON-state characteristics of In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.5}$Sb$_{0.5}$ quantum-well tunneling field-effect transistors (QWTFETs) are examined on the basis of temperature-dependent measurements. Different from commonly observed Shockley–Reed–Hall (SRH) recombination in the OFF-state, substrate leakage is identified as the source of OFF-current, which limits the steepness of the device transfer characteristics. In addition, analysis of the TFET operation in the linear regime reveals a current barrier due to an ungated region near the drain, which accounts for the unexpected parasitic resistance and current saturation at low temperatures. This barrier can be eliminated by reducing the gate-to-drain distance, as illustrated by device simulations. The applied methodology provides a design guideline for the gate-to-drain alignment tolerance in TFETs. © 2014 The Japan Society of Applied Physics

Recently, power supply voltage (V_{DD}) scaling of complementary-metal–oxide–semiconductor (CMOS) technology has become limited by the 60 mV/decade subthreshold swing at room temperature.[1,2] Tunneling field-effect transistors (TFETs) are attractive because of their potential to achieve a steep subthreshold swing (SS) by harnessing the sharp switching process of band-to-band tunneling. TFETs fabricated with various structures and material systems (Si, Ge, III–Vs) have demonstrated sub-60 mV/decade SS at room temperature[3–6] and low drive currents owing to limited tunneling efficiency. The ON-current of TFETs has been tremendously improved by band gap engineering of type-II (staggered gap) heterostructures.[7] In addition, *line TFETs*, with the gate electric field aligned to the tunneling direction, enable stronger gate modulation over the entire tunneling junction and improved ON-current compared with conventional lateral TFET designs.[8–12] Alternatively, density-of-states switching in TFETs with two quantum wells (QWs) has also been proposed to obtain a steep SS over a much wider range of drive currents.[13] Understanding the underlying physics of TFET operation is the key to further improvement. Temperature-dependent measurement and simulation studies on TFETs have provided useful information on TFET design.[4,10,14–17] Unfortunately, performance is often degraded due to series resistance.[11,18–20] Nevertheless, few hypotheses and suggestions for improvement have been made without further analysis. Series resistance arising from the gate underlapping the source/drain (in lateral TFETs) or drain extension region (in line TFETs) is a concern because of process variations in all TFET structures. Furthermore, owing to the penetration of the electric field from the drain, which induces additional band bending and V_{DS} dependence of the transfer characteristics, it is sometimes desirable to move the drain away from the gated area.[16] Devices suffering from either series resistance or excessive drain modulation exhibit linear output characteristics without saturation. Physical analysis of the origin of the series resistance and quantitative characterization are imperative to provide design guidelines for high-performance TFETs.

We previously demonstrated the fabrication and preliminary room-temperature results of quantum-well TFETs (QWTFETs) based on ultrathin In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.5}$Sb$_{0.5}$ heterostructures.[21] In this work, we perform a temperature-dependent study (from 150 to 300 K) on In$_{0.53}$Ga$_{0.47}$As/

GaAs$_{0.5}$Sb$_{0.5}$ QWTFETs in order to understand the limitations of the device design and to guide structure optimization. The temperature dependence of the ON-current, OFF-current, and SS provide information on the bottleneck of device operation and the limiting factors for the steepness at room temperature. A physical analysis scheme of the devices' ON-state linear regime behavior is proposed to further explore design solutions, and an improved structure is suggested on the basis of simulation results.

A cross-sectional view of the In$_{0.53}$Ga$_{0.47}$As/GaAs$_{0.5}$Sb$_{0.5}$ QWTFET structure is illustrated in Fig. 1(a), where a self-aligned air-bridge structure is used to prevent direct source-to-drain tunneling from the GaAsSb layer to the InGaAs layer. A raised drain with heavily doped In$_{0.53}$Ga$_{0.47}$As is used with a Mo contact. The designed distance between the gate and S/D contacts is $L_{GS} = L_{GD} = 1 \, \mu m$. The epitaxial structure with the layer thicknesses and doping is shown in Fig. 1(b). Details of the fabrication process can be found in Ref. 21.

Figures 2(a) and 2(b) respectively plot the transfer and output characteristics of the TFET with gate dimensions of $L_g = 3.8 \, \mu m$, $W_g = 22 \, \mu m$ at room temperature. The transfer characteristics show a minimum SS of 140 mV/decade at $V_{DS} = 0.05 \, V$. This non-ideal SS is mainly due to 1) the high interface trap density at the high-k/III–V interface; 2) the high leakage through the 30 nm InP buffer layer, which is greatly reduced at a lower temperature, as shown in the following section. The output characteristics exhibit negative-differential-resistance (NDR) behavior at a forward bias (negative V_{DS}), which is solid evidence of tunneling behavior.

In order to gain insights into the physics and limitations of the device structure, a temperature-dependent study was carried out from 300 to 150 K. Figure 3(a) shows the I_{DS}–V_{GS} curves from 150 to 300 K at $V_{DS} = 0.05 \, V$. The SS versus I_{DS} is plotted in Fig. 3(b) at various temperatures, showing a significantly improved SS_{min} of 58 mV/decade and SS_{eff} of 80 mV/decade (I_{DS} from 10 pA to 10 nA) at 150 K. One limiting factor for achieving a steep subthreshold is the high-k/InGaAs interface traps (D_{it}). The split-C–V characteristics of on-chip MOSFET-like test structures have been shown in our previous work,[21] and D_{it} on the order of $10^{13} \, cm^{-2} \, eV^{-1}$ near the conduction band results in a severely degraded SS. Given the typical HfO$_2$/InGaAs D_{it} of ~ 2–3×10^{13} cm^{-2} eV^{-1} at the conduction band edge,[22] the first-order calculation of the intrinsic SS at 300 K should be close to
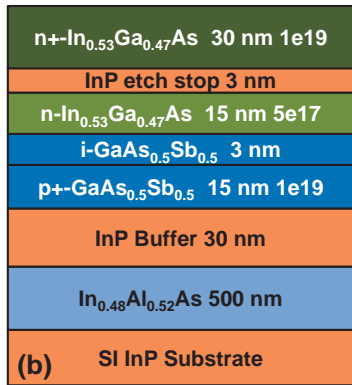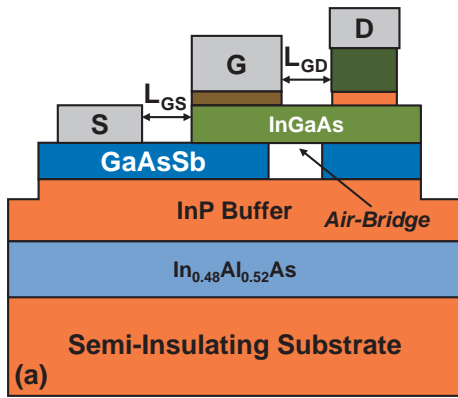
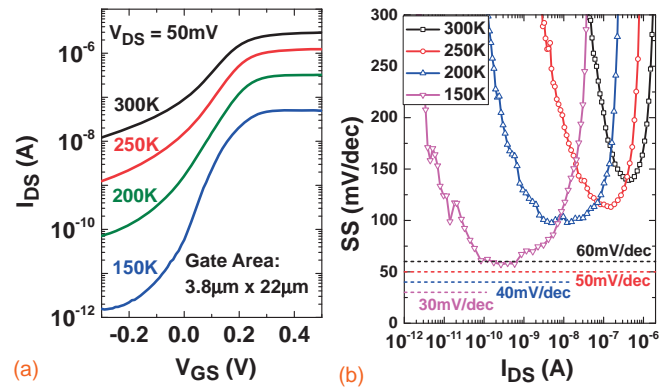**Fig. 1.** (a) Schematic cross-sectional view of the $In_{0.53}Ga_{0.47}As/$GaAs$_{0.5}$Sb$_{0.5}$ QWTFET. (b) Epitaxial structure with layer thicknesses and doping for the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ QWTFET fabrication.
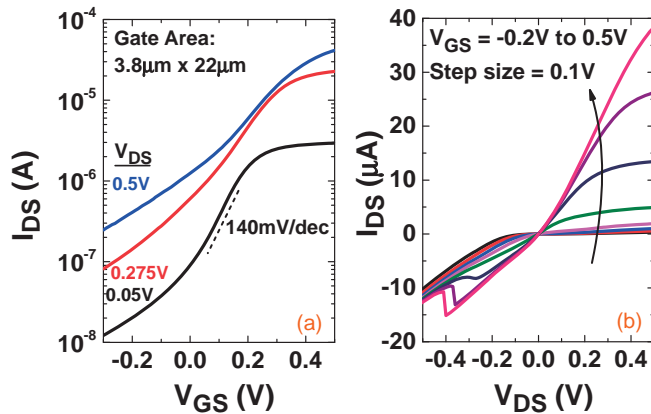

Fig. 2. (a) Transfer and (b) output characteristics of the fabricated TFET with gate dimensions of $3.8 \times 22\,\mu m^2$ at room temperature.

Fig. 3. (a) I_{DS}–V_{GS} curves of the TFET from 150 to 300 K at low V_{DS}. The OFF-state leakage current is markedly decreased at 150 K. (b) SS versus drive current from 150 to 300 K. $SS \sim 60\,mV/decade$ over more than one decade of I_{DS}, and $SS_{eff} = 80\,mV/decade$ is achieved at 150 K.
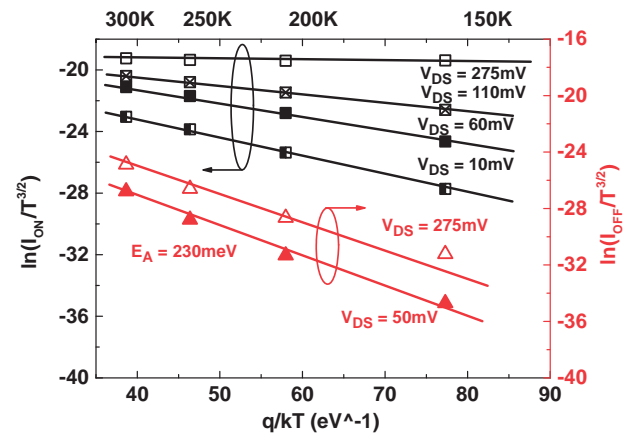
Fig. 4. ON-current ($V_{GS} = 0.5\,V$) and OFF-current ($V_{GS} = -0.3\,V$) at various V_{DS} values versus inverse thermal energy. The linear relationship in the semi-log scale implies an energy barrier in the current path, and the slopes are related to the barrier height.

$SS_{in} = SS_{ex}/(1 + qD_{it}/C_g) \sim 48\,mV/decade$ with a CET of 2.0 nm. Although interface traps tend to be frozen out at low temperatures, those in the conduction band, where TFETs are operated, are not. Consequently, the SS at 150 K is still not close to the thermal limit of 30 mV/dec. The OFF-current is another major factor limiting the SS. When the temperature decreases to 150 K, the leakage current in the OFF-region decreases substantially (I_{off} decreases by a factor of 10^4), exhibiting a slightly improved SS compared with the thermal limit. Therefore, the OFF-state leakage must be reduced in order to realize a steeper SS. The large OFF-current may originate from leakage through the 30-nm-thick unintention-

ally doped InP buffer layer and may be eliminated by either undercutting the InP layer under the drain (floating drain) or using a heterostructure-on-insulator (HOI) substrate.

It can be observed from Fig. 3(a) that the ON-current of the device for a low drain bias (linear regime) degrades as the temperature decreases. There are two probable reasons for this: 1) an increase in the height of the tunneling barrier and 2) decreased thermionic emission over a parasitic barrier in the current path. In order to analyze the underlying physics, the ON-current at $V_{GS} = 0.5\,V$ was extracted at different drain biases, and the Arrhenius plot [$\ln(I_{ON}/T^{3/2})$ vs $1/kT$] is shown in Fig. 4, where $T^{3/2}$ accounts for band gap widening at lower temperatures. It is seen from the plot that the ON- and OFF-currents show thermal behavior at lower drain biases as $\ln(I_{ON}/T^{3/2})$ is linear versus $1/kT$. The slope of the OFF-current is due to the thermal process of carrier injection into the InP buffer. Different from the Shockley–Reed–Hall (SRH) recombination observed in a previous study,[14] which has a slope equal to half of the effective band gap at the tunneling interface, the 230 meV OFF-current slope in the Arrhenius plot is closer to the conduction band offset at the GaAsSb/InP heterointerface than ~ 145 meV, half of the effective band gap calculated with a self-consistent Poisson-
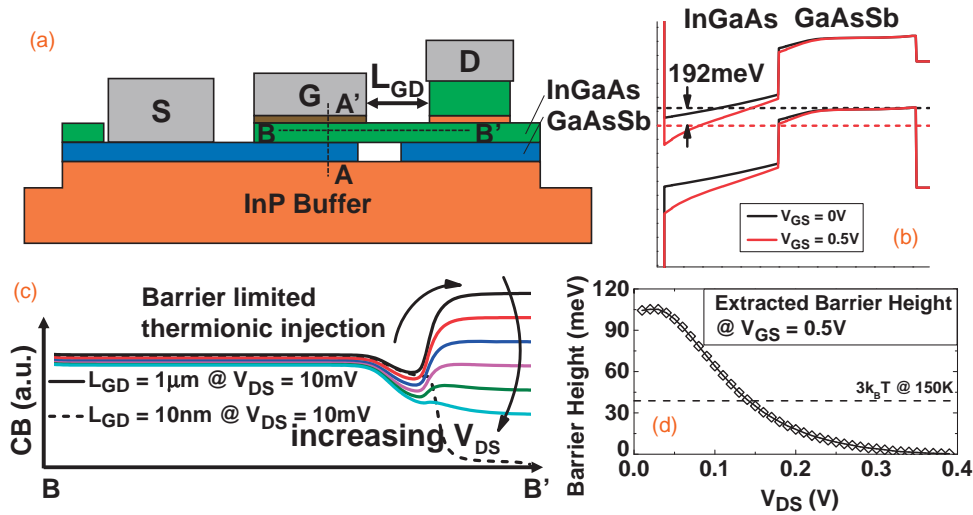
Fig. 5. Physical model for the InGaAs/GaAsSb vertical TFET in the ON-state. (a) Simplified schematic view. (b) Simulated band diagram along the tunneling direction (A–A′). The application of $V_{GS} = 0.5$ V changes the InGaAs first subband energy by 192 meV (neglecting D_{it}). (c) InGaAs conduction band diagram parallel to the gate (B–B′) simulated at $V_{GS} = 0.5$ V and various V_{DS} values. The barrier from the channel to the ungated InGaAs region dominates the drive current at a low V_{DS}. (d) Channel–drain barrier height extracted from the activation energies in Fig. 4.

Schrodinger simulator.[23] Since the unintentionally doped InP is n-type, the slope indicates the barrier that the electrons overcome when injected into the GaAsSb layer and eventually extracted by the drain. On the other hand, the linear variation of the ON-current with the bias implies a parasitic-bias-dependent barrier in the current path, with the slopes of the lines related to the barrier height.

On the basis of the above observation, self-consistent Poisson-Schrodinger calculations of the band diagram[23] and TCAD simulations[24] are performed to investigate and model the barrier in the current path. Figure 5 shows the simulation results of the current barrier located on the drain side of the ungated region. The band diagram normal to the gate plotted in Fig. 5(b) is calculated self-consistently under a quasi-equilibrium assumption. It can be seen that the gate voltage swing of 0.5 V introduces a modulation of approximately 192 meV to the first subband of InGaAs, where the majority of the electrons are located. However, owing to the presence of a large number of interface traps,[21] the actual modulation is smaller than 192 meV. At small V_{DS} and large V_{GS}, the conduction band in the gated region is below the drain conduction band, as illustrated in Fig. 5(c). The dimensions used in the simulation were extracted from cross-sectional transmission electron microscopy (TEM) images. It can be seen that a barrier is present in the ungated region near the drain for small V_{DS}, which restricts electron flow. When the drain bias increases, the barrier diminishes and finally disappears. The barrier height extracted from the slope of the Arrhenius dependence is plotted in Fig. 5(d) at different V_{DS} values. The output characteristics of the device at 150 K are plotted in Fig. 6, where the curves corresponding to $V_{GS} = 0.4$ and 0.5 V start to separate at $V_{DS} = 0.14$ V (circled point). The output characteristics are consistent with the extracted barrier height in Fig. 5(d), where the barrier height drops to $3k_BT$ at $V_{DS} = 0.14$ V. This suggests that for $V_{DS} < 0.14$ V, the current is limited by the thermionic barrier near the drain and for $V_{DS} > 0.14$ V, the current is limited by the tunneling across the heterojunction, hence the divergence
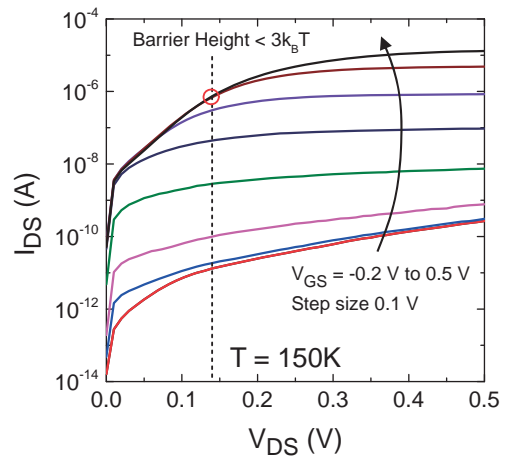
Fig. 6. Measured I_{DS}–V_{DS} curves for different V_{GS} values at 150 K. The output curves corresponding to $V_{GS} = 0.4$ and 0.5 V start to separate at $V_{DS} = 0.14$ V, where the barrier height becomes smaller than $3k_BT$.

of the two curves at different V_{GS} values. The fundamental problem in the device structure is that the ungated drain extension region is lightly doped; thus, a barrier forms in this region. In order to eliminate this barrier, the lightly doped region must be shortened. The simulation result with $L_{GD} = 10$ nm is shown in Fig. 5(c), where the electrons from the drain populate the lightly doped region, and the barrier is eliminated. In future work, L_{GD} can be reduced with a self-aligned gate-last process. On the other hand, although it is not seen in the simulation, the short-L_{GD} design may introduce drain-induced tunneling leakage (DITL), which exhibits strong V_{DS} dependence in the output characteristics without saturation. Additionally, simulation results for different values of L_{GD} suggest a relatively long L_{GD} to prevent significant drain bias dependence and ambipolar conduction behavior.[16] It should be clear that the value of L_{GD} involves a trade-off between electrostatics and transport. Thus, it is important to understand the origin and magnitude of the parasitic barrier

for low-V_{DD} TFET design. It is worth noting that L_{GD} of 40 nm is sufficient for suppressing the non-ideal effects shown in Ref. 16, and thus L_{GD} should be in the range of 40–100 nm. This is the probable origin of the series resistance in previously reported TFETs with long air-bridge designs,[11] although it was not previously characterized. Furthermore, this analysis technique is not only limited to line TFETs. The gate underlapping the source/drain junctions in lateral TFETs also results in a similar phenomenon: a thermal barrier forms in the ungated lightly doped channel region, limiting the tunneling carrier transport from the channel to the drain. With the methodology demonstrated, it is easy to interpret the unexpected series resistance or estimate the impact of such underlapping on device performance.

In summary, the temperature-dependent behavior of $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ QWTFETs is characterized and physical analysis is carried out for the ON-state behavior. The *SS* and ON/OFF ratio at 150 K are markedly improved owing to the suppression of the leakage current, which is shown to be through the InP substrate and can be remedied by including a floating drain or an HOI structure in future TFET designs. The Arrhenius plot of the device ON-current reveals a parasitic barrier within the carrier transport path, which significantly impacts the drive current. The output characteristics at 150 K corroborate the theory, and the barrier height can be extracted from the Arrhenius plot. Such analysis can provide a guideline for TFET designs with gate underlapping issues or TFET designs addressing the trade-off between series resistance and DITL.

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