Adhesive Force Characterization for MEM Logic Relays With Sub-Micron Contacting Regions

Jack Yaung, Louis Hutin, *Member, IEEE,* Jaeseok Jeon, *Member, IEEE,* and Tsu-Jae King Liu, *Fellow, IEEE*

***Abstract*—Contact adhesive force (F_a) scaling is critical for relay miniaturization, since the actuation area and/or actuation voltage must be sufficiently large to overcome the spring restoring force (F_k) in order to turn on the relay and F_k must be larger than F_a in order to turn off the relay. In this work, contact adhesive force is investigated in MEM logic relays with contact dimple regions as small as 100 nm in lateral dimension. The results indicate that van der Waals force is predominant. An adhesive force of 0.02 nN/nm^2 is extracted for tungsten-to-tungsten contact. F_a reduction should be possible with contact dimple size reduction and contact surface coating. [2013-0057]**

***Index Terms*—MEM relay, stiction, adhesive force, pull-in mode.**

I. Introduction

MICRO-ELECTRICAL-MECHANICAL (MEM) relays recently have attracted interest for digital logic applications [1] because they can provide for zero standby power and potentially can operate with lower active power than CMOS transistors [2]–[4]. In order for MEM relays to be a viable option for low-power computing, they must operate with low supply voltage (V_{DD}). Logic relays developed to date [5] operate with higher voltages than state-of-the-art CMOS transistors, however. Although the actuation voltage of a relay can be reduced by proportionately scaling down every one of its dimensions [6], contact adhesive force (F_a) ultimately will limit relay scaling. This is because the actuation area and/or actuation voltage must be sufficiently large to overcome the spring restoring force (F_k) of the suspension beams in order to turn on the relay, and F_k must be larger than F_a in order to turn off the relay. Therefore, F_a reduction is critical for relay size and voltage scaling.

Studies of adhesion between structures are usually performed using cantilever beam array (CBA) or double clamped beam (DCB) array. Using DCB with contact dimples, Laboriante *et al*. [7] showed that F_a is due to material-to-material bonding and that real contact is made only at a small number of asperities regardless of lithographically defined contact area, so that F_a does not scale with the apparent contact area - although in principle F_a can be reduced until the number of contacting asperities becomes one. Using CBA, DelRio *et al*. [8] showed that contact adhesion is due to van der Waals force between the contacting surfaces and has linear dependence on the apparent contact area, so that it can be reduced with scaling. These experimental findings indicate that differences in the geometry and topography of the apparent contact area can have dramatic impact on the nature of the contact adhesive force.

Conventional CBA approach uses optical interferometry to measure the cantilever beam shape; it is then fitted with Finite Element Matrix (FEM) Simulations to extract the adhesive force. The beam shape is a function of electrostatic attractive force (F_e), contact area and F_a. The previous two cannot be easily calculated since the beam cannot be modeled as a parallel plate and the contact area increases as F_e increase.

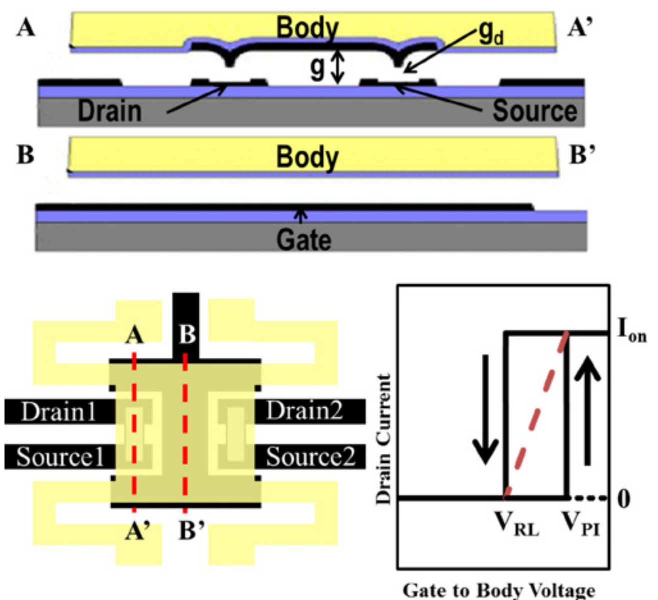

Fig. 1. Top: Schematic cross sections through the channel (A-A') and center (B-B') of a MEM logic relay. Bottom left: Plan-view illustration of the MEM logic relay. Bottom right: conceptual I_D-V_{GB} characteristic of a MEM logic relay. The dashed line indicates an effective sub-threshold slope due to the difference between the turn-on voltage (V_{PI}) and turn-off voltage (V_{RL}).

Manuscript received February 25, 2013; revised May 7, 2013; accepted June 3, 2013. Date of publication July 12, 2013; date of current version January 30, 2014. This work was supported in part by the NSF Center of Integrated Nanomechanical Systems (COINS) Grant EEC-0832819 and the NSF Center for Energy Efficient Electronics Science (E3S) Grant ECCS-0939514. Subject Editor H. Zappe.

J. Yaung, L. Hutin, and T.-J. King Liu are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: jack@eecs.berkeley.edu; lhutin@eecs.berkeley.edu; tsujae@berkeley.edu).

J. Jeon is with the Department of Electrical and Computer Engineering, Rutgers, The State University of New Jersey, Piscataway, NJ 08854 USA (e-mail: jaeseok.jeon@rutgers.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JMEMS.2013.2269995

1057-7157 © 2013 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.
See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

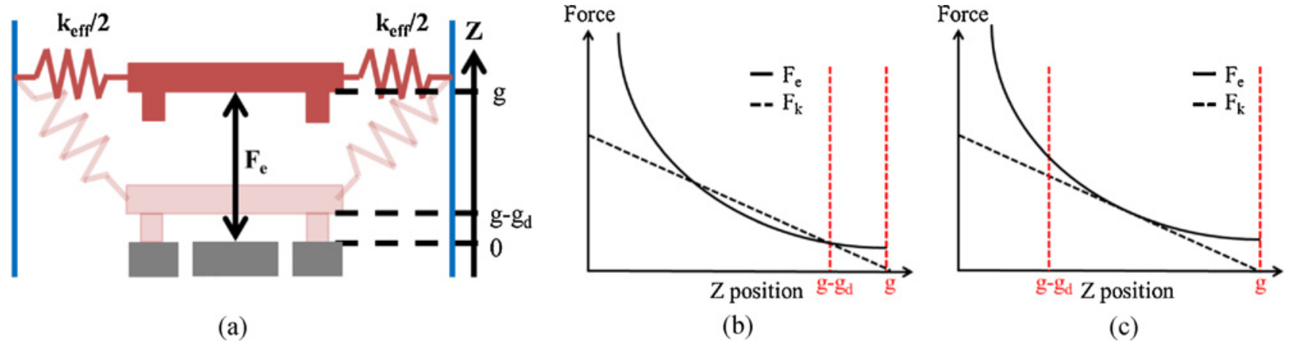

Fig. 2. (a) Conceptual illustration of a logic relay in the on state (pink) or off state (red). Force *vs*. Z-position curves for (b) a relay designed for non-pull-in mode operation, *i.e.* small g_d/g ratio, and (c) a relay designed for pull-in-mode operation, *i.e.* large g_d/g ratio. The F_e curves are for $V_{GB} = V_{PI}$.

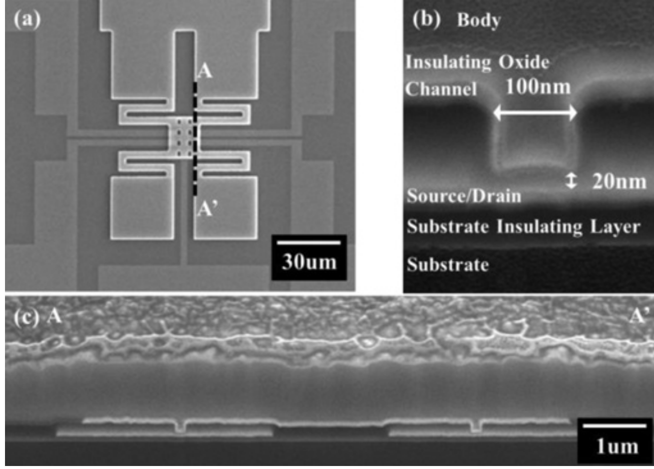

Fig. 3. SEM analyses of a MEM logic relay with ultra-small contact dimples: (a) plan view, (b) cross-sectional view of contact dimple region, (c) cross sectional view through the channel region.

In this work, functional logic relay consist of folded flexure beams and a center plate with contact dimples is used as shown in Fig. 1. Since F_e only exists between the center parallel plate, F_e can be easily computed, as a result F_a can be extracted simply by measuring pull in and release voltage. The adhesive force is investigated in MEM logic relays with dimpled contact regions of length ranging from 1.5 μm down to 100 nm. The experimental results are then compared to theoretical modeling to elucidate the magnitude and scaling behavior of F_a. Minimal switching energy of a relay for a scaled contact width is projected based on experimental results.

II. Relay Structure, Operation and Fabrication

Fig. 1 illustrates the structure and current-*vs*.-voltage (I-V) characteristic of an electrostatically actuated relay designed for digital logic applications. The movable body electrode is suspended by folded-flexure beams above the source, drain and gate electrodes. No current flows in the off state because the channels (conductive strips attached underneath the body via an intermediary dielectric layer of Al_2O_3) are separated from the source/drain electrodes by the contact dimple gap. If a voltage is applied between the gate and body electrodes, the resultant electrostatic attractive force (F_e) will actuate the body downward. When the applied gate-to-body voltage (V_{GB}) is greater than or equal to the pull-in voltage (V_{PI}), the channels will come into contact with the underlying source/drain electrodes, so that current can flow and hence the device is in the on state. Note that the current increases abruptly as V_{GB} is increased above V_{PI} to turn on the device. To turn off the device, V_{GB} must be reduced below the release voltage (V_{RL}) such that $F_k \geq F_e + F_a$ and the channels will come out of contact with the source/drain electrodes. Note that the current decreases abruptly as V_{GB} is decreased below V_{RL} and that $V_{RL} < V_{PI}$.

The hysteresis voltage ($V_{PI} - V_{RL}$) depends on the relative sizes of the as-fabricated (*i.e.* $V_{GB} = 0$) contact dimple gap (g_d) and actuation gap (g), as explained with the aid of Fig. 2: In the on state, the vertical (Z) position of the body is reduced (from g) to g-g_d. F_e increases superlinearly whereas F_k increases linearly with decreasing Z-position. If g_d is small (less than $\sim$g/3) as shown in Fig. 2(b), then F_e does not overtake F_k before the Z-position decreases to g-g_d; in other words, at $V_{GB} = V_{PI}$ $F_e = F_k$ so that V_{GB} only needs to be reduced slightly to reduce F_e by F_a in order to turn off the relay. If g_d is large (greater than $\sim$g/3), however, then F_e exceeds F_k when the relay is on (and the relay is said to be "pulled in"), so that F_e needs to be reduced by more than F_a to turn off the relay, as shown in Fig. 2(c). Therefore, the hysteresis voltage is larger for a relay designed to operate in pull-in mode.

F_a can be extracted from measurements of V_{PI} and V_{RL}, which are given by the following equations [9]:

$$V_{PI} = \sqrt{\frac{8k_{eff}g^3}{27\varepsilon_o A_{ov}}} \quad \text{pull-in mode} \tag{1}$$

$$V_{NPI} = \sqrt{\frac{2k_{eff}g_d(g-g_d)^2}{\varepsilon_o A_{ov}}} \quad \text{non-pull-in mode} \tag{2}$$

$$V_{RL} = \sqrt{\frac{2(k_{eff}g_d - F_a)(g-g_d)^2}{\varepsilon_o A_{ov}}} \tag{3}$$

where k_{eff} is the effective spring constant and A_{ov} is the effective area of overlap between the gate and body electrodes. By rewriting (1) or (2) to obtain k_{eff} as a function of V_{PI} or V_{NPI}, and substituting into (3), an expression for F_a as a function of V_{PI} or V_{NPI} and V_{RL} can be obtained:

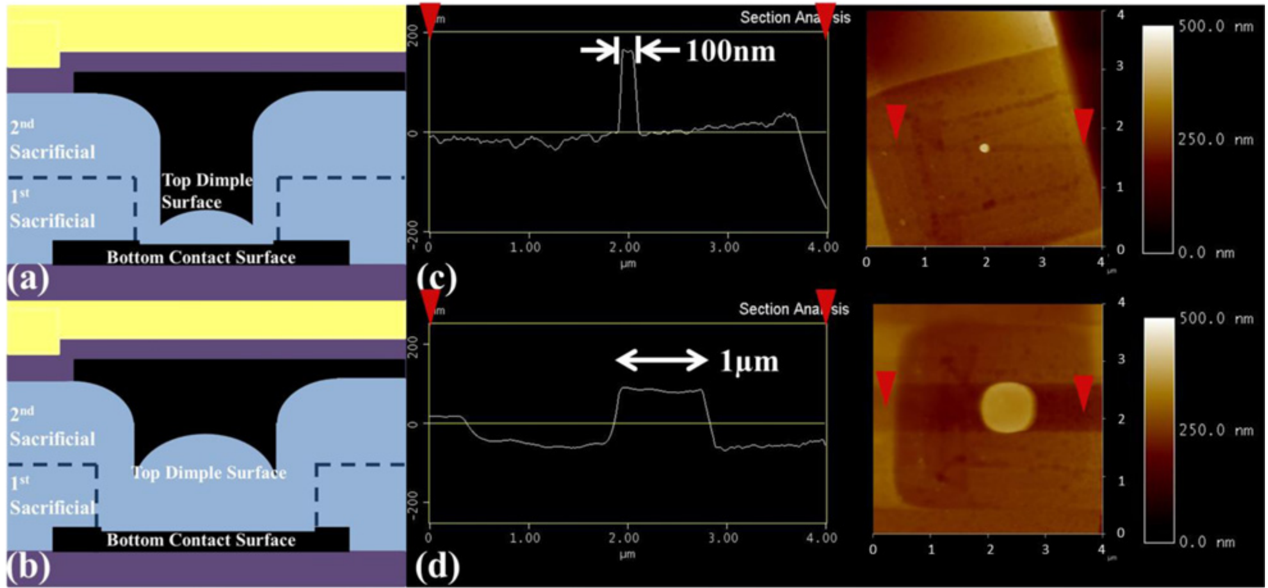

Fig. 4. (a) Schematic cross section of small contact dimple. Due to poor conformality of deposition, the 2nd sacrificial LTO layer is thinner in the contact region, so that the as-fabricated dimple gap (g_d) is smaller. (b) Schematic cross section of a large contact dimple. (c) AFM scan of a 100 nm-wide contact dimple (upside down). (d) AFM scan of a 1 μm-wide dimple (upside down).

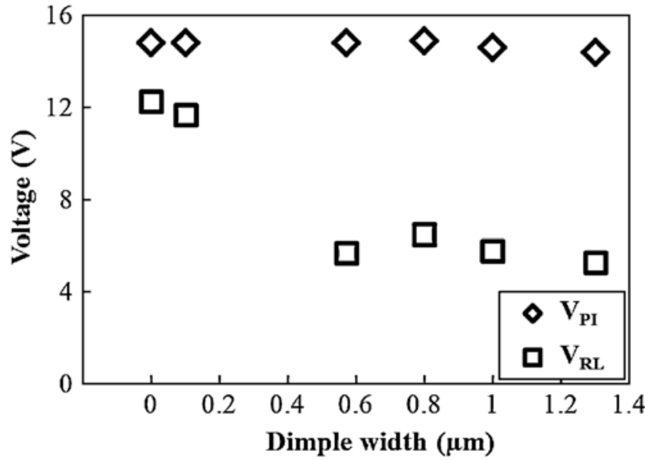

Fig. 5. Measured pull-in and release voltages of MEM logic relays of various contact dimple sizes. Theoretical values for the case of zero adhesive force are shown for "0" dimple width, for reference. (Note that the hysteresis voltage in this case is due purely to pull-in mode operation.).

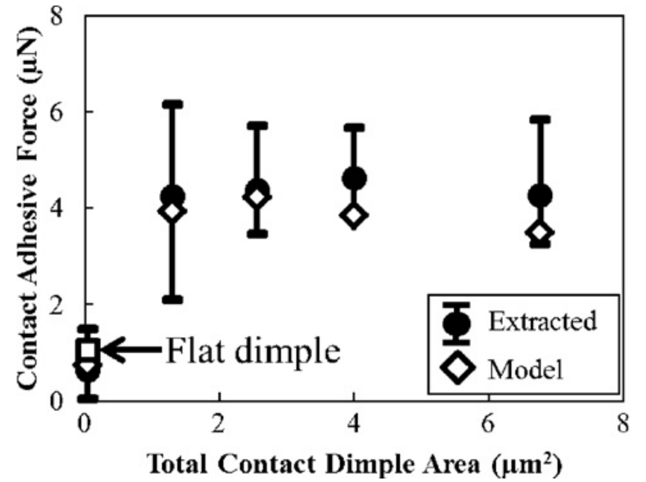

Fig. 6. Extracted F_a *vs.* total contact dimple area. Modeling results assuming 1.5 nm surface roughness are indicated with diamond symbols. Also shown is the modeling result for the case of a non-curved contact dimple surface.

$$F_a = \frac{27 g_d \varepsilon_o A_{ov}}{4 g_3} V_{PI}^2 - \frac{\varepsilon_o A_{ov}}{2(g - g_d)^2} V_{RL}^2 \qquad \text{pull-in mode} \quad (4)$$

$$F_a = \frac{\varepsilon_o A_{ov}}{2(g - g_d)^2} (V_{NPI}^2 - V_{RL}^2) \qquad \text{non-pull-in mode} \quad (5)$$

The 6-terminal MEM logic relays used to investigate F_a scaling in this work were fabricated as follows. First, 100 nm Al_2O_3 was deposited via atomic layer deposition (ALD) to insulate the surface of the Si wafer substrate. Then, 50 nm tungsten (W) was deposited by sputtering and patterned to form the source, drain and gate electrodes. Next, 100 nm SiO_2 (low temperature oxide, or LTO) was deposited via low-pressure chemical vapor deposition (LPCVD) to form the first sacrificial layer, and patterned to define the contact dimple regions. Afterwards, a second layer of sacrificial LTO was deposited to provide for the contact dimple gap. Then, 50 nm W was sputtered and patterned to form the channels, and 50 nm Al_2O_3 was deposited by ALD to insulate the channels from the body. Prior to deposition of 1 μm p-type polycrystalline-$Si_{0.4}Ge_{0.6}$ structural/body material by LPCVD, via holes were etched through the sacrificial layers to form anchor and interconnect regions. Lastly the structures were released by selectively removing the sacrificial LTO layers in HF vapor. Fig. 3 shows plan-view and cross-sectional scanning electron microscopy (SEM) images of a fabricated relay.

III. Results and Discussion

In order to accurately extract F_a, the relay mode of operation first must be identified; *i.e.* the contact dimple gap

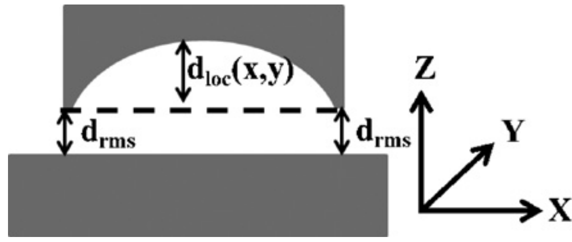

Fig. 7. Illustration of the modeled contact geometry. Surface roughness results in an average separation distance d_{rms}. The local separation distance between contacts is $d_{total} = d_{rms} + d_{loc}$. The radius of curvature for the top surface is 10.5 μm, based on AFM measurements.

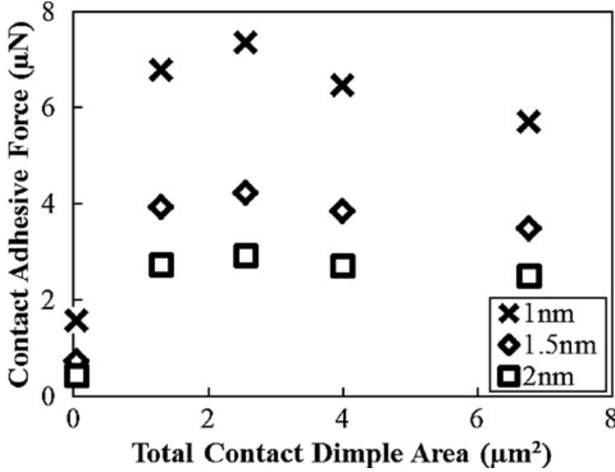

Fig. 8. Modeled van der Waals force *vs.* total contact dimple area, for various values of rms roughness of the contact dimple surface. As surface roughness decreases, the average separation distance decreases and F_a increases.

and actuation gap for zero bias must be accurately measured. (They cannot be assumed based on the thicknesses of the sacrificial layers used during the device fabrication process, due to the effects of non-conformal thin-film deposition in the contact dimple region and non-zero strain gradient within the structural material.) Optical interferometry measurements were performed to determine the out-of-plane deflection of the structure. It was discovered that all of the relays operate in pull-in mode (although the sacrificial layer thicknesses were chosen to achieve non-pull-in-mode operation), due to out-of-plane deflection resulting in both increased g and increased g_d.

In order to examine the contact geometry and topography precisely, the relay structures were carefully lifted off the substrate using carbon tape, and atomic force microscopy (AFM) was used to profile the contact dimple region. The smallest dimple examined has a width ~100 nm and height 160 nm. The dimple height was found to increase with decreasing dimple width due to poor conformality of the LPCVD process. Also, all dimples were found have a raised perimeter, so that contact to the underlying source/drain electrodes (when a relay is in the on state) is likely only made along the perimeter of the dimple. Fig. 4 shows AFM scans of a large dimple and the smallest dimple.

Fig. 5 plots the measured values of V_{PI} and V_{RL} as a function of contact dimple width. Since the relays all have

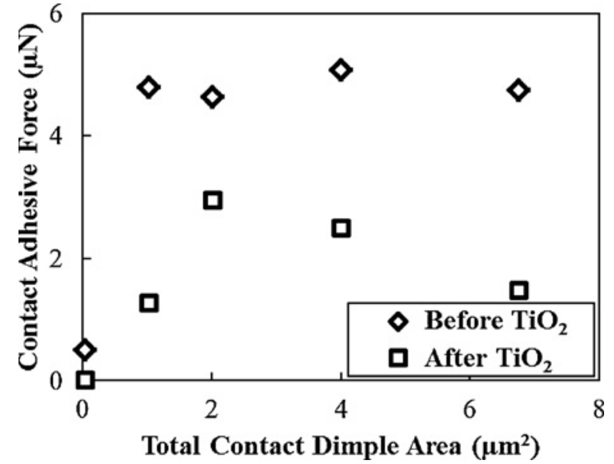

Fig. 9. F_a (extracted from V_{PI} and V_{RL} measurements) *vs.* total contact dimple area before and after ALD TiO_2 coating. F_a is reduced significantly after coating since TiO_2 has a lower Hamaker constant than W.

the same values of g, k_{eff} and A_{ov}, V_{PI} does not vary with dimple width. It can be seen that the hysteresis voltage is significantly reduced for the relay with the smallest contact dimples. Shown for reference are the theoretical values of V_{PI} and V_{RL} for zero adhesive force. (The hysteresis voltage in this case is due purely to pull-in-mode operation, and should scale with V_{PI}.)

Fig. 6 plots the range of extracted F_a values (using Eqn. (4)) as a function of the contact dimple area. 15 relays of each contact dimple size were measured. Large variation in F_a is seen for the larger contact dimple areas, with an average value ~4.5 μN that does not scale with area. Significantly (6×) lower F_a and less variation is seen for the smallest contact dimple area. Theoretical modeling is presented in the following section to explain these results.

IV. Contact Geometry and Adhesive Force Modeling

Adhesive forces include capillary force, van der Waal force and material bonding [10]. Since a dry release process was used for the relays studied in this work, capillary force should be negligible. Material-to-material bonding should yield a constant adhesive force regardless of contact dimple area [7], because the number of contacting asperities remains approximately the same. Since the observed adhesive force is not constant - in fact it is significantly reduced for the smallest contact dimple - van der Waals force is likely predominant in the relays studied in this work.

The van der Waals force between two surfaces can be modeled by the following equation:

$$F_V = \frac{HA_c}{6\pi d^3} \tag{6}$$

where H is the Hamaker constant, d is the distance between the two surfaces and A_C is the contact area assuming that the surfaces are flat. The Hamaker constant for tungsten is 40×10^{-20} J [11]. In order to adapt this model to the logic

relays in this work, the topography and the roughness of the contact dimples must be considered.

As shown in Fig. 4, the dimple surface is concave due to a non-conformal sacrificial-LTO deposition process. In contrast, the surface of the bottom electrode (which is contacted by the dimple when the relay is in the on state) is roughly planar. The van der Waals force at any location along the contact dimple surface is dependent on its separation from the bottom electrode surface, which is dependent on the curvature of the contact dimple surface as well as the surface roughness:

$$F_V = \int_{A_C} \frac{H dA}{6\pi(d_{loc}(x, y) + d_{rms})^3} \tag{7}$$

where d_{rms} is an equivalent rms roughness of the two contacting surfaces and d_{loc} is the local distance between the two contacting surfaces. The roughness of the bottom electrode is measured with an AFM. Since it is very difficult to measure the roughness of the contact dimple, estimations are made based on typical measured rms surface roughness of the 2nd sacrificial layer. The modeled contact geometry is shown in Fig. 7.

The modeled van der Waals force is shown in Fig. 8, for various values of rms surface roughness. It can be seen to be roughly independent of contact dimple size, for total contact dimple area larger than 1 μm^2, and to decrease significantly for the smallest total contact area (0.04 μm^2). This behavior can be explained qualitatively by the fact that, while the perimeter of the contact dimple decreases the average separation between contacting surfaces also decreases with decreasing contact size. However, for very small contact sizes the effect of the surface curvature becomes negligible, so that F_a scales with contact size. The effect of decreasing average separation is more pronounced for lower surface roughness.

The modeled van der Waals force for 1.5 nm rms surface roughness well explains the experimental findings, as shown in Fig. 6. The large variation in F_a observed for the larger contacts is most likely due to variations in contact dimple surface curvature, which is confirmed by AFM measurements of several contact dimples. For reference, the van der Waals force assuming flat contacting surfaces is also shown in Fig. 6 for the smallest contact dimple area. Since the effect of surface curvature on F_a is relatively minor at that point, it can be used to estimate the van der Waals force per unit area: 0.02 nN/nm^2.

Given the van der Waals force per contact area, one can estimate the minimal switching energy for a relay as a digital logic device. The switching energy of a relay is simply the energy to charge the gate to body capacitor; the expression for a pull-in mode device is shown as the following:

$$E_s = C_{gb} V_{PI}^2 = \frac{8 k_{eff} g^3}{27(g - g_d)} \tag{8}$$

In order for the relay to turn off, F_k must be larger than F_a, which gives the minimum constraint for spring constant and the minimum switching energy:

$$k_{eff} > \frac{F_a}{g_d} \tag{9}$$

$$E_s > \frac{8 F_a g^3}{27 g_d (g - g_d)} \tag{10}$$

For a relay fabricated using 8 nm process technology, with 5 nm dimple gap, the operating voltage for a 6-terminal relay is projected to be as low as 0.09 V, with a switching energy of 45 aJ. To reduce F_a one can further miniaturize the contact dimples or alter the contacting surface material. To demonstrate the latter approach, relays were coated with an ultra-thin layer of TiO_2 of $\sim$0.5 nm by ALD and then electrically characterized. The extracted F_a values plotted in Fig. 9 verify that TiO_2 has a lower Hamaker constant than W.

V. Conclusion

6 terminal relay structures with dimple contacts provide a simple way to extract contact adhesive force without the need of FEM simulations. Contact adhesion in MEM logic relays is found to be predominantly due to van der Waals force and hence can be reduced by employing contacting materials with lower Hamaker constant. Experimentally observed non-linear scaling of contact adhesive force with apparent contact area is well explained by a non-planar contact dimple surface in combination with surface roughness. For very small contact sizes, the effect of the surface curvature becomes negligible, so that F_a should scale with contact size.

The adhesive force for a tungsten-to-tungsten contact is found to be 0.02 nN/nm^2, this will result in a minimum switching energy of 45aJ for a 8 nm feature size NEM relay. It is shown that to further reduce the switching energy, ultra-thin oxide coating such as TiO_2 can be used in the future to reduce the van der Waals force between contacts.

Acknowledgement

The MEM relays were fabricated in the UC Berkeley Marvell Nanofabrication Laboratory.

References

[1] M. Spencer, F. Chen, C. C. Wang, R. Nathanael, H. Fariborzi, A. Gupta, H. Kam, V. Pott, J. Jeon, T.-J. King Liu, D. Markovic, E. Alon, and V. Stojanovic, "Demonstration of integrated micro-electro-mechanical relay circuits for VLSI applications," *IEEE J. Solid State Circuits*, vol. 46, no. 1, pp. 308–319, Jan. 2011.

[2] R. Nathanael, V. Pott, H. Kam, J. Jeon, and T.-J. K. Liu, "4-terminal relay technology for complementary logic," in *Proc. IEEE IEDM Tech. Dig.*, 2009, pp. 223–226.

[3] J. Rubin, R. Sundararaman, M. K. Kim, and S. Tiwari, "A single lithography vertical NEMS switch," in *Proc. IEEE Int.* Conf. *Micro Electro Mech. Syst.*, Jan. 2011, pp. 95–98.

[4] N. Sinha, T. Jones, Z. Guo, and G. Piazza, "Demonstration of low voltage and functionally complete logic operations using body-biased complimentary and ultra-thin AlN piezoelectric mechanical switches," in *Proc. IEEE Int. Conf. Micro Electro Mech. Syst.*, Jan. 2010, pp. 751–754.

[5] R. Nathanael, J. Jeon, I. Chen, Y. Chen, F. Chen, H. Kam, and T.-J. K. Liu, "Multi-input/multi-output relay design for more compact and versatile implementation of digital logic with zero leakage," in *Proc. Very Large Scale Iintegr. Technol. Syst. Applicat.*, 2012.

[6] H. Kam, V. Pott, R. Nathanael, J. Jeon, E. Alon, and T.-J. K. Liu, "Design and reliability of a MEM relay technology for zero-standby-power digital logic applications," in *Proc. IEEE IEDM Tech. Dig.*, Dec. 2009, pp. 809–812.

[7] I. Laboriante, B. Bush, D. Lee, F. Liu, T.-J. King-Liu, C. Carraro, and R. Maboudian, "Interfacial adhesion between rough surfaces of polycrystalline silicon and its implications for M/NEMS technology," *J. Adhes. Sci. Technol.*, vol. 24, nos. 15–16, pp. 2545–2556, 2010.

[8] F. DelRio, M. de Boer, J. Knapp, E. Reedy, Jr, P. Clews, and M. Dunn, “The role of van der Waals forces in adhesion of micromachined surfaces, ” *Nat. Mater.*, vol. 4, no. 8, pp. 629–634, Aug. 2005.
[9] S. D. Senturia, *Microsystems Design*, New York, NY, USA: Springer, 2001.
[10] B. D. Jensen, K. Huang, L. L. W. Chow, and K. Kurabayashi, “Adhesion effects on contact opening dynamics in micromachined switches,” *J. Appl. Phys.*, vol. 97, no. 10, p. 103535, May 2005.
[11] I. W. Osborne-Lee, “Calculation of Hamaker coefficients for metallic aerosols from extensive optical data,” in *Particles on Surfaces,* Vol. 1. New York, NY, USA: Plenum, 1988, pp. 77–90.

Jack Yaung received the B.S. degree in electrophysics from National Chiao Tung University, Taiwan. He is currently pursuing the Ph.D. degree in electrical engineering in the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA, USA. His current research interests include scaling of microelectromechanical relays for digital logic and advanced process for nanoscale mechanical devices.

Louis Hutin (M’11) was born in Evreux, France, in 1985. He received the Joint International M.Sc. degree in micro and nanotechnologies from the Grenoble Institute of Technology, France, the Politecnico di Torino, Italy, and the École Polytechnique Fédérale de Lausanne, Switzerland in 2007, and the Ph.D. degree in micro and nanoelectronics from the Grenoble Institute of Technology in 2010. From 2007 to 2010, his research at CEA-Leti, Grenoble, France, focused on high-mobility channel MOSFETs for advanced substrates (sSOI, SiGeOI, GeOI), and Schottky-junction transistors. He joined the University of California, Berkeley, CA, USA, in 2010 as a Post-Doctoral Researcher, where he is currently focusing on the optimization and scaling of micro/nanoelectromechanical relays for ultralow-power digital logic circuits.

Jaeseok Jeon received the B.A.Sc. degree with first-class honors in electronics engineering from Simon Fraser University, Burnaby, BC, Canada, in 2007, and the Ph.D. degree in electrical engineering from the University of California, Berkeley, CA, USA, in 2011. In 2011, he joined Rutgers, The State University of New Jersey, as an Assistant Professor in the Department of Electrical and Computer Engineering. In 2006, he was an Electronics Designer at the Kodak Graphic Communications Group, Toronto, ON, Canada. His research interests include nano-electronic materials, devices, and processing technologies. He was a recipient of the 2006 NSERC-USRA Award. He was a co-recipient of the 2011 ISSCC Jack Raper Award for Outstanding Technology Directions.

Tsu-Jae King Liu (SM’00–F’07) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA. From 1992 to 1996, she was a member of Research Staff at the Xerox Palo Alto Research Center, Palo Alto, CA, USA. In August 1996, she joined the faculty of the University of California, Berkeley, CA, USA, where she is currently the Conexant Systems Distinguished Professor of Electrical Engineering and Computer Sciences, and EE Division Chair and Associate Chair with the EECS Department. She has authored or co-authored over 400 publications and holds over 80 U.S. patents. Her research activities are currently in nanometer-scale logic and memory devices, and advanced materials, process technology, and devices for energy-efficient electronics.

Dr. Liu was a recipient of the DARPA Significant Technical Achievement Award in 2000 for the development of the FinFET, the IEEE Kiyo Tomiyasu Award in 2010 for contributions to nanoscale MOS transistors, memory devices, and MEMs devices, and the Intel Outstanding Researcher in Nanotechnology Award in 2012. She has served on committees for many technical conferences, including the IEEE International Electron Devices Meeting and the IEEE Symposium on VLSI Technology, and served as an Editor for IEEE ELECTRON DEVICES LETTERS from 1999 to 2004.