A Novel Digital Etch Technique for Deeply Scaled III-V MOSFETs

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***Abstract*— We demonstrate a new digital etch technique for controllably thinning III–V semiconductor heterostructures with sub-1-nm resolution. This is a two-step process consisting of low-power O_2 plasma oxidation, followed by diluted H_2SO_4 rinse for selective oxide removal. This approach can etch a combination of InP, InGaAs, and InAlAs in a precise and nonselective manner. We have also developed a method to determine the etch rate per cycle, and to control the etch depth in actual device structures. For InP, the etch rate is ∼0.9 nm/cycle. We illustrate the new process by fabricating L_g = 60-nm self-aligned buried-channel InGaAs MOSFETs. These devices feature a composite gate dielectric consisting of 1-nm InP and 2-nm HfO_2 for an overall sub-1-nm effective oxide thickness. A typical device shows a peak transconductance of 1.53 mS/μm (V_{ds} = 0.5 V), subthreshold swing of 89 mV/decade, and 102 mV/decade at V_{ds} = 0.05 and 0.5 V, respectively, and ON current of 326 μA/μm at I_{OFF} = 100 nA/μm and V_{dd} = 0.5 V.**

***Index Terms*— Digital etch, InGaAs, quantum-well devices, MOSFETs, buried-channel, self-alignment.**

I. Introduction

InAs-RICH InGaAs exhibits outstanding electron transport properties and is a promising channel material for future CMOS applications [1]. Significant progress has recently taken place on InGaAs MOSFET research [2]–[6]. Future CMOS requires ultra-scaled III-V device architectures such as thin-body planar, Nanowire or Trigate MOSFETs. To realize these structures, common wet etch techniques cannot be used. A method to precisely etch III-Vs heterostructures containing InP, InGaAs and InAlAs is highly desirable.

Digital etch techniques have been proposed to etch Silicon and III-Vs [7]–[13]. In this approach, the two elemental components of etching, oxidation and oxide removal, are applied separately. For III-Vs, a typical oxidation agent is an H_2O_2 solution while the native oxide is stripped by acids [9], [10]. This scheme can result in chemical cross contamination that leads to poor process repeatability. Recently, UV ozone was used for oxidation of InGaAs surface-channel devices, followed by oxide removal by HCl [11]. This addresses the cross contamination issue. This approach has only been demonstrated with InGaAs.

In this letter, we demonstrate a new digital etch process that allows the precise non-selective etching of InAlAs, InGaAs, and InP layer structures with sub-1 nm precision. We also introduce a method to determine the etch rate and etch depth. We show that the resulting surface is smooth and can be used directly for high-quality insulator-channel interface formation in InGaAs MOS applications. We demonstrate state-of-the-art self-aligned InGaAs QW-MOSFETs fabricated by this technique.

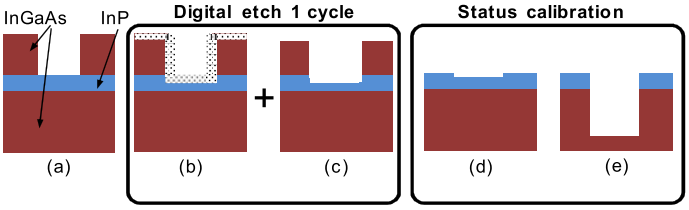

Fig. 1. Illustration of InP digital etch rate calibration (see text).

II. Experiment

Our digital etch approach consists of native III-V oxide formation through exposure to low power oxygen plasma in a commercial asher system. This is followed by oxide removal in diluted H_2SO_4 (H_2SO_4:H_2O=1:1) for 30 s at room temperature followed by DI rinse. By repeating these two steps, the semiconductor can be thinned down in a controlled manner.

Fig. 1 illustrates our approach to calibrating the etch rate of the thin InP barrier in the gate recess region of a buried-channel MOSFET. First [Fig. 1(a)], the top InGaAs cap is removed by well-established selective wet etching, leaving a gate recess opening (for tight lateral control, dry etching can also be used [13]). Following this, multiple cycles of digital etch are performed [Fig. 1(b) and (c)]. To calibrate the etch rate, one needs to know when the InP barrier is breached. For this, after a given number of cycles we cleave a small portion of the sample and dip it in H_2O_2:H_3PO_4:H_2O (1:1:25) for 30 s. In our calibrations, this solution etches InGaAs over InP with a selectivity of at least 100 to 1. If even a small amount of InP (>0.5 nm) is left [Fig. 1(c)], this etchant only removes the InGaAs cap and the sample appears almost perfectly flat under an optical microscope [Fig. 1(d)]. On the other hand, if the InP barrier has been breached, the H_3PO_4 solution produces readily visible trenches in the underlying InGaAs layer [Fig. 1(e)]. If the thickness of the InP layer is

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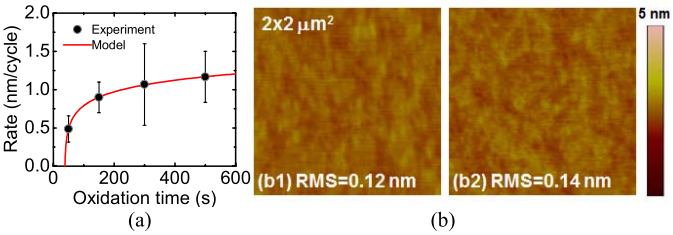

Fig. 2. (a) Etch rate per cycle of digital etch as a function of oxidation time under O2 plasma, and fitting with Lukeš' model [14]. (b) Surface profile after: (b1) cap wet etch, and (b2) four additional cycles of digital etch surface, where ∼4 nm of InP have been removed.

known (from MBE calibrations or TEM), the etch rate can be determined.

Fig. 2(a) shows measured InP digital etch rate per cycle as a function of oxygen exposure time. The InP etch rate increases for the first 150 s of oxidation time but it then saturates to a rate of about 0.9 nm/cycle. Here we assume that the native oxide is completely removed in every cycle and therefore the etch rate is directly proportional to the oxide thickness. The saturation behavior in Fig. 2(a) reflects the self-limiting nature of the oxidation process; once the oxide thickness is thick enough, the diffusion rate of oxidizing species is sharply curtailed. The data between 50 to 500 s follows Lukeš' rate law for GaAs oxidation [14]: $\boldsymbol{d=A+B\cdot log(t+t_0)}$ with fitting parameters A =0 nm, B =0.44 nm/dec and $t_o = -37$ s. The negative t_0 value reflects the incubation time of the O_2 plasma oxidation process. Because of this, the fitting applies for $t + t_o > 0$.

The error bars in the etch rate data shown in Fig. 2(a) come from two sources of uncertainty. First, the discrete nature of digital etch cannot resolve fractions of an etch cycle. Using a thicker InP layer for calibration can reduce this error. Second, non-uniformities in the etch rate (especially for low oxidation rates) or in the initial layer thickness can result in the sample not clearing entirely and uniformly within the same etch cycle. However, the uncertainty of etch rate is not a significant problem when it comes to precise etching of a given structure as we show below. We can still control the etch depth down to sub-1 nm without knowing precisely the etch rate.

MOSFET applications require a high-quality semiconductor surface prior to high-k deposition. Fig. 2 also shows AFM surface scans (b1) after InGaAs cap wet etch, and (b2) after four additional cycles of digital etch. Only very subtle roughening of the surface after digital etch is observed, from an RMS roughness of 0.12 nm to 0.14 nm.

Usually the cap in a recessed-gate III-V FET heterostructure includes multiple layers of various semiconductors, such as InP and InAlAs [6], [13]. When those layers need to be recessed, even if the etch rate for those materials might be different, the method depicted in Fig. 1 can be used to determine the number of cycles "N" that it takes to etch all layers and breach through the final InP barrier regardless of the composition and etch rate of those layers. As a result, when using "N − 1" cycles, the device will be left with less than 1 nm of InP above the channel.

We have used the InP-terminated digital etch to fabricate buried-channel self-aligned InGaAs MOSFETs with a scaled

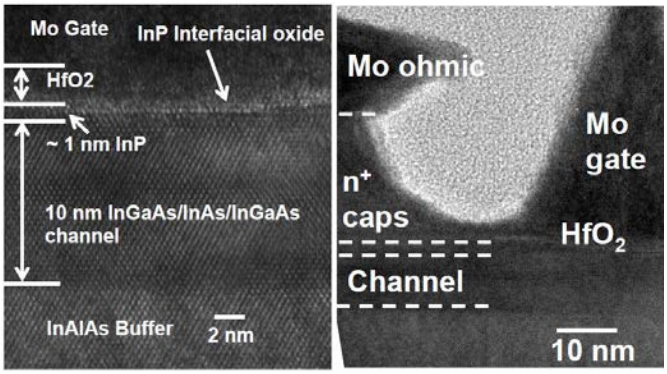

Fig. 3. High resolution TEM cross-sections of QW-MOSFET with ∼1 nm InP barrier. (a) Intrinsic gate region. (b) Extrinsic ledge region that connects the source/drain to the gate edge.

down barrier. More details of the device and process design are given in [6]. Above the channel and from the top down, our heterostructure contains a heavily-doped InGaAs cap followed by a composite n^+-InP/n^+-InAlAs/i-InP (3/3/3 nm) ledge designed to provide low-resistance access to the intrinsic device. The original thickness of the i-InP etch stop layer is 3 nm. This complex layer structure must be precisely etched to leave about 1 nm i-InP above the channel. We accomplish this through a combination of wet etch to remove the InGaAs cap above the n^+-InP, followed by 5 cycles of digital etch with the O_2 plasma oxidation lasting 150 s and the oxide removal taking 30 s in H_2SO_4. Immediately after the last cycle of digital etch and DI rinse, 2 nm of HfO_2 is ALD deposited directly on top of the InP barrier. The total EOT of 1 nm InP plus 2 nm HfO_2 is 0.8 nm.

Fig. 3 shows high-resolution TEM cross sections of the MOSFET structure after the gate is fully formed. A thin InP native oxide layer is visible below the HfO_2 dielectric [Fig. 3(a)]. Fig. 3(b) shows the extrinsic access region that connects the source/drain contact structure to the gate edge. The rounded-edge profile of the cap results from the isotropic nature of both, the cap wet etch and the digital etch.

III. Results and Discussion

Fig. 4(a) shows the output characteristics of a 60 nm gate length MOSFET fabricated by this process. The device exhibits sharp saturation and good turn off. R_{on} is 485 $\Omega\cdot\mu$m at the highest V_{gs}–V_t of 0.6 V. The transfer and transconductance characteristics are shown in Fig. 4(b). The peak transconductance at $V_{ds} = 0.5$ V is 1.53 mS/μm with the transfer curves showing negligible hysteresis. The subthreshold and gate current characteristics are shown in Fig. 4(c). A subthreshold swing of 89 mV/dec is obtained at $V_{ds} = 0.05$ V, and 102 mV/dec at 0.5 V. This is one of the lowest subthreshold swings ever reported in this gate length dimension ($L_g \leq 60$ nm) for planar III-V MOSFETs [6]. Drain induced barrier lowering (DIBL) is 156 mV/V. The gate leakage current is very low ($I_g < 1 \times 10^{-8}$ A/μm). The device combines excellent current drive and control of short-channel effects. At $I_{off} = 100$ nA/μm and $V_{dd} = 0.5$ V, it delivers an ON current of 326 μA/μm. This is the second highest

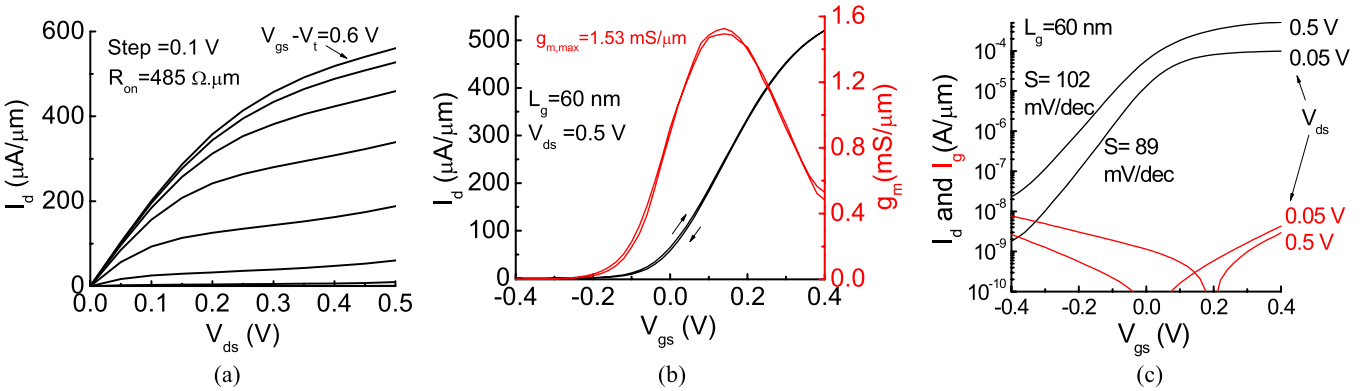

Fig. 4. Performance of a L_g = 60 nm QW-MOSFET fabricated by the proposed digital etch technique. (a) Output characteristics. (b) Transfer and transconductance characteristics. (c) Subthreshold and gate leakage current characteristics.

value demonstrated in any III-V MOSFETs for $L_g \leq 60$ nm [2]–[6], [11]–[13]. A higher value has been recently demonstrated by using a combination of cap RIE etch and the digital etch presented here. This allows for further EOT scaling and an optimized access region with low R_{sd} [13].

Long channel ($L_g = 20\ \mu$m) transistors with identical gate stack and channel configuration have also been fabricated using the same digital etch technique. A very high channel electron mobility of 4650 $cm^2V^{-1}s^{-1}$ at $N_s = 4 \times 10^{12}$ cm^{-2} has been extracted by the split-CV method.

IV. Conclusion

In summary, we introduce a new digital etch process for the precise etching of III-V heterostructures and a calibration method. We demonstrate the new techniques by fabricating short-channel and long-channel self-aligned InGaAs QW-MOSFETs. The high drive current, low leakage, negligible hysteresis, steep subthreshold swing and high mobility of those MOSFETs indicate the superior gate stack quality that results from our digital etch fabrication process that exposes a fresh InP surface right before gate oxide ALD.

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