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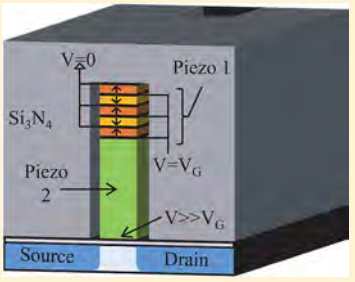
A Nanoscale Piezoelectric Transformer for Low-Voltage Transistors

Sapan Agarwal* and Eli Yablonovitch

Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California 94720, United States

ABSTRACT: A novel piezoelectric voltage transformer for low-voltage transistors is proposed. Placing a piezoelectric transformer on the gate of a field-effect transistor results in the piezoelectric transformer field-effect transistor that can switch at significantly lower voltages than a conventional transistor. The piezoelectric transformer operates by using one piezoelectric to squeeze another piezoelectric to generate a higher output voltage than the input voltage. Multiple piezoelectrics can be used to squeeze a single piezoelectric layer to generate an even higher voltage amplification. Coupled electrical and mechanical modeling in COMSOL predicts a 12.5× voltage amplification for a six-layer piezoelectric transformer. This would lead to more than a 150× reduction in the power needed for communications.



KEYWORDS: *Piezoelectric, transformer, subthreshold swing, field-effect transistor, low voltage*

In order to reduce the power consumption of modern electronics, the operating voltage needs to be significantly reduced. Unfortunately, conventional transistors fundamentally require around half a volt to switch. On the other hand, electrical wires only need millivolts to overcome noise and communicate information. This voltage mismatch results in a significant amount of power being wasted by charging the wires to a high voltage. To overcome this mismatch, either a new low voltage switch[1−5] or a voltage transformer is needed. In this paper, we propose a new CMOS compatible piezoelectric voltage transformer that can be placed on the gate of each transistor to reduce the voltage needed for switching. This results in the piezoelectric transformer field-effect transistor, or PT-FET.[6] The transformer can also be used with any capacitive device that requires a high electric field.

Conventional transformers operate on one of two principles. A typical magnetic transformer operates by converting electrical energy to magnetic energy and then back to electrical. By converting between energy forms the input and output voltage can be different. Alternatively, a switched capacitor or charge pump transformer operates by charging several capacitors in parallel and then discharging them in series. This allows the voltage across each capacitor to add in series. In designing a piezoelectric transformer we would like to take advantage of both principles.

The piezoelectric transformer was first invented in 1956.[7] It operates by converting electrical energy to mechanical energy and then back to electrical energy. An alternating current (ac) voltage is placed across a piezoelectric to generate a mechanical sound wave. This sound wave is used to compress a second piezoelectric to generate an output voltage that can be higher or lower than input voltage. To maintain a steady current these transformers need to operate at an ac voltage. They also need to operate near the mechanical resonance frequency to maintain a high power conversion efficiency. These limitations would make a conventional transformer useless for CMOS logic as the circuits must be able to operate at direct current (dc). Fortunately, transistors only require a high voltage on the gate and do not need a dc current through the gate. Consequently, a nanoscale piezoelectric transformer can be designed to amplify a dc voltage.

A nanoscale piezoelectric voltage transformer is illustrated in Figure 1c. First consider a single piezoelectric that is placed on the gate of a transistor as shown in Figure 1a. It is simply a high-k capacitor in series with the transistor gate capacitance. Next consider what happens when a compressive force is applied as shown in Figure 1b. Applying a compressive force induces a polarization charge on the piezoelectric. The series gate capacitance limits the amount of free charge that is generated as shown on the right of Figure 1b. Consequently, the polarization charge is greater than the free charge and induces an electric field. This electric field results in a voltage, V_{G2}, between C_{piezo} and C_g that is greater than the applied voltage V_G. Therefore, applying a force results in a higher output voltage than V_G. In Figure 1c, we show how to apply that force. The top piezoelectric is used to squeeze the bottom one, while the Si_3N_4 is used as a rigid frame. Applying a voltage to the top piezoelectric causes the piezoelectric to expand. This is illustrated on the right of Figure 1c by the positive and negative charge separating when an electric field is applied. When the top piezoelectric expands it will squeeze the lower one inducing a polarization charge and therefore a voltage increase.

In Figure 2, we show a simulated piezoelectric voltage transformer that results in a 4.5× voltage enhancement! For illustration, the top piezoelectric is $0.67Pb(Mg_{1/3}Nb_{2/3})O_3-0.33PbTiO_3$ (PMN−PT[8−10]) and the bottom piezoelectric is ZnO. There are many different choices[11,12] for the piezoelectrics such as AlN, PZT (lead zirconium titanate), SiO_2, or even HfO_2.[13] For instance, using PZT-5H for the top piezoelectric and AlN for the bottom piezoelectric gives a

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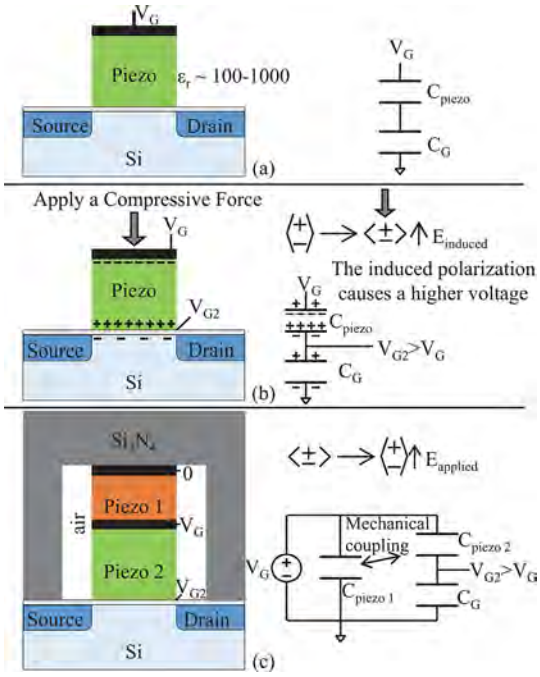

Figure 1. Operation of a piezoelectric transformer is illustrated (a) A single piezoelectric layer just acts like a series capacitor. (b) Applying a force to the piezoelectric induces a polarization charge which creates an electric field. The electric field results in a voltage, V_{G2}, between the piezoelectric and the gate oxide that is greater than V_G. (c) The required force can be provided by a second piezoelectric stacked directly on top of the first piezoelectric.

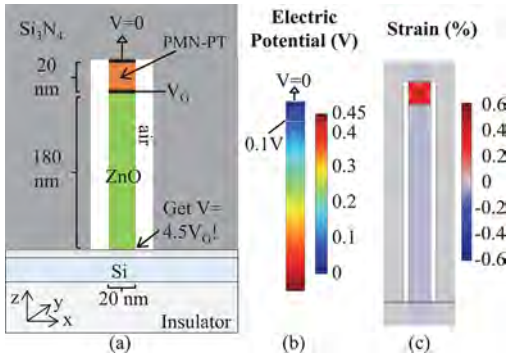

Figure 2. (a) This structure is simulated in COMSOL and gives a 4.5× voltage enhancement. The contacts are assumed to be 1 nm thick tungsten layers and the air gap is 5 nm wide. The transistor is electrically modeled as a 10 aF/μm capacitor. (b) The electric potential in the piezoelectrics is plotted. If 0.1 V is applied at the top gate, 0.45 V is measured at the bottom of the transformer. The potential scales linearly with the input voltage and so the enhancement is always 4.5× regardless of the input voltage (for a constant gate capacitance). (c) The strain, ε_{zz}, in the structure is plotted. The voltage across the top piezoelectric causes it to expand and compress the lower piezoelectric. The strain is proportional to the gate voltage and is shown for V_G = 0.1 V.

simulated voltage enhancement of 2.2×. The electric potential and mechanical strain are simulated using the finite element method in COMSOL multiphysics. For the proof of concept simulations, bulk values of the material parameters are used. The properties for PMN−PT are taken from ref 6, and the default values in COMSOL are used for ZnO.[14] In a nanoscale structure, the piezoelectric coefficient, d_{33}, in PMN−PT may reduce due to adhesion to the substrate. Fortunately, ferroelectricity continues down to the unit cell level[15] and recently high piezoelectric response relaxor ferroelectric thin films have been grown.[9] To estimate the impact of a reduced piezoelectric coefficient we can see what happens when we replace bulk PMN−PT (d_{33} = 2.5 nm/V) with bulk PZT-5H[14] (d_{33} = 0.6 nm/V). The voltage amplification reduces from 4.5× to a respectable 2.7×.

The MOSFET is electrically modeled by a single capacitor. The gate oxide in series with the transistor is assumed to have a total capacitance of 10aF/μm. This corresponds to an induced charge density of 3.1 × 10^{11} /cm^2 at an amplified voltage of 1 V. To switch with this low of a charge density, the depletion capacitance, source/drain capacitance, and other parasitic capacitances need to be reduced to less than 10aF/μm. The low capacitances can be achieved by using a fully depleted ultrathin body MOSFET. A longer channel length can also be used to reduce the impact of the source and drain as their capacitance is fixed, while the total charge increases as the channel length increases. The mechanical performance of the transformer can be maintained at a long channel length by using a narrow channel width, allowing the transformer to expand/shrink in the y-direction in Figure 2a. The trade-off between charge density and voltage amplification is discussed in more detail later.

The large 10:1 aspect ratio in the simulated structure allows the piezoelectrics to expand/contract in the lateral dimension and maximizes the voltage amplification. The structure can be optimized for smaller aspect ratios and larger dimensions by slightly reducing the voltage amplification. For instance with a 4:1 aspect ratio, 125 nm long channel, 100 nm thick PMN−PT on top, and 400 nm thick ZnO on the bottom, a 3.1× voltage enhancement is simulated. However, in the larger structure a lower charge density of 1 × 10^{11}/cm^2 is induced at an amplified voltage of 1 V. This is because the charge density is proportional to the electric field and applying the same voltage across a thicker device results in a lower electric field. The longer channel length allows for a higher total transistor capacitance of 20 aF/μm.

So far we have taken advantage of one mechanism to design a transformer: converting between energy forms. We can also use the concept of charging capacitors in parallel and discharging them in series. This is shown in Figure 3. A series of piezoelectric layers are charged in parallel and then mechanically connected in series with the bottom layer. By polling each of the top layers in alternating directions, all of the layers will expand when a voltage is applied to them. Consequently, each layer will add to the pressure on the bottom layer. This gives a voltage enhancement of 12.5×. This would correspond to a 156× reduction in power used to charge the wires ($P = CV^2$).

Next, we analytically derive this voltage enhancement in 1D. We consider the structure shown in Figure 4. Piezo 0 and Piezo 1 are oppositely polled so that they both expand and compress Piezo 2. This means that the displacement in Piezo 2, ΔL_2 will be n times the displacement in Piezo 1, ΔL_1, where n = 2 is the number of identical but oppositely polled top layers

$$\Delta L_2 = -n\Delta L_1 \quad (1)$$

Here we assumed that the Si_3N_4 frame, Si substrate, and metal contacts are perfectly rigid. As we will see later in the simulated results, some mechanical energy is lost due to deformation of the nitride and the silicon wafer. We also choose the area of the

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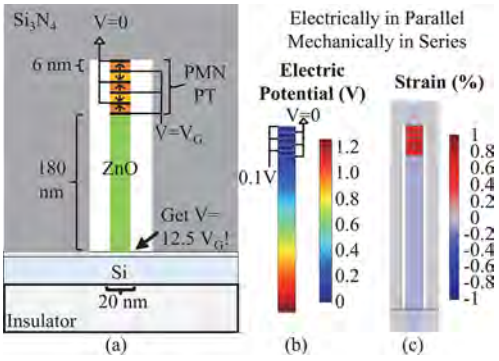

Figure 3. (a) Multiple oppositely polled piezoelectric layers can be used on top to increase the pressure on the bottom piezoelectric and thus increase the voltage enhancement. The contacts are assumed to be 1 nm thick tungsten layers and the air gap is 5 nm wide. The transistor is electrically modeled as a 10 aF/μm capacitor. (b) The electric potential in the piezoelectrics is plotted. If 0.1 V is applied across each of the top piezoelectrics, 1.25 V is measured at the bottom of the transformer. (c) The strain ε_{zz} in the structure is plotted.

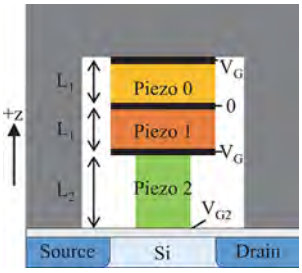

Figure 4. In this transformer, the upper piezoelectrics have a larger area than the lower piezoelectric. By using a stiff contact (such as tungsten) between Piezo 1 and Piezo 2, the stress in Piezo 2 can be increased by the ratio of the areas.

top piezoelectrics to be larger than the area of the bottom piezoelectric. Because the force must be the same on both, but the bottom piezoelectric has a smaller area, the stress will be larger

$$T_1 = T_2\frac{A_2}{A_1} \tag{2}$$

T_1 is the stress in Piezo 1, T_2 is the stress in Piezo 2, A_1 is the area of Piezo 1, and A_2 is the area of Piezo 2. This assumes that there is a perfectly rigid metal between the piezoelectric layers to transfer the force. In reality, the metal will deform slightly and so we will not get the full benefit of the area ratio. This can be modeled by an effective area ratio A_1/A_2 that is closer to 1 than the physical area ratio. Even with $A_1/A_2 = 1$ the transformer still operates as seen from Figure 2 and 3.

In general, a piezoelectric is described by a coupled set of equations[16]

$$S = sT + dE \tag{3}$$

$$D = dT + \varepsilon E \tag{4}$$

where S is the strain, s is the compliance (1/Pa), T is the Stress (Pa), d is the piezoelectric constant (m/V), E is the electric field (V/m), D is the electric displacement field (C/m^2), and ε is the permittivity (F/m). By applying these equations for Piezo 1 and 2 and using eq 1 and 2 to couple the layers, we can derive an expression for the voltage enhancement.

First, we apply eq 3 to Piezo 1 and use the fact that the applied electric field is V_G/L_1 where L_1 is the thickness of Piezo 1.

$$S_1 = s_1T_1 + d_1\left(\frac{V_G}{L_1}\right) \tag{5}$$

The subscript 1 is used to indicated the material properties of material 1. Multiplying by L_1 and using the fact that $S_1L_1 = \Delta L_1$ gives

$$\Delta L_1 = s_1T_1L_1 + d_1V_G \tag{6}$$

This equation shows that an applied voltage will induce a length change. It also shows that a smaller L_1 is desirable as it results in a higher T_1 for a given V_G and ΔL_1. However, 3D considerations require that L_1 approximately equal the channel length. This is because when the piezoelectric expands vertically, it needs to be able to contract laterally to approximately conserve its volume. Subsequently applying eq 4 to piezo 1 gives

$$D_1 = \frac{Q_1}{A_1} = d_1T_1 + \varepsilon_1\frac{V_G}{L_1} \tag{7}$$

The same equations apply to any additional top layers such as Piezo 0.

Next we need to consider Piezo 2. The electric field is given by $(V_{G2} - V_G)/L_2$. Plugging this into eq 3 and multiplying by L_2 gives

$$\Delta L_2 = s_2T_2L_2 + d_2(V_{G2} - V_G) \tag{8}$$

Applying a stress T_2 will compress Piezo 2 and induce a voltage $(V_{G2} - V_G)$. Equation 4 becomes

$$D_2 = d_2T_2 + \varepsilon_2\frac{(V_{G2} - V_G)}{L_2} \tag{9}$$

The induced surface charge is given by $D_2 = Q_2/A_2$. Equations 1 and 2 and eqs 6–9 form a system of equations that can be simplified to the following system

$$Q_1 = \frac{\varepsilon_1A_1}{L_1}V_G - d_1(nT_{12} + T_{21}) \tag{10}$$

$$Q_2 = \frac{\varepsilon_2A_2}{L_2}(V_{G2} - V_G) - d_2(nT_{12} + T_{21}) \tag{11}$$

where

$$T_{12} = \frac{d_1}{\frac{s_1nL_1}{A_1} + \frac{s_2L_2}{A_2}}V_G \tag{12}$$

$$T_{21} = \frac{d_2}{\frac{s_1nL_1}{A_1} + \frac{s_2L_2}{A_2}}(V_{G2} - V_G) \tag{13}$$

T_{12} is the stress caused by the voltage across each of the top layers. T_{21} is the stress caused by the voltage across the bottom layer. Equations 10 and 11 are the transformer equations for the piezoelectric transformer. Equation 11 can be solved for the voltage amplification by using the fact that the surface charge, Q_2, will be controlled by the gate capacitance

$$D_2 = \frac{Q_2}{A_2} = -C_GV_{G2} \tag{14}$$

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Plugging eq 14 into eq 11 and solving for V_{G2} gives

$$V_{G2} = \left(\frac{-nd_1d_2 + \left(ns_1L_1\frac{A_2}{A_1} + s_2L_2\right)C_G}{d_2d_2 - \left(ns_1L_1\frac{A_2}{A_1} + s_2L_2\right)\left(\frac{\varepsilon_2}{L_2} + C_G\right)} + 1 \right) V_G \tag{15}$$

This equation gives the voltage amplification provided by the transformer. To maximize the voltage amplification we want to maximize the first term in the numerator, nd_1d_2. We also want the terms in the denominator to cancel. However, the second term in the denominator will always be larger than the first term, d_2d_2. V_{G2} is maximized when C_G is small ($C_G \ll \varepsilon_2/L_2$). This corresponds to inducing a small amount of charge or driving a smaller load with the transformer. To maximize V_{G2}, the stress in Piezo 2 should be maximized by satisfying the following condition

$$\frac{nL_1}{L_2} \times \frac{A_2}{A_1} \ll 1 \text{ and } C_G \ll \frac{\varepsilon_2}{L_2} \tag{16}$$

Making $L_2 \gg nL_1 \times (A_2/A_1)$ maximizes the mechanical energy in Piezo 2. Taking these limits gives

$$V_{G2} = \left(\frac{-nd_1d_2}{d_2d_2 - (s_2L_2)\left(\frac{\varepsilon_2}{L_2}\right)} + 1 \right) V_G$$

$$= \left(n\frac{d_1}{d_2} \times \frac{1}{1/k_2^2 - 1} + 1 \right) V_G \tag{17}$$

where $k_2^2 = d_2/(s_2\varepsilon_2)$ is called the electromechanical coupling coefficient. It is the ratio of mechanical energy stored/electrical energy input and is always less than 1. For good piezoelectrics, k^2 is approximately 0.5 to 0.9.[8,16] Looking at eq 17 we see that there are three voltage enhancement factors we can take advantage of. First, we can increase n, the number of upper layers used to squeeze the bottom piezoelectric. Second, we can increase the ratio d_1/d_2. Increasing d_1 increases the stress induced by a given voltage across Piezo 1. Decreasing d_2 (while maintaining a high k_2) means that a given stress will induce a higher voltage in Piezo 2. Finally, we can increase the electromechanical coupling coefficient, k_2, so that it approaches 1. A high k_2 means that all the mechanical energy applied to Piezo 2 will be converted into electrical energy. Because we are considering the small charge/low C_G limit, the electrical energy will correspond to a high voltage as Energy = QV and Q is small.

Now that we have shown that an ideal transformer can give arbitrarily high voltage enhancement, we consider the optimization of the simulated structure shown in Figure 2. The materials, PMN-PT and ZnO were chosen to optimize the d_1/d_2 ratio and electromechanical coupling coefficient k_2 in eq 17. In Figure 5a–c, we show the voltage amplification versus the top piezoelectric thickness, bottom piezoelectric thickness, and metal contact thickness, respectively. There is an optimal thickness for each of the piezoelectrics. As the contact metal gets thicker, a small amount of mechanical energy is lost and so the voltage amplification decreases slightly. If we assume that the Si_3N_4 and Si form a perfectly rigid frame the voltage amplification would increase to 5.0× for the structure in Figure 2. However, due to the loss of mechanical energy, the voltage amplification is only 4.5×.

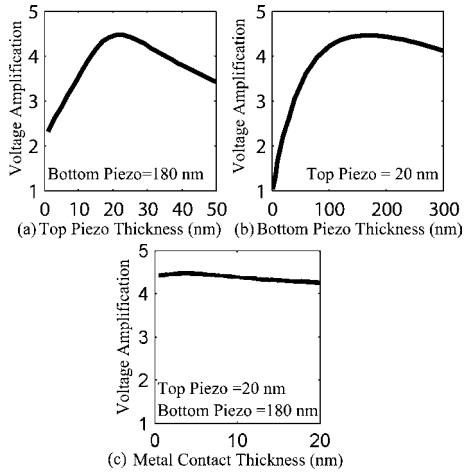

Figure 5. Voltage amplification versus (a) top piezoelectric thickness, (b) bottom piezoelectric thickness, and (c) metal contact thickness is shown. When the top piezoelectric is too thin, it is mechanically clamped (it cannot shrink laterally while expanding vertically to preserve volume) and so the amplification decreases. If the top piezoelectric is too thick or the bottom piezoelectric is too thin, the mechanical energy will be wasted in squeezing the top piezoelectric rather than the bottom one, resulting in a lower voltage amplification. If the bottom piezoelectric is extremely thick, the strain decreases and the bottom piezoelectric struggles to produce a sufficient amount of charge, decreasing the voltage amplification. As the metal contacts get thicker, the voltage slightly decreases as some mechanical energy is lost in the metal. Fortunately, using a stiff metal, tungsten, means that there is only a small change in amplification. In all the plots, the transistor is modeled by a 10aF/μm capacitor.

In Figure 6a, we show the voltage amplification versus induced charge density (eq 14) for an amplified voltage V_{G2} of 1 V. The voltage amplification drops to 1 if the transistor capacitance is too high. This is because the piezoelectric cannot provide enough charge if the capacitance is too high. Fortunately, low voltage operation requires less current and therefore less channel charge. The required charge can be

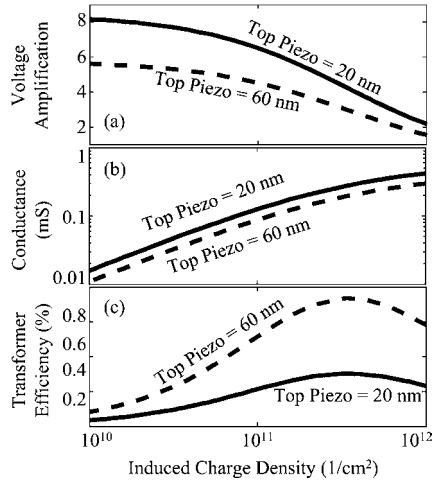

Figure 6. (a) Voltage amplification, (b) conductance, and (c) transformer efficiency are plotted versus the induced charge density for the structure in Figure 2. The amplified gate voltage, V_{G2}, is assumed to be 1 V. The dotted lines represent a thicker top PMN-PT layer of 60 nm. The thicker top piezoelectric reduces the PMN-PT capacitance and therefore increases the efficiency to nearly 1%.

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estimated from the required channel conductance. The drift velocity limited conductance is given by

$$\frac{I}{V_{SD}} = \frac{W}{L}\frac{Q}{A}\mu_e \tag{18}$$

For a conductance of 1 mS/um from a channel with a 400 $cm^2/(V\ s)$ mobility, we need a charge density of $3 \times 10^{11}/cm^2$. In a conventional transistor at a source drain bias of 1 V, the drift velocity would be 2×10^8 cm/s, which is 10 times higher than the thermal velocity of 1.2×10^7 cm/s in silicon. Consequently the velocity would be limited by the thermal velocity and $5 \times 10^{12}/cm^2$ carriers would be required in the channel to get a conductance of 1 mS/μm. Fortunately, at a low voltage less than 60 mV, the drift velocity would be less than the thermal velocity and so a channel carrier density of $3.1 \times 10^{11}/cm^2$ is needed. Using $Q = CV$ gives an effective transistor gate capacitance of 10 aF/μm (for a 20 nm long channel and 1 V amplified gate bias, V_{G2}). The 12.5× voltage transformer allows us to reduce the voltage to 80 mV, giving a reasonable velocity saturated conductance of 750 μS/μm. The conductance of the two layer transformer from Figure 2 is given in Figure 6b. As the conductance and induced charge density increase, the voltage amplification decreases. At a charge density of $10^{11}/cm^2$, the voltage amplification is 6.4× but the conductance is reduced to 130 μS/μm.

The efficiency of the transformer can be found by comparing the input energy to the energy required to charge the channel. Input energy is simply given by the induced charges Q_1 (eq 10) and Q_2 (eq 11) times the applied voltage V_G: $E_{in} = (Q_1 + Q_2) \times V_G$. The charge and therefore energy is dominated by the capacitance of the top piezoelectric PMN−PT. Q_2 is the induced charge density in the channel that is plotted in Figure 5. The energy required to charge the channel is given by $E_{out} = Q_2 \times V_{G2}$. Thus, the transformer efficiency is given by

$$\eta_{transformer} = \frac{E_{out}}{E_{in}} = \frac{Q_2 V_{G2}}{(Q_1 + Q_2)V_G} \tag{19}$$

This is plotted in Figure 6c. As we can see the transformer efficiency is only around 1% at best. This is because the piezoelectrics themselves have some loss and mechanical energy is lost in the SiN frame, Si substrate, and metal contacts. Nevertheless, the efficiency does not tell the whole story as the transformer operates at a lower charge density than a conventional transistor. For instance, we can compare the energy required to charge a 1 nm gate oxide to the energy required to charge the transformer: $\eta = (C_{OX} \times V_{G2}^2)/((Q_1 + Q_2) \times V_G)$. For an induced charge density of $10^{11}/cm^2$ in the transformer this results in a reasonable efficiency of 55%. At $10^{12}/cm^2$, the efficiency drops to 7%. For periodic clocking circuits it might also be possible to design the transformer to operate at its resonant frequency where the efficiency will be much higher. In general, the transformer will be extremely useful for longer wires where the capacitance can be fF's to pF's and the energy consumed by the transformer is negligible compared to the wires.

Next, we estimate the mechanical speed. Because this device involves physical motion, the speed will be limited by the rate at which the piezoelectrics can expand/contract. We estimate this by dividing the speed of sound (~3000 m/s) by the height of the piezoelectric stack (200 nm) to get a maximum speed of 15 GHz.

The transistor will operate in the linear triode regime as the voltage amplification results in a gate voltage that is significantly larger than the applied source drain voltage. In CMOS logic, this will increase the electrical delay by at worst a factor of 2 as the lower current at low voltages will take longer to charge a given load capacitance. Nevertheless, the mechanical delay will limit the speed and so this is not a major consideration. The linear operation will also pose significant challenges for analog designs that require saturation.

The stress and strain can also be estimated to ensure that the device does not mechanically break. Equation 4 can be applied to the bottom piezoelectric in Figure 2 to estimate the stress. The surface charge needs to be around $3 \times 10^{11}/cm^2$ and the electric field will be approximately 1 V/180 nm. Plugging this into eq 4 and the material properties for ZnO gives T = 94 MPa. This can be plugged into eq 3 for the bottom piezoelectric to estimate the strain, $S = -0.06\%$. Because the displacement, ΔL, must be the same in each piezoelectric the strain in the top piezoelectric will just be $S_1 = S_2(L_2/L_1) = 9S_2 = 0.53\%$. Thus, the calculated strain and stress are reasonable and should be safely achievable in the piezoelectric layers.

Many piezoelectrics are either ferroelectric or polar. This means that they have a large spontaneous polarization at zero bias. A spontaneous polarization on the bottom piezoelectric will cause a threshold shift for which needs to be compensated. The spontaneous polarization can also be a significant source of variability. Consequently, nonpolar piezoelectrics such as quartz or nonpolar faces of a polar piezoelectric are preferred for the bottom piezoelectric.

The piezoelectric transformer can be extended to enable alternate logic structures. A potential NAND gate is shown in Figure 7. The piezoelectric stack can be prestrained so that

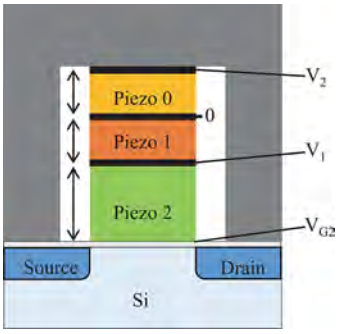

Figure 7. A multilayer piezoelectric transformer can be used to implement more complicated logic functions by applying different voltages to each of the top layers.

both inputs V_1 and V_2 must be high to reduce the strain and turn off the device. Piezo 0 and Piezo 1 simply need to be polled such that they shrink when a voltage is applied.

Overall, we've proposed a new piezoelectric voltage transformer that can be used to significantly reduce the voltage and therefore power of long interconnects in modern electronics. A two-layer piezoelectric stack can increase the voltage by 4.5× and a six-layer stack can amplify the voltage by 12.5×. Increasing the transformer aspect ratio and increasing the number of layers can allow for arbitrarily high voltage amplification. A scaled piezoelectric transformer has a reasonable mechanical speed of 15 GHz and promises to significantly reduce the power required for electronic communications.

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AUTHOR INFORMATION

Corresponding Author

*E-mail: sapan@berkeley.edu.

Notes

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