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Two-dimensional to three-dimensional tunneling in InAs/AlSb/GaSb quantum well heterojunctions

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We examine room temperature band-to-band tunneling in 2D InAs/3D GaSb heterostructures. Specifically, multi-subband, gate-controlled negative differential resistance is observed in InAs/AlSb/GaSb junctions. Due to spatial confinement in the 10 nm-thick InAs layer, tunneling contributions from two distinct subbands are observed as sharp steps in the current-voltage characteristics. It is shown that the relative position of the steps can be controlled via external gate bias. Additionally, the extracted separation in the subband energy agrees well with the calculated values. This is the first demonstration of a gate controlled tunneling diode with multiple subband contributions. © 2013 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4812563]
experiment was carried out at room temperature. The scanning electron microscopy (SEM) images of a fabricated device are shown in Fig. 1(b).

III. RESULTS AND DISCUSSION

Electrical characterization of the devices was carried out at room temperature with an Agilent 4155 semiconductor parameter analyzer (Fig. 2(a)). Figure 2(b) shows measured current, $I$, as a function of the applied tunnel diode voltage, $V_{TD}$, at different gate bias, $V_G$, for a representative device. Interestingly, two distinct NDR peaks in the $I - V_{TD}$ characteristics are visible, exhibiting steepness of $\sim 25 \, \text{mV/decade}$ and $\sim 6 \, \text{mV/decade}$, at $V_G = 0 \, \text{V}$. Analysis shows that these steps correspond to tunneling between the two lowest electron subbands of the InAs QW and the bulk GaSb valence band, illustrating the characteristics of tunneling in a 2-D to 3-D junction. The InAs QW here is defined by the 10 nm thick InAs that is sandwiched between a 10 nm ZrO$_2$ layer on top and $\sim 2$ nm AlSb layer on the bottom, which gives rise to the 2D subband formation. Furthermore, by changing $V_G$, a shift in the voltage positions of the peaks is observed, demonstrating the gate control over the device. By varying the gate bias, the carrier concentration in the InAs can be controlled, moving the position of the Fermi energy level with respect to the subband edges and subsequently changing the $V_{TD}$ at which tunneling occurs. Additionally, in the forward bias region, the diffusion current dominates at high voltages, while in the reverse bias region, the expected tunnel current is observed. Note that given the T-shaped gate geometry used here, the gate fields will be different for the regions directly beneath the foot and the head of the gate. However, the gate-dependence of the static $I-V$ characteristics is dominated by the regions directly under the gate foot given the stronger gate field in those regions.

$I-V_G$ at a fixed $V_{TD}$ was also measured. Figure 2(c) shows an $I-V_G$ curve of the same device when $V_{TD}$ is fixed at $-0.45 \, \text{V}$. Analogous to the $I-V_{TD}$ curves, two steps in the current are observed. These steps are due to the change in the Fermi level with respect to the InAs subband edges, enabling control over the number of subbands contributing to tunnel current at a given junction voltage. The $V_G$ positions at which the current rises agree well with Fig. 2(b).

By taking the derivative of current as a function of the applied voltage (either $V_{TD}$ or $V_G$) in Figs. 2(b) and 2(c),

![FIG. 1. (a) Fabrication process flow. (b) Representative SEM images of a device after fabrication. The magnified image depicts the elevated InAs QW floor, which was designed to isolate the InAs QW from the GaSb substrate.](image1.png)

![FIG. 2. (a) Device schematic showing the configuration of the applied voltages. (b) The measured current as a function of the tunnel diode voltage ($V_{TD}$) when the gate bias $V_G$ is swept from $-0.4 \, \text{V}$ to $1.2 \, \text{V}$ in $0.4 \, \text{V}$ steps. (c) The measured current as a function of the gate bias at a fixed $V_{TD}$ of $-0.45 \, \text{V}$. The device active area is $0.375 \times 24 \, \mu\text{m}^2$.](image2.png)
peak positions (T1 and T2) arising from the two lowest InAs subbands can be obtained from the experimental data. Here, the gate coupling ratio, which is the ratio of the peak position separation $\Delta V_{TD}$ from Fig. 2(b) over the peak position separation $\Delta V_G$ from Fig. 2(c), is approximately 23%. While already high, the gate coupling may be further improved in the future by device epilayer structure design optimization and the use of thinner gate dielectric layers. At $V_G < -0.4$ V, the current becomes gate independent. We attribute this current to the ungated junction regions as marked in Fig. 1(a-iv) beneath the metal contacts. In the future, a more controlled etch of the GaSb/AlSb layers under the metal contact areas is needed to further reduce this ungated tunneling path. Similar multiple peak negative differential resistance behavior was also observed in Refs. 16 and 17; additionally, in this work, the peak position dependence on gate bias is demonstrated for the first time.

In order to gain better insight into the above multi-peak NDR behavior, a cross-sectional band alignment of the device is depicted in Fig. 3(a). The effect of the applied $V_{TD}$ is also qualitatively shown. The 10 nm thick InAs is structurally confined and thus exhibits step-wise 2-D density of states. The energy spacing of the subbands in the InAs layer and the spacing between the NDR peaks can be simulated by using Nextnano simulation tool. In Nextnano, by specifying quantum well region and including 1-band-schroedinger equations, energy band diagram and the subband energy levels can be both simulated. The experimental NDR peak positions (T1, T2) and spacing (T2-T1) obtained from $I-V_{TD}$ curves as a function of the gate bias are plotted in Fig. 3(b). The corrected peak position spacing after taking into account the voltage drop across the estimated series resistance in the device is also shown. From the $I-V_{TD}$ curve, the series resistance of the tunnel diode can be estimated to be $\sim 51 \Omega$ by taking the slope of the curve in the region where diffusion current dominates. By subtracting the voltage drop due to this series resistance from the total applied $V_{TD}$, the peak spacings at each gate bias can be corrected as shown in Fig. 3(b). The corrected experimental and calculated peak spacings match well as shown in Fig. 3(b). This provides strong support that the observed multipeak NDR is due to tunneling between InAs 1st ($E_1$) and 2nd ($E_2$) subbands and the GaSb valence band. Note that the sharpness of the steps is enhanced when series resistance is large. Similar effect of series resistance on I-V characteristics has also been reported in Ref. 18.

To further analyze our results, the analytical model shown below was fit to the experimental data. The total current in the tunnel diode can be expressed in the following equation:

$$I_{\text{diffusion}} = I_0 \times \left( \exp \left( \frac{qV_{TD}}{kT} \right) - 1 \right), \quad (1)$$

where $I_0$ is assumed to be $10^{-11}$ A

$$I_{\text{diode}} = I_{\text{tunnel}} + I_{\text{diffusion}}, \quad (2)$$

with the tunneling component calculated via\textsuperscript{19}

$$I_{\text{tunnel}} = C \int_{E_{\text{in}}}^{E_{\text{out}}} v_i T \frac{\text{DOS}_c \times \text{DOS}_v}{\text{DOS}_c + \text{DOS}_v} \times (F_n - F_p) dE, \quad (3)$$

where $v_i$ represents the injected velocity in the $i$th subband of InAs, $T$ represents the tunneling probability, $\text{DOS}_c$ and $\text{DOS}_v$ stand for the density of states of conduction band of InAs and valence band of GaSb, and $F$ represents the Fermi-Dirac distribution functions. $n$ and $p$ represent electrons and holes, respectively. Additionally, the following assumptions were utilized: (1) the tunneling probability is calculated via the WKB approximation; (2) electron velocity was given by the $z$-component of the momentum in the InAs quantum well ($v_i = \sqrt{2E_i/m}$, where $E_i$ is the energy of the $i$th bound state);
(3) the InAs DOS is 2-D with effective mass $m_e = 0.032m_0$, the GaSb DOS is 3-D with effective mass $m_h = 0.34m_0$. $E_C(\text{InAs}) = 4.92 \text{ eV}$, $E_V(\text{GaSb}) = 4.06 \text{ eV}$, $E_2-E_C = 0.31 \text{ eV}$, $E_2-E_1 = 0.09 \text{ eV}$, $C = 6.7 \times 10^{-32}$ were applied in this calculation.

The joint density of states $DOS_c = DOS_v/(DOS_c + DOS_v)$ was used, as it enables capture of the key features in a 2-D to 3-D tunneling junction. The sharpness of the drop in the experimental behavior is affected by the series resistance.\textsuperscript{18} To account for the series resistance in the simulation, a load line analysis model was used on the calculated $I-V$ curves similar to Ref. \textsuperscript{18}. The calculated $I-V$ is shown in Fig. 4, which is in good agreement with the experimental data, further highlighting the tunneling current in a 2-D to 3-D junction.

\section*{IV. CONCLUSIONS}

In summary, negative differential resistance with multiple peaks from InAs/AlSb/GaSb system is experimentally demonstrated and theoretically analyzed. Critically, the results show that the peak positions can be controlled by an external gate bias demonstrating that this structure is an excellent candidate for future TFET devices. Furthermore, it is shown that the observed voltage spacings between the current peaks fit well with calculated subband spacings of the 2D InAs, and that the observed $I-V$ behavior may be fit with a simple tunnel diode model. Finally, the observation of gate-controlled tunneling between a quantum well and a bulk semiconductors is of great importance, as it allows TFETs with junctions of various dimensionalities to be explored.\textsuperscript{20}

\section*{ACKNOWLEDGMENTS}

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