$In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ Quantum-Well Tunnel-FETs With Tunable Backward Diode Characteristics

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***Abstract*— Vertical quantum-well (QW) tunnel-FETs are fabricated based on an ultrathin $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ staggered gap (type-II) heterostructure lattice matched to InP. Area-dependent QW-to-QW tunneling current is demonstrated. Devices with HfO_2 high-k gate dielectric (EOT $\sim$ 1.3 nm) exhibit minimum subthreshold swings of 140 mV/decade at 300 K, with an ON-current density of 0.5 $\mu A/\mu m^2$ at V_{DD} = 0.5 V. Sharp negative differential resistance is observed in the output characteristics. For the first time, gate-tunable backward diode characteristics are demonstrated in this material system, with peak curvature coefficient of 30 V^{-1} near V_{DS} = 0 V. These results show the potential of vertical TFETs in hybrid IC applications.**

***Index Terms*— Areal tunneling, heterojunction, quantum well (QW), tunable backward diode, tunnel-FET (TFET).**

I. Introduction

THE tunnel-FET (TFET) is of interest as a candidate for future low-power applications due to its potential for steep subthreshold swing (SS) [1]. Several previous studies of TFETs have experimentally demonstrated sub-60-mV/decade SS, albeit only at low currents [2]–[5]. Device structures with enhanced tunneling modulation and tunneling area (also known as line TFETs) have been proposed to enhance the electrostatic control over the tunneling junction [6]–[8]. These designs enable tunneling under the entire gate area and the drive current should be proportional to the gate area, as predicted in [9]. High drive current has been attained in III–V line TFETs [10], [11], which improved the tunneling efficiency using InAs/AlGaSb and InAs/GaSb near broken-gap heterostructures, despite the fact that the drive currents are still perimeter dominated. However, steep SS remains elusive. Devices to date operate by modulating the tunneling barrier width, which is only effective at low drive current. Density-of-state switching has been proposed for steep SS over a much larger range of drive current [12]. This requires two quantum-well (QW) overlapping in the confinement direction, and a step-like turn on is predicted when the sub-bands of the QWs align. Creating such a TFET is one of the goals of this letter.

On the other hand, backward diodes are useful in radio frequency applications for mixing and detection [13]. The type-II heterostructure based III–V backward diodes have demonstrated excellent performance with the highest reported curvature coefficient $\gamma = (d^2I/dV^2)/(dI/dV)$ of 47 V^{-1} [13]. Using different bias conditions than normal TFETs, we show that the diode nature of the heterostructure TFET enables operation as a gate-tunable backward diode.

In this letter, line TFETs based on an ultrathin $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ heterostructure are reported with experimentally observed gate-area-dependent drive current. The type-II band alignment with small effective mass enables strong quantum confinement in the two QWs. The diode-mode operation of the device is also demonstrated for the first time with gate-tunable backward diode characteristics, and peak γ = 30 V^{-1} near V_{DS} = 0 V is obtained.

II. Device Structure and Fabrication

The ternary compound InGaAs/GaAsSb system is attractive because of its direct bandgap and tunable band alignment [14]. Since the device layers are designed ultrathin to form QWs, it is essential to have good epitaxial quality, which can be provided by the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ lattice-matched material system on InP, as a demonstration. Further variations on the material composition can be investigated in the future to balance the tradeoff between growth quality and the effective bandgap at the heterointerface.

The $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical TFET structure and corresponding material layers are shown in Fig. 1(a). The self-aligned source recess and air-bridge structure are used in the device to eliminate parasitic tunneling paths in the ungated regions. The epitaxial layers used for device fabrication are grown on semi-insulating InP by molecular beam epitaxy. The device layers consist of 18-nm p+-$GaAs_{0.5}Sb_{0.5}$ (Be $\sim 10^{19}$ cm^{-3}) and 15-nm n-$In_{0.53}Ga_{0.47}As$ (Si $\sim 5 \times 10^{17}$ cm^{-3}). The ON-state band diagram of the device is simulated self-consistently using nextnano3 [15] [Fig. 1(b)]. The first sub-bands of both materials are marked as well.

The device fabrication process flow is shown in Fig. 1(c). All the patterning is done with e-beam lithography. ALD HfO_2 is deposited at 250 °C as a gate dielectric, as described in [16]. A TMAH-based highly selective wet etch is used to remove the

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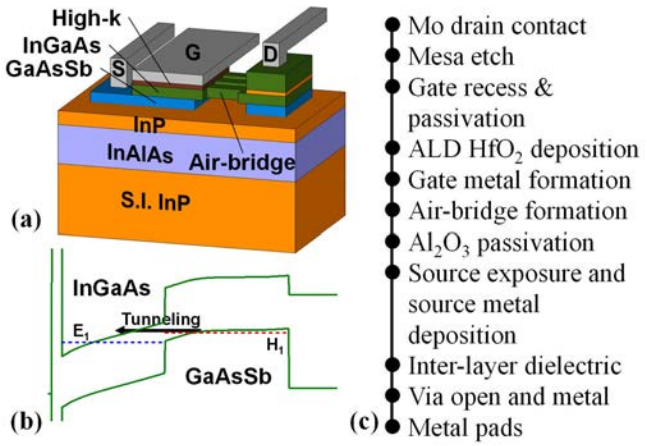

Fig. 1. (a) 3-D schematic view, (b) corresponding simulated ON state band diagram with first subbands of InGaAs and GaAsSb, and (c) process flow of the type-II $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical TFET.

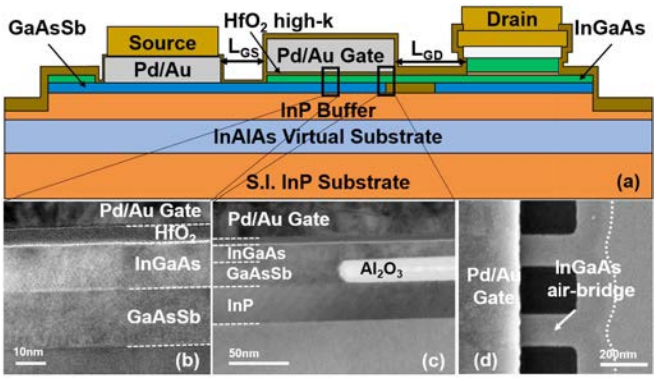

Fig. 2. (a) Schematic cross-sectional view of the fabricated $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ vertical TFET. (b) HR-XTEM of the tunneling junction and gate-stack in the gated region. (c) XTEM at the edge of the InGaAs air bridge. (d) Top-view SEM image of the InGaAs air bridge after suspension. The air bridge is self-aligned to the gate, and the outline of the etched GaAsSb is highlighted.

GaAsSb to suspend the InGaAs air bridge, followed by ALD Al_2O_3 deposition for passivation. The n-InGaAs is recessed self-aligned to the gate with 1:2 H_2O_2:citric acid for the source contact. A schematic cross-sectional view of the device is shown in Fig. 2(a), where the distance between the gate and S/D contacts is $L_{GS} = L_{GD} = 1$ μm. Fig. 2(b)-(d) show the XTEM and SEM images of the fabricated device with the air bridge self-aligned to the gate. From Fig. 2(b), 5.3 nm of HfO_2 gate dielectric (EOT $\sim$ 1.3 nm from dielectric constant calibration [16]) is measured.

III. Results and Discussion

The transfer and output characteristics of the TFET with gate dimensions of 3.8 $\times$ 22 μm^2 are shown in Fig. 3(a) and (b). The minimum (point) SS at low V_{DS} is 140 mV/decade and the effective SS for I_{DS} from 20 nA to 2 μA is 220 mV/decade. The output characteristics show good saturation for positive V_{DS}, and V_{GS}-dependent negative differential resistance is clearly seen in the negative V_{DS} region. This is solid evidence of the tunneling nature of

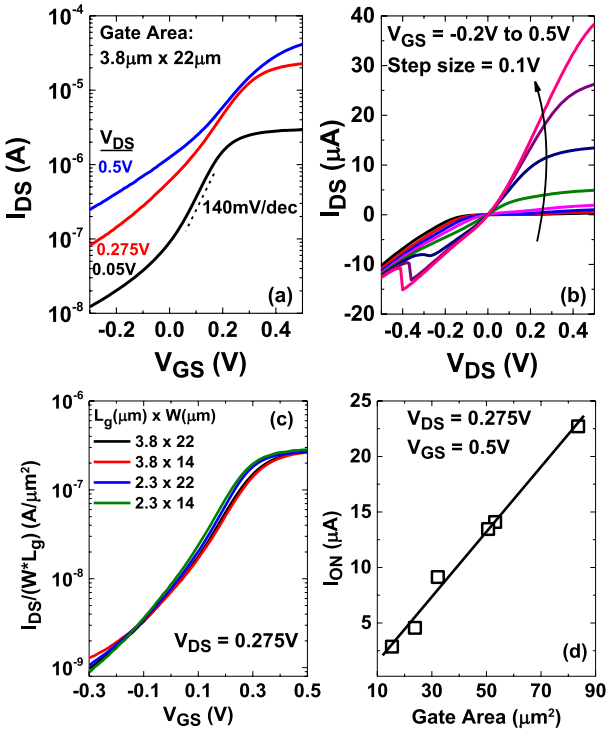

Fig. 3. (a) Transfer and (b) output characteristics of the fabricated TFET with gate dimension of 3.8 $\times$ 22 μm^2. (c) I_{DS}–V_{GS} curves at $V_{DS} = 0.275$ V for four devices with different gate dimensions normalized to the gate area. (d) Drive current at $V_{GS} = 0.5$ V versus gate area shows areal tunneling current in the vertical TFET.

the device operation. Fig. 3(c) plots the I_{DS}–V_{GS} curves at $V_{DS} = 0.275$ V for four different device sizes normalized to gate area, showing appropriate scaling behavior with gate area. I_{DS} is also plotted at $V_{GS} = 0.5$ V over a wide range of gate areas in Fig. 3(d) to confirm the areal tunneling behavior.

Two factors have been identified that impact the SS: high OFF current and high D_{it} in the InGaAs conduction band at the HfO_2/InGaAs interface. The OFF current may originate from the leakage through the 30-nm-thick InP buffer layer, which can be eliminated by undercutting the InP layer under the drain contact. Multifrequency split C–V characteristics are measured for on-chip MOSFET-like test structures with InGaAs channels (Fig. 4). The two-FET method with $L_{g1} = 16.8$ μm and $L_{g2} = 10.4$ μm is adopted to eliminate the parasitic capacitance. A capacitance equivalent thickness of $\sim$2 nm is obtained at $V_G - V_{FB} = 0.5$ V and minimum D_{it} of 2×10^{12} $cm^{-2}eV^{-1}$ is extracted near the midgap ($V_{GS} \sim$ 0.2 V) using the high–low method [17]. The frequency dispersion at high V_{GS} is mainly due to D_{it} near and in the InGaAs conduction band. This is where the Fermi level spans in the subthreshold regime, resulting in relatively large SS, which can be improved by reducing D_{it} via further optimization of the gate-stack.

The total extrinsic resistance, R_{ext}, is estimated to be 930 Ω for a 3.8 $\times$ 22 μm^2 device from contact and sheet resistance measurements on the transmission-line model test structures. R_{ext} is negligible compared with the total ON-state resistance of 1.75×10^4 Ω. This is probably due to the strong quantization in the ultrathin InGaAs layer, which is expected

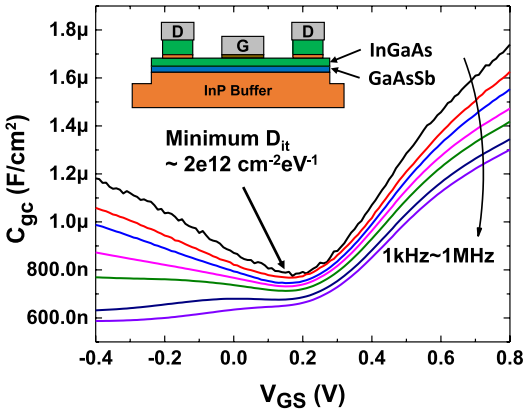

Fig. 4. Multifrequency split C–V characteristics of the MOSFET-like test structure (inset). Two-FET method is applied with extracted minimum mid-gap D_{it} of 2×10^{12} cm^{-2}eV^{-1}. The frequency dispersion at high V_{GS} is mainly due to high D_{it} ($>10^{13}$ cm^{-2}eV^{-1}) near and in the conduction band.

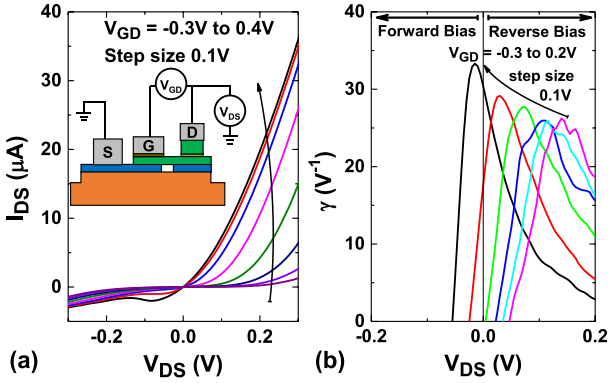

Fig. 5. (a) I_{DS}–V_{DS} characteristics and of the device under fixed V_{GD} bias demonstrate backward diode behavior with (b) tunable curvature coefficient (γ) at different V_{GD}. An excellent peak γ of 30 V^{-1} is achieved.

to increase the tunneling barrier by ~150 meV relative to the bulk E_{g-eff} of 270 meV [18]. Therefore, E_{g-eff} needs to be reduced in the future by optimizing the alloy composition to increase current drive.

Diode-mode measurements were performed with fixed V_{GD} bias (Fig. 5). The gated-diode nature of the TFET exhibits tunable backward diode behavior with varied V_{GD}. The curvature coefficients, γ, corresponding to $V_{GD} = -0.3$ to 0.2 V are plotted with varying V_{DS} in Fig. 5(b). The zero-bias γ is measured as high as 30 V^{-1} with appropriate V_{GD}. The gate bias may be used to optimize for either minimum noise (zero V_{GD}) or high sensitivity (appropriate V_{GD}) with a single device. This demonstration exhibits the potential of the vertical TFET for future hybrid integrated circuit applications.

IV. Conclusion

$In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ QW vertical TFETs are fabricated with self-aligned G/S-recess and G/D-air-bridge structures, demonstrating tunneling current that scales with gate area. Devices exhibit minimum SS of 140 mV/decade at 300 K. Completely isolated S/D and reduced D_{it} are required to significantly improve device performance. Diode-mode operation shows excellent nonlinearity at zero bias with gate tuning of the characteristics, showing the versatility of the vertical TFET in IC applications.

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