Impact of Quantization Energy and Gate Leakage in Bilayer Tunneling Transistors

James T. Teherani, Sapan Agarwal, Eli Yablonovitch, Judy L. Hoyt, and Dimitri A. Antoniadis

***Abstract*—The effect of quantum mechanical confinement in recently proposed thin-body double-gate electron–hole bilayer tunneling transistors is examined. In such devices, a vertical electric field, which is produced by oppositely biased double gates, induces vertical band-to-band tunneling across the intrinsic semiconductor channel. It is found that reducing body thickness in order to increase tunneling probability, i.e., source–drain current drive, considerably increases confinement energy, requiring a large gate and semiconductor electric field, and therefore voltage, to reach electron and hole eigenstate alignment. Furthermore, large electric fields across the gate dielectrics are expected to cause substantial gate leakage current. Design limits based on this analysis are discussed.**

***Index Terms*—Electron–hole bilayer, leakage currents, quantization, tunneling field-effect transistor (TFET), tunneling transistors, tunneling.**

I. Introduction

TUNNELING field-effect transistors (TFETs) have attracted much attention because of their potential to overcome the subthreshold swing (SS) thermal limit of 60 mV/dec at room temperature. Many different TFET structures have been suggested to minimize SS and maximize on-current, and a review is provided in [1]. Of these structures, the electron–hole bilayer TFET has been recently proposed as a novel design that can obtain low SS from an electrostatically doped p-i-n homojunction. Lattanzio *et al.* simulated this structure for both Si and Ge and reported impressive results [2], [3]; however, these papers did not elaborate on the impact of quantization. This letter provides an in-depth analysis of vertical quantization in the channel of electron–hole bilayer TFETs and suggests fundamental limits to the scalability of the semiconductor body thickness. The evaluation is performed for homojunction structures of Si, Ge, and InAs. The results highlight the tradeoffs between tunneling distance, quantization energy, and gate leakage current.

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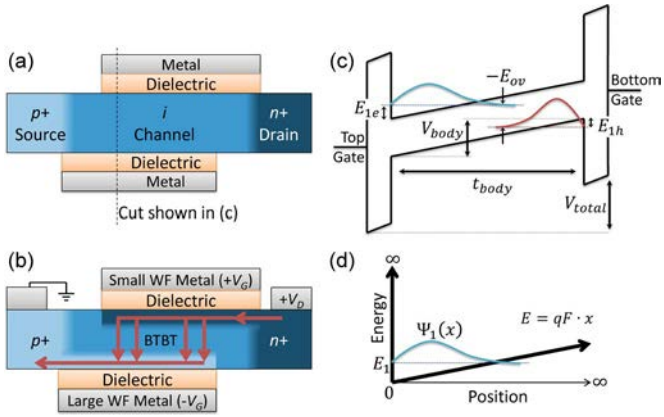

Fig. 1. (a) Electron–hole bilayer TFET structure. (b) Structure with applied bias and current flow (arrows). BTBT occurs between electron- and hole-rich layers induced by oppositely biased top and bottom gates. (c) Vertical band diagram of (a) before eigenstate alignment. BTBT results when the first electron eigenstate (blue) overlaps in energy with the first hole eigenstate (red). (d) Analytically solved potential barrier problem akin to (c).

II. Device Structure

An electron–hole bilayer TFET consists of a p^+ source, an n^+ drain, and a nominally undoped channel bound by offset top and bottom gates with equal dielectric thickness shown in Fig. 1(a). The gates are oppositely biased to create an electron (hole) gas along the top (bottom) gate extending to the n^+ drain (p^+ source). The device turns on when sufficient potential is applied between the gates to enable vertical band-to-band tunneling (BTBT) across the channel [4], as shown in Fig. 1(b). To facilitate small *applied* gate voltages, it was suggested [2] that all or part of the voltage be absorbed by the work-function (WF) difference of the two gate materials; however, common metals only span $\sim$1 eV in WF energy, and voltage differences far beyond this would require new circuit architectures accommodating uneven gate and drain biases. It is therefore important to assess the range of required voltages and the impact of this voltage range on device operation.

In this letter, we investigate the body voltage at the onset of conduction of a bilayer TFET, which is expected to occur when the first electron and hole eigenstates align in energy. We analytically determine the body voltage in order to deduce the total voltage, the gate efficiency, and the expected gate leakage at the onset of eigenstate alignment at $V_{ds} = 0$ V.

III. Theory

Fig. 1(c) shows a vertical band diagram of the channel with oppositely biased top and bottom gates. Assuming an *ideal*

triangular potential [shown in Fig. 1(d)] for holes and electrons, the quantization energy of the nth level is

$$E_n \approx \left(\frac{3\pi}{2}\left(n-\frac{1}{4}\right)\right)^{2/3}\left(\frac{q^2F^2\hbar^2}{2m^*}\right)^{1/3} \quad (1)$$

where q is the elementary charge, F is the semiconductor electric field, $\hbar$ is the reduced Planck's constant, m^* is the effective mass of either holes or electrons in the direction of quantization, and $n = 1, 2, 3, \ldots$ [5]. We use (1) to calculate the required potential across the semiconductor, i.e., $V_{\rm body}$, and the entire structure, i.e., $V_{\rm total}$, [shown in Fig. 1(c)] at eigenstate alignment in Section IV.

Equation (1) assumes an infinite barrier at zero and a triangular potential that goes as $qF \cdot x$ from zero to infinity, as shown in Fig. 1(d). The equation assumes a constant vertical electric field throughout the semiconductor body, yet any charge distribution in the body will create a nonuniform field. Indeed, appreciable charge distributions do accumulate near the top and bottom gates at eigenstate alignment, i.e., at the expected sharp onset of device conduction, which cause a larger electric field near the semiconductor surface than by simply assuming $F = V_{\rm body}/t_{\rm body}$. We compare the analytical approximation with the numerical simulations of the actual structure in Section IV and find that the analytical solution adequately and succinctly captures the physics of the problem and provides insight into the parameters that affect quantization.

IV. Analysis

Using (1), we determine the energy overlap $(E_{\rm ov})$ between the first electron and hole eigenstates as a function of the vertical potential difference across the channel of the semiconductor body $(V_{\rm body} = F \cdot t_{\rm body})$, i.e.,

$$E_{\rm ov} = qV_{\rm body} - (E_G + E_{1e} + E_{1h}) \quad (2a)$$

$$= qV_{\rm body} - E_G - \left(\left(\frac{9\pi}{8}\right)^{2/3}\left(\frac{\hbar^2}{2}\right)^{1/3}\left(\frac{qV_{\rm body}}{t_{\rm body}}\right)^{2/3} \times \left[(m_e^*)^{-1/3} + (m_h^*)^{-1/3}\right]\right). \quad (2b)$$

E_G is the bulk semiconductor band gap, $t_{\rm body}$ is the semiconductor thickness, and m_e^* and m_h^* are electron and hole effective masses along the quantization direction, which is assumed to be [100] in this letter. The first electron and hole eigenstates are aligned in energy when $E_{\rm ov} = 0$, which we call *eigenstate alignment*.

We solve (2) at eigenstate alignment to find $V_{\rm body}$ as a function of $t_{\rm body}$ for Si, Ge, and InAs, as shown in Fig. 2. A runaway condition occurs at small $t_{\rm body}$ when the confinement energy becomes exceedingly large.

We self-consistently solve the Schrödinger–Poisson equations with *nextnano3* [6] using the effective mass approximation for the structure shown in Fig. 1(c). We plot the numerical results for the InAs body with infinite and finite dielectric-semiconductor energy barriers in Fig. 2. The HfO_2 dielectric parameters from [7] were used in the numerical simulation

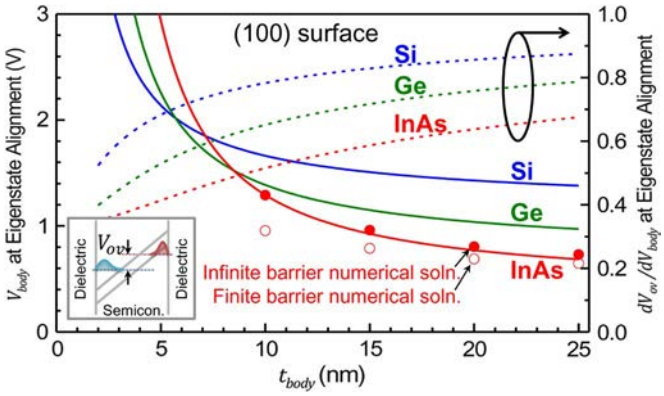

Fig. 2. (Solid lines) Body voltage and (dashed lines) body-voltage efficiency at eigenstate alignment $(V_{\rm ov} = 0)$ as a function of the body thickness analytically calculated for an infinite triangular well. Symbols represent numerical calculations of $V_{\rm body}$ at eigenstate alignment for the InAs structure shown in Fig. 1(c). At small body thicknesses, $V_{\rm body}$ surges because of rapidly growing quantization energy. The inset depicts the vertical band diagram of the channel and highlights $V_{\rm ov}$. The material parameters used in the calculation are provided in Table I.

of the finite barrier, except that the conduction and valence band barriers for HfO_2/InAs were set to 2.36 and 3.11 eV, respectively, due to the electron affinity difference of InAs and Si. As expected, the analytical triangular-well solution of (2) compares very well with the numerical solution for infinite barriers, but the finite barrier solution yields a smaller $V_{\rm body}$ at eigenstate alignment due to wave function penetration into the dielectric resulting in less quantization. Although a finite barrier reduces the voltage required for eigenstate alignment, wave function penetration into the dielectric results in increased gate leakage current.

Of the chosen materials, InAs exhibits the widest variation between finite and infinite barrier solutions due to its small conduction band mass. InAs Γ-band quantization rapidly increases for a body thickness less than 10 nm, which may lead to electron population of the L- and X-bands at eigenstate alignment. Nonparabolicity of the InAs Γ-band will increase the quantization mass [8], but doubling m_e^* only reduces the quantization energy by 20% due to the $-1/3$ power-law dependence on mass. Therefore, we do not expect nonparabolicity to substantially affect our conclusions.

The relation $dV_{\rm ov}/dV_{\rm body}$ (calculated from the derivative of (2b) where $qV_{\rm ov} = E_{\rm ov}$) is plotted in Fig. 2 and represents the incremental body-voltage efficiency at bringing the electron and hole eigenstates into alignment. Quantization limits the efficiency to less than 1. *Increasing the body voltage, in order to increase eigenstate overlap, increases the electric field, which in turn increases quantization.* The corresponding incremental gate-voltage efficiency is calculated as the product of $dV_{\rm ov}/dV_{\rm body}$ and $dV_{\rm body}/dV_{\rm total}$, which represents the fraction of the total gate-to-gate incremental voltage, i.e., $dV_{\rm total}$, that appears across the semiconductor body. The voltage across the gate dielectrics can be derived from the semiconductor electric field.

Reduced gate efficiency is particularly troubling for materials with small effective mass. For a 20-nm InAs body with a 1-nm equivalent oxide thickness (EOT), the total gate-to-gate voltage efficiency at eigenstate alignment is given by $dV_{\rm ov}/dV_{\rm total} =$

TABLE I
SEMICONDUCTOR MATERIAL PROPERTIES USED IN CALCULATIONS

	Si	Ge	InAs
E_G (eV)	1.12	0.66	0.35
m_e^* (m_o)	$m_l = 0.92$	$\frac{3m_l m_t}{m_t + 2m_l} = 0.12$	$m_\Gamma = 0.026$
m_h^* (m_o)	$m_{hh} = 0.49$	$m_{hh} = 0.33$	$m_{hh} = 0.41$
ϵ_r	11.7	16.2	15.15

The effective mass is calculated along [100] for the lowest energy (heaviest) eigenstate. Subscripts l, t, Γ, and hh denote longitudinal, transverse, gamma-point, and heavy-hole masses, respectively. The relative permittivity is given by ϵ_r.

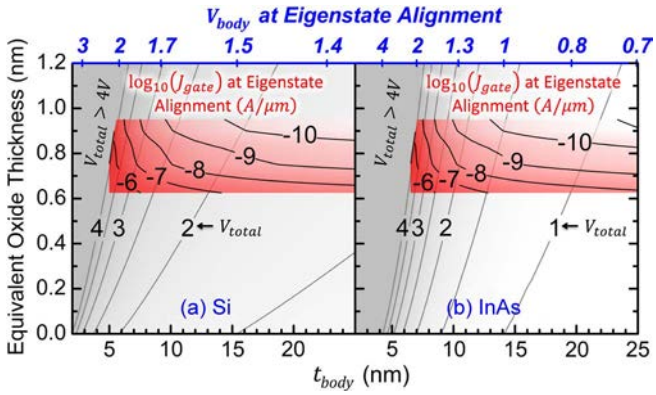

Fig. 3. Gate leakage current (inset, black contours with red shading) and $V_{\rm total}$ (gray contours) at eigenstate alignment as a function of EOT and body thickness for (a) Si and (b) InAs. The leakage current is derived from high-κ on Si experimental data [7], and the top axis ($V_{\rm body}$) is derived from Fig. 2. The gate leakage (in amperes per micrometer of width) is calculated for a 50-nm gate length but can be linearly scaled with the gate length. Decreasing $t_{\rm body}$ increases $V_{\rm body}$ (due to quantization) and thus increases the electric field and gate leakage current. While InAs generally requires less voltage for eigenstate alignment compared to Si, the 30% larger relative permittivity of InAs causes a higher dielectric field resulting in similar gate leakage current contours.

$dV_{\rm ov}/dV_{\rm body} \cdot dV_{\rm body}/dV_{\rm total} = 0.63 \cdot 0.72 = 0.45$. (Relative permittivity values used in the calculation are provided in Table I.) The total gate efficiency declines to 0.29 when the body thickness is decreased to 10 nm. Therefore, in order to realize a gate-voltage SS $(dV_{\rm total}/d\log(I))$ of less than 60 mV/dec in a 10-nm InAs structure, the internal SS $(dV_{\rm ov}/d\log(I))$ must be lower than 18 mV/dec.

Large electric fields exist in the gate dielectric at eigenstate alignment, which can cause significant gate tunneling current that would increase OFF-state current and inhibit the small SS seen at low currents in simulations [2], [3]. Increasing the body thickness decreases the electric field, but at the expense of the ON-state current, since tunneling probability exponentially depends on tunneling distance.

To estimate gate leakage, we use experimental data for scaled HfO_2/SiO_2 compound dielectrics on Si [7]. Results are shown for Si [see Fig. 3(a)] and InAs [see Fig. 3(b)] versus body thickness and EOT at eigenstate alignment. To produce the plot, we calculate the dielectric field of the experimental n-channel FETs of [7] and map the field to the corresponding body thickness of the bilayer TFET structure at eigenstate alignment. From the experimental $J_{\rm gate}$ versus $V_{\rm gate}$ plots, we then interpolate gate leakage current at eigenstate alignment as a function of $t_{\rm body}$ for EOT values between 0.61 and 0.97 nm. We perform the gate leakage analysis for InAs [see Fig. 3(b)] using the same experimental data as for Si, assuming that the compound HfO_2/SiO_2 dielectric on Si represents the best expected performance for dielectrics on other material systems. Remarkably, the gate leakage contours of Fig. 3(a) and (b) are quite similar. Although the net voltage required for eigenstate alignment is lower for InAs compared to Si for large body thicknesses, the 30% larger permittivity of InAs causes a higher electric field in the dielectric, and these effects compensate each other.

Fig. 3 represents the design tradeoff between gate leakage, total voltage, and body thickness. Increasing the dielectric thickness exponentially decreases gate leakage but increases $V_{\rm total}$ for a given $V_{\rm body}$, which reduces gate efficiency. Based on this analysis, we believe that an InAs electron–hole bilayer TFET with a body thickness of ~15 nm and an EOT of ~0.9 nm may represent a reasonable balance between OFF- and ON-state performance: smaller body thickness and EOT result in objectionably high leakage current; larger body thickness would greatly reduce tunneling probability and therefore ON-state current; and thicker EOT requires larger total voltages.

V. CONCLUSION

We have shown the adverse effect of increasing quantization energy with decreasing body thickness on the gate efficiency of proposed electron–hole bilayer TFETs. The gate leakage tunneling current is also shown to dramatically increase with decreased body thickness at small EOT, limiting the minimum body thickness that can be used for such devices in the quest for increased source–drain current. The SS of experimental devices is expected to be significantly degraded compared to reported ideal simulations due to gate leakage caused by large electric fields at eigenstate alignment.

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