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Interface quality of InAs-on-insulator (XOI) field-effect transistors (FETs) with a ZrO_2 gate dielectric is examined as a function of various chemical treatments. With a forming gas anneal, InAs XOI FETs exhibit a low subthreshold swing of ~72 mV/dec with an interface trap density of $\sim 1.5 \times 10^{12}$ states/cm^2 eV—both of which are comparable to the best reported epitaxially grown III-V devices on III-V substrates. Importantly, the results indicate that the surface properties of InAs are preserved during the layer transfer process, thereby, enabling the realization of high performance III-V FETs on Si substrates using the XOI configuration. © *2013 AIP Publishing LLC* [http://dx.doi.org/10.1063/1.4802779]

III-V compound semiconductors present a promising class of materials for future low-power and high-speed electronics due to their low carrier effective mass and high mobilities.[1–3] Two promising approaches have been explored for integration of III-V semiconductors on Si wafers: (i) direct epitaxial growth on Si using buffer layers[4] and (ii) selective layer transfer from an epitaxial growth substrate onto a Si/SiO_2 substrate.[5,6] The latter approach results in III-V on insulator (XOI) structures and presents the advantage of removing lattice mismatch constraints associated with the growth substrate. To date, high electron mobility InAs and InAsSb field-effect transistors (FETs);[7,8] high hole mobility InGaSb FETs;[9] and III-V complementary-FETs[10] have been demonstrated on Si substrates by using the XOI scheme. Despite these recent advancements, the dielectric and III-V interface quality is still largely unknown, and it remains a question whether similar interface qualities to direct epitaxial growth processes[11] can be obtained in XOI devices. Here, we focus on answering this question for InAs XOI FETs with ZrO_2 gate dielectrics by examining the effect of various chemical treatments on the interface properties. Specifically, the subthreshold swing (SS) and interface trap density (D_{it}) are systematically characterized by current-voltage (I-V_G), capacitance-voltage (C-V_G), and conductance-frequency (G/ω-f) measurements. The long-channel devices treated under the optimal condition exhibit a SS as low as ~72 mV/decade and D_{it} of $\sim 1.5 \times 10^{12}$ states/cm^{-2} eV, both of which are comparable to the best values reported for the epi-grown and/or bulk III-V devices.[11] The results demonstrate that high quality interfaces can be obtained in layer transferred InAs XOI structures, which is of fundamental importance for the practice use of this technology for future scaled transistors.

Ultrathin (~10 nm-thick) InAs films grown by a molecular beam epitaxy (MBE) on GaSb substrates with an AlGaSb sacrificial layer were transferred onto thermally grown SiO_2 (1.6 μm thick) on p$^+$Si substrates using a previously described process.[5] Before transferring the InAs film to the Si/SiO_2 substrate, the back surface of the lifted-off InAs was cleaned with 1% HF in water to remove AlGaSb residues. After transferring the film onto the Si/SiO_2 substrate, the top surface of the InAs was cleaned with hot acetone at ~60 °C to remove organic residues. Due to InAs native oxide formation during the fabrication process, the final thickness of InAs is ~8 nm as confirmed by transmission electron microscopy. Ni source (S) and drain (D) electrodes were patterned, followed by contact annealing at 300 °C for 1 min in N_2 to obtain low contact resistances (~200-300 Ω μm) as previously reported.[12] A 10 nm-thick ZrO_2 film was deposited as the gate dielectric by atomic layer deposition (ALD) at 130 °C using tetrakis (ethylmethylamido) zirconium and water precursors. After ZrO_2 deposition, various thermal annealing and plasma treatments were performed, followed by an examination of the effect on the interface quality between InAs and ZrO_2 (i.e., top interface), InAs and SiO_2 (i.e., bottom interface), and the trap density in ZrO_2. The post-ALD thermal annealing was performed in either 5% H_2 in N_2 or 200 ppm H_2S in N_2 for 30 min at 170 °C under atmospheric pressure. This temperature was chosen since thermal annealing at >170 °C resulted in noticeable degradation of InAs device properties (including SS) for both gas environments. No change in the contact resistance is observed after this step. In addition, samples exposed to CF_4/O_2 plasma (120 sccm CF_4, 10 sccm O_2, 30 W, 3 min)[11] after ZrO_2 deposition were prepared and characterized. In addition to the above treatments, InAs XOI FETs with thermally grown oxide using 2% O_2 in Ar at 350 °C for 1 min before ZrO_2 deposition were prepared. Prior to the thermal oxidation, InAs native oxide was etched by 3% NH_4OH in water. Our previous studies[5] have shown the thermal oxide of InAs to improve the SS of XOI FETs as compared to untreated samples and those with etched interfacial native oxide.

After the various surface/interface treatments, Ni/Au gate (G) electrodes were patterned and ZrO_2 over the contact

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bonding pads was etched. Figure 1 shows a cross-sectional schematic of an InAs XOI FET on a Si substrate and a top-view scanning electron microscopy (SEM) image of a representative device used in this study, depicting multiple InAs ribbons bridging the S/D contacts. XOI FETs with overlapped (i.e., $L_{SD} = L_G$, where L_{SD} is the S/D spacing and L_G is the gate length) and underlapped (i.e., $L_G < L_{SD}$) gate structures were prepared. Current-gate voltage (I_{DS}-V_{GS}), capacitance-voltage (C-V_{GS}), and conductance-frequency (G/ω-f) measurements were subsequently performed for each sample. Specifically, the underlapped gate structure was necessary to reduce G-S/D parasitic capacitances for C-V and G/ω-f measurements. Note that for all devices, the ZrO_2 gate dielectric leakage currents were below the measurement set-up noise level for the applied voltage range of −2 V to 2 V.

To examine the effect of various treatments on the interface properties, SS of XOI FETs was first systematically explored at room temperature. Figure 2(a) shows representative I_{DS}-V_{GS} characteristics of overlapped gate InAs XOI FETs at $V_{DS} = 500$ mV fabricated with and without H_2/N_2 forming gas anneal (FGA) after ALD of ZrO_2 gate dielectric. Clearly, a drastic improvement in the SS from ∼110 mV/dec to 72 mV/dec is observed by the FGA. Despite the relatively thick gate dielectric used here (∼10 nm thick ZrO_2), SS value of ∼72 mV/decade is among the lowest values reported for III-V transistors to date, regardless of the device configuration. FGA is well known to fix the point defects at Si/SiO_2 interfaces,[13] even at low annealing temperatures.[14] Similarly, we hypothesize that the forming gas anneal used here reduces dangling bonds at $InAs/ZrO_2$ and $InAs/SiO_2$ interfaces in addition to reducing the trap density of ZrO_2 gate dielectric (see supplementary material[15]). In the future, more detailed characterization of the chemical bonding at the interfaces is required to shed light on the observed behavior. It is worth noting that the peak effective mobility after FGA is ∼2300 cm^2/Vs, which is slightly higher than the mobility without annealing (∼2000 cm^2/Vs). This mobility improvement is attributed to the improved interface and reduced D_{it}.

Figure 2(b) shows the average SS and the standard deviation obtained from multiple devices (4–20) for each treatment condition. The average SS of untreated devices is 111 ± 10.6 mV/decade. Overall, for all the treatments presented here, an improvement in SS is observed as compared to the untreated devices. The FGA treatment provides the best average SS of 77 ± 6.4 mV/dec at $V_{DS} = 500$ mV. Thermal oxidation of InAs provides the second best interface with a SS of 92 ± 3.2 mV/dec. The thermal oxide of InAs is denser than the native oxide and under optimal conditions can cause surface restructuring of InAs.[16] Additionally, since sulfur passivation is well known to improve III-V surface/interface properties;[17] here, we explored H_2S gas annealing after ZrO_2 deposition. This treatment results in devices with SS = 95 ± 8.5 mV/dec. It is speculated that H_2S diffuses to the InAs interfaces, causing sulfur passivation of InAs. With CF_4/O_2 plasma treatment at room temperature after ZrO_2 deposition, the SS is ∼96 ± 10.1 mV/dec. This fluorine termination results in similar properties as annealing in H_2S gas.

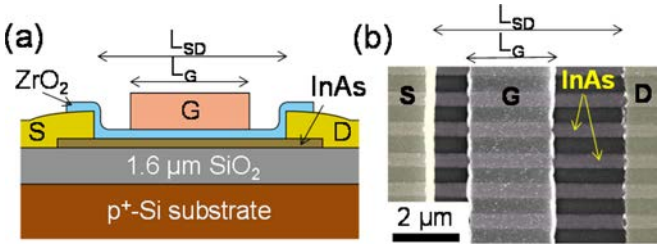

FIG. 1. (a) Cross-sectional schematic of an ultrathin InAs XOI FET with an underlapped gate structure (i.e., $L_G < L_{SD}$). (b) SEM image of a representative device.

Next, we quantify the density of interface traps for InAs XOI FETs as a function of surface/interface treatments using two different techniques. First, D_{it} is analytically extracted from SS using circuit models,[18] and G/ω-f analysis is subsequently used to more directly assess D_{it} (Ref. 19). Figure 2(c) shows D_{it} extracted from SS for different treatments obtained from the following analytical expression:

$$SS = \frac{2.3kT}{q}\left(1 + \frac{C_{it}}{C_{ZrO2}} + \frac{C_{body}}{C_{ZrO2}} - \frac{\frac{C_{body}{}^2}{C_{ZrO2}C_{SiO2}}}{1 + \frac{C_{it}}{C_{SiO2}} + \frac{C_{body}}{C_{SiO2}}}\right),$$

Here $D_{it} = C_{it}/q$, where C_{it} is the interface trap capacitance. $C_{ZrO2} = 1.06 \times 10^{-6}$ F/cm^2 and $C_{SiO2} = 2.16 \times 10^{-9}$ F/cm^2 were measured as the top and bottom oxide capacitances, respectively. InAs capacitance in the depletion regime, $C_{body} = \varepsilon_{InAs}/t_{InAs} \sim 1.67 \times 10^{-6}$ F/cm^2 was calculated using a dielectric constant of $\varepsilon_{InAs} = 15.1$ and body thickness of $t_{InAs} = 8$ nm by the parallel plate capacitance formula. k and q are Boltzmann constant and the electron charge, respectively. The lowest extracted D_{it} value is for samples annealed in forming gas with ∼1.1×10^{12} states/cm^2 eV.

Next, detailed C-V measurements were used to characterize the interface properties. C-V measurements at the sample temperature of 250 K were conducted for XOI FETs with the underlapped gate structure as shown in Fig. 3(a). Note that the C-V measurements had to be performed at low temperatures in order to lower the thermal leakage current and noise in InAs which is a small band gap semiconductor. We focus on samples that were annealed in forming gas after ZrO_2 deposition since they exhibited the lowest SS. To

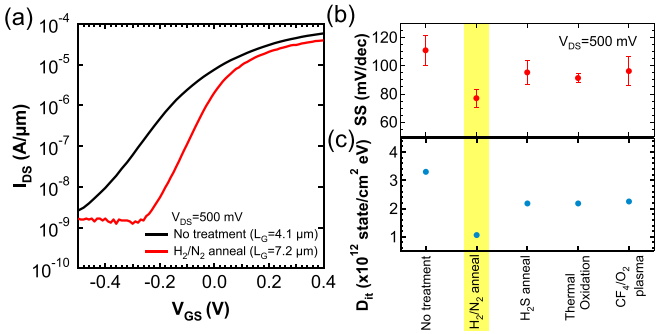

FIG. 2. (a) I_{DS}-V_{GS} characteristics at $V_{DS} = 500$ mV for two representative devices, with (red line; $L_G \sim 7.2$ μm) and without (black line; $L_G \sim 4.1$ μm) forming gas anneal after ALD of ZrO_2 gate dielectric. (b) Average SS and (c) extracted D_{it} of XOI FETs as a function of different surface/interface treatments.

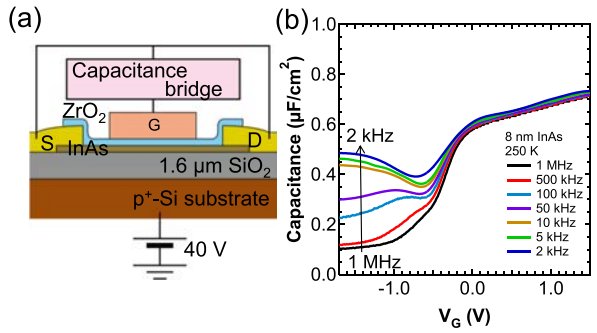

FIG. 3. (a) Device structure and the measurement setup used for *C-V* and *G/ω-f* measurements. (b) *C-V* characteristics at 250 K for an InAs XOI FET fabricated with post-ALD forming gas anneal. The DC amplitude is 50 mV.

reduce parasitic resistances from un-gated InAs channel region, global back-gate bias of 40 V is applied to p^+Si substrate during both *C-V* and *G/ω-f* measurements shown in Figs. 3 and 4 (see supplementary material[15]). Gate capacitance, C_G, was obtained from the accumulation region of *C-V* curves at $V_G = 1.5$ V to be 0.73 μF/cm^2 (Figure 3(b)). C_G consists of stack layers of ZrO_2 dielectric capacitance C_{ZrO2}, InAs charge centroid capacitance $C_{centroid}$, and density of state (DOS) quantum capacitance $C_{Q\text{-}DOS}$ calculated by using the equation previously reported.[9] From our previous study,[12] the electron charge centroid of 8 nm InAs is $t_{centroid} \sim 3.2$ nm from the top surface (at $V_G \sim 1.5$ V), giving $C_{centroid} = \varepsilon_{InAs}/t_{centroid} \sim 4.18 \times 10^{-6}$ F/cm^2. The total capacitance, $1/C_G = 1/C_{ox} + 1/C_{centroid} + 1/C_{Q\text{-}DOS}$ is calculated to be $\sim 6.1 \times 10^{-7}$ F/cm^2, where $C_{ox} = C_{ZrO2} = 1.06 \times 10^{-6}$ F/cm^2 and $C_{Q\text{-}DOS} = 2.17 \times 10^{-6}$ F/cm^2. The calculated C_G value matches with the experimental value (Fig. 3(b)). In the inversion region at $V_G < -0.5$ V, a large frequency dispersion of capacitance is observed. This trend is due to the lack of minority carrier (i.e., holes) response at high frequencies. The observed inversion behavior is similar to a conventional MOS capacitor. Note that unlike conventional MOSFETs, our XOI FETs consist of an n-channel body with ohmic metal S/D contacts to the conduction band

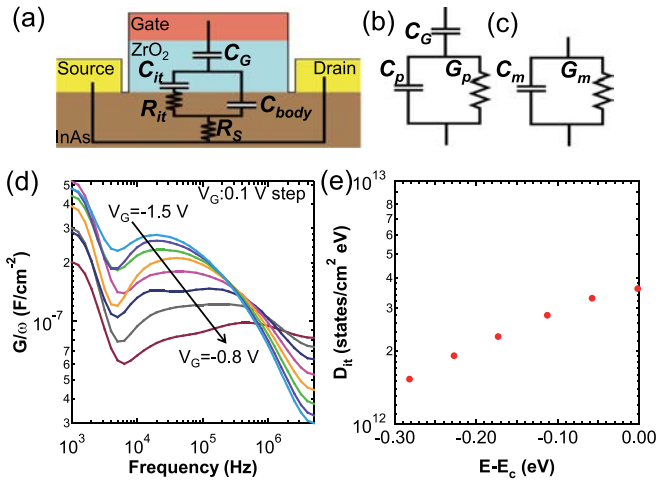

FIG. 4. (a) Equivalent circuit of an InAs XOI device. (b) Simplified circuit layout of (a). (c) Equivalent circuit as measured by the experimental set-up. C_{it} and R_{it} are interface trap capacitance and resistance, respectively. C_p is the equivalent parallel substrate capacitance. (d) G/ω vs. frequency for the same device shown in Fig. 3. (e) D_{it} vs. $E\text{-}E_c$ calculated from the peak of *G/ω-f*.

of InAs. While there are no Schottky barrier heights for electrons, the Schottky barrier height for holes is nearly the full band gap. Thereby, S/D contacts do not provide significant hole injection into the channel. This structural difference causes the observed frequency dispersion in the inversion regime.

To more carefully assess D_{it}, the conductance method,[19] *G/ω-f*, was utilized at 250 K sample temperature (Figs. 4(a)–4(c)). First to extract corrected capacitance C_c and conductance G_c, the series resistance R_s was calculated from the measured capacitance C_{ma} and conductance G_{ma} in the accumulation region by using the following equation:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2}.$$

Based on R_s, the series resistance factor was calculated as $a = G_m\text{-}(G_m{}^2 + \omega^2 C_m{}^2)R_s$, where G_m and C_m are the measured conductance and capacitance. Then G_c and C_c were calculated by

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2}, \quad C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2}.$$

Finally G_p/ω and D_{it} are described by the following equations:

$$\frac{G_p}{\omega} = \frac{\omega G_c C_G^2}{G_c^2 + \omega^2 (C_G - C_c)^2},$$
$$D_{it} = \frac{2.5}{q}\frac{G_p}{\omega},$$

where G_p is the equivalent parallel conductance. Based on these equations, first $G_p/\omega\text{-}f$ as a function of V_G bias from -0.8 V to -1.5 V was plotted in Fig. 4(d), followed by extracting D_{it} using peak G_p/ω values. Figure 4(e) depicts that D_{it} at near mid-gap of InAs is around 1.5×10^{12} states/cm^{-2} eV, consistent with D_{it} extracted from SS (Fig. 2(b)). The extracted D_{it} arises from both top (ZrO_2/InAs) and bottom (SiO_2/InAs) interfaces due to ultrathin body ($\sim$8 nm) of InAs films. To better understand the origin of D_{it} in the XOI material system, back-side interface trap density measurement is also necessary; however, this is not possible with the current device structure and requires future studies.

Our measured D_{it} value of $\sim 1.5 \times 10^{12}$ states/cm^{-2} eV for InAs XOI is comparable to previously reported values for high-κ gate dielectrics on III-V bulk wafers or epitaxial thin films ($D_{it} \sim 2 \times 10^{11}$ to 6×10^{12} states/cm^{-2} eV).[11,20] The work here suggests that the layer transfer process does not degrade the interface properties of InAs. The finding is rather surprising given that both top and bottom surfaces of InAs are exposed to various organic materials and wet etchants during the transfer process. The results suggest that the InAs surface is robust, at least in terms of D_{it}. An explanation for this result may be that the Fermi stabilization energy of InAs lies deep in the conduction band,[21] indicating that native defects create electronic states with average energy in the conduction band, thereby, causing minimal degradation on the FET properties, especially the SS. Although the measured D_{it} values here are low for III-V FET standards, they

are still large compared to Si devices. However, our lowest SS is ~72 mV/decade, which is close to the MOSFET ideal limit, despite the relatively thick gate dielectric used here. In the future, SS can be further improved by using a thinner top gate dielectric.

In summary, through subthreshold swing analyses, and *C-V* and G/ω-*f* measurements, the surface/interface properties of InAs XOI FETs on Si substrates are characterized as a function of various treatments. It is found that FGA after the deposition of the ZrO_2 gate dielectric significantly improves SS of XOI FETs, with the lowest value of ~72 mV/dec, which is close to the theoretical limit of ~60 mV/decade. The D_{it} value was extracted to be $\sim 1.5 \times 10^{12}$ states/cm^{-2} eV near the mid-gap of InAs. These results indicate that the overall quality of InAs surfaces is preserved during the layer transfer process.

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[1]D.-H. Kim and J. A. del Alamo, IEEE Trans. Electron Devices **57**, 1504 (2010).
[2]J. A. del Alamo, Nature (London) **479**, 317 (2011).
[3]M. Heyns and W. Tsai, MRS Bull. **34**, 485 (2009).
[4]M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, UShah, and R. Chau, Tech. Dig. – Int. Electron Devices Meet. **2009**, 319.
[5]H. Ko, K. Takei, R. Kapadia, S. Chuang, H. Fang, P. W. Leu, K. Ganapathi, E. Phis, H. S. Kim, S.-Y. Chen, M. Madsen, A. C. Ford, Y.-L. Chueh, S. Krishna, S. Salahuddin, and A. Javey, Nature (London) **468**, 286 (2010).
[6]M. Yokoyama, T. Yasuda, H. Takagi, N. Miyata, Y. Urabe, H. Ishii, H. Yamada, N. Furuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, Appl. Phys. Lett. **96**, 142106 (2010).
[7]K. Takei, S. Chuang, H. Fang, R. Kapadia, C.-H. Liu, J. Nah, H. S. Kim, E. Plis, S. Krishna, Y.-L. Chueh, and A. Javey, Appl. Phys. Lett. **99**, 103507 (2011).
[8]H. Fang, S. Chuang, K. Takei, H. S. Kim, E. Plis, C.-H. Liu, S. Krishna, Y.-L. Chueh, and A. Javey, IEEE Electron Device Lett. **33**, 504 (2012).
[9]K. Takei, M. Madsen, H. Fang, R. Kapadia, S. Chuang, H. S. Kim, C.-H. Liu, E. Plis, J. Nah, S. Krishna, Y.-L. Chueh, J. Guo, and A. Javey, Nano Lett. **12**, 2060 (2012).
[10]J. Nah, H. Fang, C. Wang, K. Takei, M. H. Lee, E. Plis, S. Krishna, and A. Javey, Nano Lett. **12**, 3592 (2012).
[11]Y.-T. Chen, Y. Wang, F. Xue, F. Zhou, and J. C. Lee, IEEE Trans. Electron Devices **59**, 139 (2012).
[12]K. Takei, H. Fang, S. B. Kumar, R. Kapadia, Q. Gao, M. Madsen, H. S. Kim, C.-H. Liu, Y.-L. Chueh, E. Plis, S. Krishna, H. A. Bechtel, J. Guo, and A. Javey, Nano Lett. **11**, 5008 (2011).
[13]A. Stesmans and V. V. Afanas'ev, Phys. Rev. B **57**, 10030 (1998).
[14]L. Do Thanh and P. Balk, J. Electrochem. Soc. **135**, 1797 (1988).
[15]See supplementary material at http://dx.doi.org/10.1063/1.4802779 for back-gate dependence of the devices and the effect of the forming gas annealing on ZrO_2 film quality.
[16]M. P. J. Punkkinen, P. Laukkanen, J. Lang, M. Kuzmin, M. Tuominen, V. Tuominen, J. Dahl, M. Pessa, M. Guina, K. Kokko, J. Sadowski, B. Johansson, I. J. Vayrynen, and L. Vitos, Phys. Rev. B **83**, 195329 (2011).
[17]E. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, J. Appl. Phys. **109**, 024101 (2011).
[18]J. P. Colinge, D. Flandre, and F. Van de Wiele, Solid-State Electron. **37**, 289 (1994).
[19]E. H. Nicollian and A. Goetzberger, Appl. Phys. Lett. **10**, 60 (1967).
[20]Y. Hwang, V. Chobpattana, J. Y. Zhang, J. M. LeBeau, R. Engel-Herbert, and S. Stemmer, Appl. Phys. Lett. **98**, 142901 (2011).
[21]W. Walukiewicz, Physica B **302–303**, 123 (2001).