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Extraction of Front and Buried Oxide Interface Trap Densities in Fully Depleted Silicon-On-Insulator Metal-Oxide-Semiconductor Field-Effect Transistor

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In this letter, a method is proposed and demonstrated for the first time to characterize and decouple the interface traps of both the front- and back channels of fully-depleted silicon-on-insulator (FD-SOI) metal-oxide-semiconductor field-effect transistor (MOSFET). We report the procedure and the underlying theory that allows the extraction of the energy profiles of the densities of the interface traps (D_{it}).This technique will be very useful for evaluating the interface qualities of future FD-SOI transistors.
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The fully-depleted silicon on insulator (FD-SOI) ultra-thin body UTBSOI MOSFET[1–3] is gaining new attention as an alternative technology to FinFET[4] for ultra-low power and mobile applications because of its outstanding electrostatics, low device variability due to excellent suppression of the short channel effect (SCE) with undoped channel and ultra-thin body.[5,6] UTB structure also offers great compatibility with mainstream planar CMOS for high density integration.[7,8] The performance of these FD-SOI devices are inevitably influenced by the interface traps of buried oxide, in addition to those of the front oxide, as they would degrade the sub-threshold swing, transconductance and device uniformity as the film thicknesses are scaled down.[9] Thus, a simple and reliable approach for D_{it} extraction for both the front and back interfaces simultaneously is highly desired. The most commonly used technique for characterizing the D_{it}, i.e., the charge pumping (CP) method, requires a body contact and/or with additional optical assistance as well as a gated-diode-like device[10–13] to supply the majority carrier, cannot be applied to future FD-SOI technologies as they do not provide body contacts. Nevertheless, conductance method only reflects mixing result of front- and back density of interface state instead of their individual contribution. Besides, conventional capacitance-voltage (C-V) method[14,15] is not appropriate for FD-SOI nowadays because of the large gate leakage current at low frequencies and the high series resistance at high frequencies. Therefore, DC current-voltage based technique is the most attractive. One may apply the sub-threshold technique by accumulating one channel while sweeping the gate bias of the opposite channel to evaluate the D_{it}, and it works well for a relatively thick film.[16] However, for the very thin silicon film thicknesses, it is not possible to accumulate one channel while inverting the opposite channel without using high voltages that would damage the thin gate oxide due to the strong capacitive coupling of the two channels.[17] The back surface potential will always follow the front gate voltage, i.e., the volume inversion occurs. Therefore, a dual-gate (DG) voltage-sweep technique has been utilized to characterize the buried density of interface traps (D_{itB}) for FD-SOI involving sweeping both channels in sub-threshold region, thus an average back channel D_{itB} can be derived by neglecting the D_{itF}.[18] However, ignoring the D_{itF} introduces unknown errors and an average D_{itB} leaves much information unexamined. D_{itB} and D_{itF} should be functions of the surface energy in general.

In this work, we develop an analytical method considering the capacitive coupling between the front and back channels. Using this model the distributions of both front- and back D_{it} (E_t) in the bandgap can be extracted. We successfully demonstrated the new technique on an FD-SOI MOSFET.

Theory

Fig. 1a shows an FD-SOI with very thin silicon thickness T_{Si}. As a consequence of the capacitive coupling between the front and back channels in FD-SOI, the corresponding surface potentials for front and back channel interface ϕ_{sF} and ϕ_{sB} with respect to the applied front and back bias can be expressed as follows[19,20]

$$V_{gF} = V_{fbF} + \phi_{sF}\left(1 + \frac{C_S + C_{itF}}{C_{oxF}}\right) - \phi_{sB}\frac{C_S}{C_{oxF}} - \frac{Q_S}{2C_{oxF}} \quad [1]$$

$$V_{gB} = V_{fbB} + \phi_{sB}\left(1 + \frac{C_S + C_{itB}}{C_{oxB}}\right) - \phi_{sF}\frac{C_S}{C_{oxB}} - \frac{Q_S}{2C_{oxB}} \quad [2]$$

Where $C_{oxF,B}$ and $C_{itF,B} = qD_{itF,B}$ are the oxide and interface trap capacitance of front and buried oxide, respectively, Q_S and $C_S = \frac{\varepsilon_{Si}}{T_{Si}}$

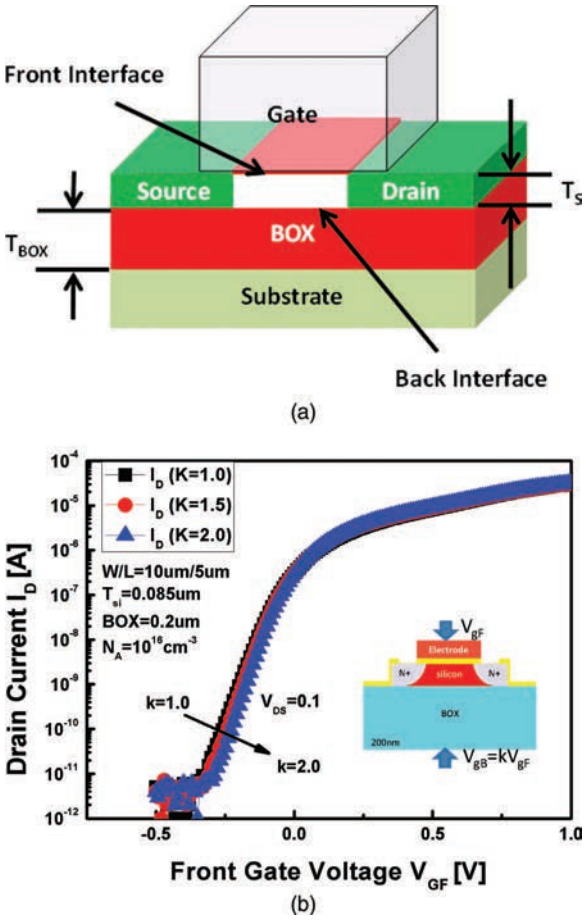

Figure 1. (a) The schematic structure of FD-SOI MOSFET (b) I_D-V_{gF} characteristics for several k values.

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are the depletion charge and depletion capacitance of silicon body, respectively. By solving Eq. 1 and 2 with $V_{gB} = k \cdot V_{gF}$ under DG, the correspond analytical expression ϕ_{sF} and ϕ_{sB} can be derived as function of k and V_{gF}

$$\phi_{sF} = \frac{C_{oxF}}{(C_{oxF} + C_{itF} + C_{\alpha 1})}\left[V_{gF}\left(k\frac{C_{\alpha 2}}{C_{oxF}} + 1 \right) - V_{fbF} + \frac{C_{\alpha 2}}{C_{oxF}}\left(\frac{Q_S}{2C_{oxB}} - V_{fbB} \right) + \frac{Q_S}{2C_{oxF}} \right] \quad [3]$$

$$\phi_{sB} = \frac{C_{oxB}}{(C_{oxB} + C_{itB} + C_{\beta 1})}\left[V_{gF}\left(k + \frac{C_{\beta 2}}{C_{oxF}} \right) - V_{fbB} + \frac{C_{\beta 2}}{C_{oxB}}\left(\frac{Q_S}{2C_{oxF}} - V_{fbF} \right) + \frac{Q_S}{2C_{oxB}} \right] \quad [4]$$

where $C_{\alpha 1} = \frac{C_s(C_{itB}+C_{oxB})}{C_s+C_{itB}+C_{oxB}}$, $C_{\alpha 2} = \frac{C_s C_{oxB}}{C_s+C_{itB}+C_{oxB}}$, $C_{\beta 1} = \frac{C_s(C_{itF}+C_{oxF})}{C_s+C_{itF}+C_{oxF}}$ $C_{\beta 2} = \frac{C_s C_{oxF}}{C_s+C_{itF}+C_{oxF}}$ are the capacitive coupling parameters under DG operation for front and back interface, respectively. Thus, for the corresponding surface potential, the front and back current operated in the sub-threshold regime, the individual current component $I_{Di,j}$, where i and j account for front and back channel current I_{DF} and I_{DB}, respectively.[21]

$$I_{D_{i,j}} = -\frac{W\mu_n}{L}\int_{\phi_{F_{i,j}}}^{\phi_{F_{i,j}}+V_D} Q_{n_{i,j}} d\phi_{F_{i,j}} \quad [5]$$

where the front and back electron density $Q_{n_{i,j}} = -\int_{\phi_{o_{i,j}}}^{\phi_{S_{i,j}}} \frac{q(n-n_0)}{E} d\phi_{i,j}$ can be adequately acquired by numerical evaluating the integral according to,[22,23] W and L are gate width and length, μ_n is the channel mobility, V_D is the applied drain voltage, ϕ_F and ϕ_o are the corresponding Fermi level along the channel and the surface potential at the source end of the channel, n_0 is the electron densities in the film region where $\phi = 0$, and E is the electric field cross the silicon film.

Total drain current I_D is the combination of I_{DF} and I_{DB} when both front and back channel are operated in the weak inversion, i.e., $I_D = I_{DF} + I_{DB}$.

It is recognized the sub-threshold swing (SS) as a significant parameter to evaluate the device performance. To determine the corresponding D_{itF} and $D_{it,B}$ utilizing the capacitive coupling concept experimentally, we took advantage of the front gate sub-threshold (SS_F) swing under DG operation, i.e., the analytical formula SS_F in terms of capacitive coupling factors from Eqs. 3 and 4 and ratio k (defined by $k = V_{gB}/V_{gF}$) can be derived as follows

$$SS_F = \frac{dV_{gF}}{d\log I_D} = \frac{2.3k_BT \cdot I_D}{q}\left(I_{DF} \cdot \frac{C_{oxF}}{(C_{oxF} + C_{itF} + C_{\alpha 1})}\left(k\frac{C_{\alpha 2}}{C_{oxF}} + 1 \right) + I_{DB} \cdot \frac{C_{oxB}}{(C_{oxB} + C_{itB} + C_{\beta 1})}\left(k + \frac{C_{\beta 2}}{C_{oxF}} \right) \right)^{-1} \quad [6]$$

The above formulations thus establish a reliable method with considering a capacitive coupling effect between the front and back interface in sub-threshold regime.

Sample preparation

N-channel FD-SOI MOSFETs were fabricated on lightly doped p-type ($\sim 10^{16}$ cm^{-3}) silicon-on-insulator SOI wafers with buried oxide (T_{BOX}) thickness of ~200 nm. Thermal oxidation was used to thin the SOI layer down to ~85 nm. The active area is patterned by optical lithography followed by dry etching. A sacrificial thermal oxide (~3 nm) is grown to remove the etch damage. After HF dip to remove the sacrificial oxide, a 3 nm gate thermal oxide is grown immediately. The channel region is patterned by optical lithography, and then ion implantation was performed to doped the source/drain regions n-type (5×10^{15} As$^+$/cm^2 at 80 keV, 7° tilt). Rapid thermal annealing (20 seconds at 900°C in N_2) was used to activate the dopants. A liftoff process was employed to deposit the non-self-aligned metal gate (30 nm Pt/10 nm Ti). Lastly, forming gas annealing (25 minutes at 350°C) was performed to improve Si/SiO_2 interface properties.

Results and Discussion

The sub-threshold conduction region corresponds to the depletion region, i.e., the surface potential ϕ_{sF} and ϕ_{sB} are smaller than $2\phi_F$ (ϕ_{sF} and $\phi_{sB} < 2\phi_F - kT/q$). Thus, to ensure both front and back channel are in sub-threshold region and this criterion, the drain current I_D versus front gate bias V_{gF} with different k values were taken at $V_{gF} > -0.3$ V under room temperature (300 K). A long channel device (5 um) with small drain voltage ($V_{DS} = 0.1$ V) was applied to avoid SCE. Fig. 1b shows the experimental data of FD-SOI and with k ratio 1, 1.5 and 2. The measured SS_F versus I_D are shown in Fig. 2. As the ratio k increases, the SS_F decreases because the faster back gate bias sweep helps the front and back channel current to rise, i.e., this SS_F is the combined result of the sweeping front the back gate voltages.[24] Note that for $k = 2$, the swing below 60 mV/dec does not contradict the well-known 60 mV/dec limit. If we express the swing in reference to the back gate voltage rather than the front gate voltage, the swing would be larger by a factor k, or <120 mV/decade. Eq. 6 automatically considers all these consequences of the back-front capacitive coupling effect.

We then applied Eq. 6 and iteratively varied $C_{itF}(\phi_{sF})$ and $C_{itB}(\phi_{sB})$ with ϕ_{sF} and ϕ_{sB} determined with Eqs. 3 and 4 until SS_F calculated with Eq. 6 matches the measured curves in Fig. 2. If only the experimental data at one k value is used in this extraction procedure, $C_{itF}(\phi_{sF})$ and $C_{itB}(\phi_{sB})$ cannot be uniquely determined. However, if two or more k values are used in this iterative extraction procedure, they can be determined in theory and ensured the data consistency. Note that here we choose optimum coupling

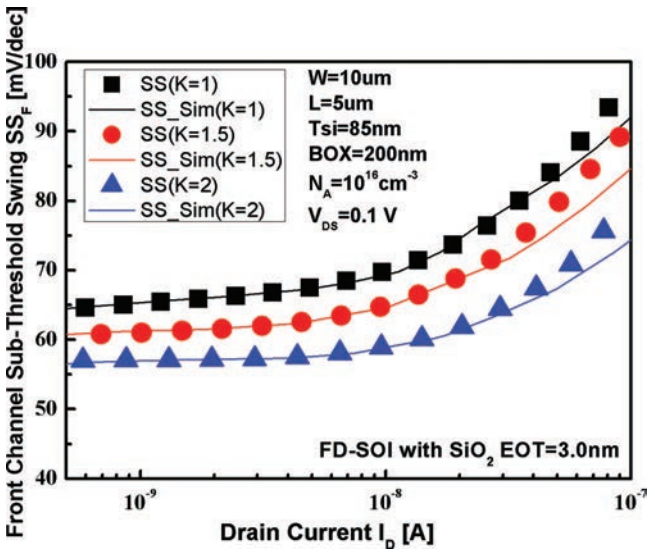

Figure 2. Symbols: Experimentally measured front gate sub-threshold swing versus corresponding I_D under three dual gate operation conditions with $k = 1$, 1.5 and 2. The measured SS_F is extracted from Figure 1. (b). Lines: Modeled SS_F by iteratively varying the D_{itF} and D_{itB} until the modeled SS_F match the measured data.

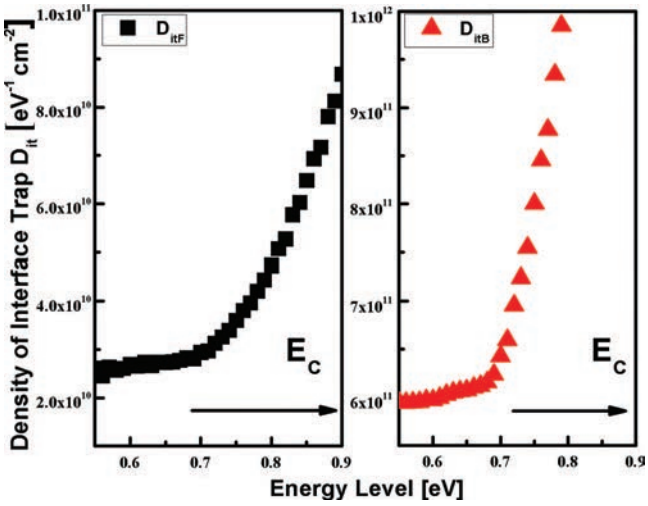

Figure 3. Extracted D_{it} distributions or the n-type FD-SOI MOSFET. U-shaped distribution over the energy gap and the larger back channel D_{itB} than the front channel D_{itF} agree with expectations.

condition (60 mv/dec)[13] at both front- and back surface potentials increase at the same rate with respect to the applied front gate voltage, i.e., $d\phi_{sF}/dV_{gF} = d\phi_{sB}/dV_{gF}$. The chosen of appropriate k value is necessary to achieve optimum coupling condition in this approach. We have found that using three k values allowed us to clearly extract a certain pair of $D_{itF,B}$. Excellent agreement between the data and reconstructed SS_F for the three k values can be seen in Fig. 2. Once a certain pair of D_{itF} and D_{itB} are adequately quantified from the iterative fitting method, the extraction has been fully completed. Fig. 3 plots the extracted trap densities against the surface potential. They exhibit the typical U-shaped distributions over the energy bandgap. The mid gap D_{it} extracted from this method for D_{itF} and D_{itB} are 2.30×10^{10} and 5.85×10^{11} (eV^{-1} cm^{-2}), respectively, which are in agreement with those generally reported.[3]

Conclusions

In this work, we demonstrated an experimental technique for extracting the front and back interface D_{it} simultaneously and the underlying theory. By extending the analytical model at DG condition, D_{itF} and D_{itB} can be determined through iteratively fitting the SS_F versus I_D data. The key is to simultaneously fit the data gathered at several ratios of the front and back gate voltage sweeping rates. The technique is used to demonstrate for the first time the extraction of the front and back interface D_{it} (E_t) distributions of an FD-SOI MOSFET. This technique can be valuable as the industry is developing the UTB-SOI technology with nm thin FD-SOI body as a 28 nm and beyond production technology.[25]

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