Planar GeOI TFET Performance Improvement With Back Biasing

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***Abstract*—Reverse back biasing of a planar germanium-on-insulator tunneling field-effect transistor provides for significant improvement in $I_{\rm ON}/I_{\rm OFF}$, by over an order of magnitude for 0.25 V operating voltage. Optimization of the gate-to-source overlap and source doping gradient is key to maximizing the benefit of back biasing.**

***Index Terms*—Germanium-on-insulator (GeOI), reverse back bias, tunneling FET (TFET).**

I. Introduction

OFF-STATE leakage current $(I_{\rm OFF})$ is a major challenge for continued miniaturization of the conventional metal–oxide–semiconductor field-effect transistor (MOSFET), because it limits threshold voltage (V_T) scaling and hence supply voltage $(V_{\rm DD})$ scaling so that power density now constrains chip design [1]. To address this issue, alternative transistor designs in which band-to-band tunneling (BTBT) rather than thermionic emission serves as the carrier-injection mechanism have been proposed [2]. For a tunneling FET (TFET) in the OFF state, BTBT current is very low because the energy bandgap serves to cut off the high-energy tail of the valence-electron distribution in the source [3]. The semiconductor material should have a small effective bandgap (E_g) for the TFET to achieve sufficiently high BTBT drive current in the ON state $(I_{\rm ON})$ to make it either a compelling alternative or a complementary low-power switching device to the MOSFET [4], [5]. Germanium (Ge) is a CMOS-compatible material that has a substantially smaller bandgap than does silicon (Si), so that Ge TFETs can achieve ~3 orders of magnitude higher $I_{\rm ON}$ than Si TFETs [4]. When E_g is small, BTBT at the drain junction in the OFF state can undesirably increase $I_{\rm OFF}$. To limit the component of $I_{\rm OFF}$ due to this reverse-biased diode leakage, the effective area of the drain-to-source junction should be limited, for example, by using a thin-body structure [6], [7].

Reverse back biasing has been reported to provide for improved ON/OFF current ratio $(I_{\rm ON}/I_{\rm OFF})$ in a thin-body Si TFET [8]. This work investigates the effect of a reverse back bias on the performance of a planar thin-body Ge n-channel TFET, and how the TFET design should be optimized to maximize the benefit of this effect. It is found that by co-optimizing the back-bias voltage (V_B) and the source design, $I_{\rm ON}/I_{\rm OFF}$ can be improved by more than 10× for a gate length of 30 nm.

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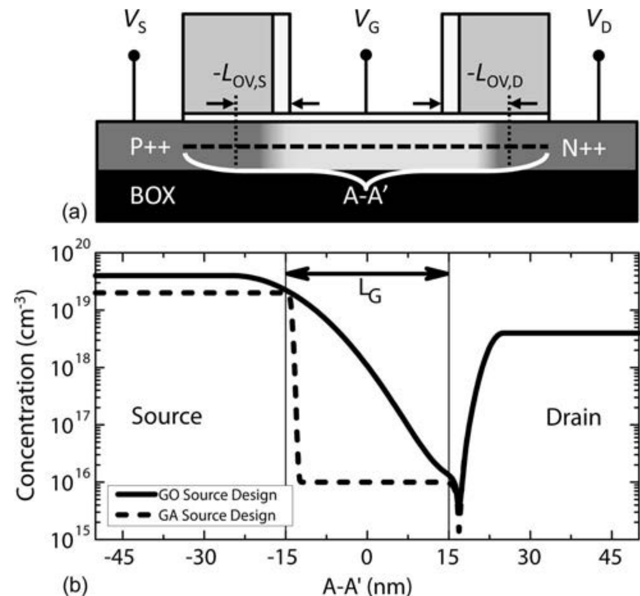

Fig. 1. (a) Schematic cross section of an n-channel planar GeOI TFET. A-A′ is the cutline for which the absolute value of the net dopant concentration profile is shown in (b). (b) Comparison of doping profiles for (solid line) a GO source design and (dashed line) a GA source design. The center of the channel region is located at $x = 0$ nm.

II. TFET Design and Simulation

A. Device Structure

Fig. 1(a) is a cross-sectional schematic illustration of the planar germanium-on-insulator (GeOI) TFET structure studied in this work. The voltage applied to the gate electrode (V_G) is capacitively coupled to the semiconductor surface potential via the gate dielectric layer; by changing this applied voltage, the electric field within the semiconductor is modulated. For tunneling to occur, the electric field must be sufficiently large to cause the valence band to overlap (in energy) with the conduction band. A built-in electric field either within the source region or across the source–channel junction reduces the gate-voltage swing needed to induce a band overlap, i.e., it results in steeper switching behavior [9]. The rate of carrier injection is

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exponentially dependent on the width of the tunneling barrier, which depends on both E_g and the magnitude of the electric field F [2], [10]. This suggests that an abrupt source doping profile should be optimal for tunneling from the source to the channel [11]. Kane's model provides a compact expression for the BTBT current

$$I_{\mathrm{TUNNEL}} \propto A \cdot F \cdot \exp(-B/F) \quad (1)$$

where A and B are material-dependent parameters [12].

The net doping profiles within the semiconductor layer along the A-A′ cutline are shown in Fig. 1(b), for two TFET designs. One has a maximum p-type source dopant concentration of 2×10^{19} cm^{-3} aligned to the gate edge and a narrow Gaussian source doping profile that corresponds to a gradient of 1 nm/dec; this is heretofore referred to as the gate-aligned (GA) source design. The other has a maximum p-type source dopant concentration of 4×10^{19} cm^{-3} offset from the gate edge by 10 nm and a wide Gaussian source doping profile that corresponds to a gradient of 20 nm/dec; this is heretofore referred to as the gate-overlapped (GO) source design. As will be shown hereinafter, the GA source design is optimal if $V_B = 0$ V, but the GO source design is optimal if $V_B < 0$ V.

B. Fixed Device Design Parameters

The default value for the gate length (L_G) is 30 nm to avoid significant short-channel effects, as will be discussed hereinafter. The other fixed design parameters are chosen to achieve good electrostatic integrity: The Ge thickness (T_{Ge}) is 10 nm, the gate dielectric has an equivalent oxide thickness of 0.8 nm, and the buried oxide layer is 10 nm thick. The gate-sidewall spacers comprise an inner 5-nm-thick silicon dioxide layer and an outer 15-nm-thick silicon nitride layer. The Ge-channel region is lightly doped p-type $(10^{15}$ $\mathrm{cm}^{-3})$. The gate material is metallic with a work function of 4.0 eV. Ohmic contacts to the source and drain regions (each 30 nm long) are made along the upper Ge surfaces outside of the spacers. The underlying substrate is p-type silicon $(1 \times 10^{19}$ cm^{-3} dopant concentration). The n-type drain has a maximum dopant concentration of 4×10^{18} cm^{-3} that is offset from the edge of the gate by 10 nm and a Gaussian doping profile that corresponds to a gradient of 5 nm/dec [refer to Fig. 1(b)]. This drain design was found to be optimal for minimizing OFF-state leakage without degrading $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$, for $V_{\mathrm{DD}} = 0.25$ V and $V_B = 0$ V.

C. Variable Device Design Parameters

The maximum source dopant concentration N_{SRC} was varied from 1×10^{18} cm^{-3} to 1×10^{20} cm^{-3} in this study. The source doping profile decays as a Gaussian function toward the channel region. The gate-to-source overlap $L_{\mathrm{OV},S}$ is defined as the distance from the gate edge to the position where the Gaussian decay begins. (If $L_{\mathrm{OV},S}$ is negative, the source doping profile begins decaying from a position to the left of the gate edge. If $L_{\mathrm{OV},S}$ is positive, the source doping profile begins decaying from a position to the right of the gate edge, underneath the gate.) $L_{\mathrm{OV},S}$ was varied from -14 to 6 nm, and the doping gradient (DG) was varied from 1 to 22 nm/dec, in this study. The three source-design parameters (N_{SRC}, $L_{\mathrm{OV},S}$, and DG), as well as the body thickness T_{Ge}, influence the location and size of the tunneling region and thereby $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$.

D. Device Simulation

Synopsys TCAD software was used to study the performance of GeOI TFETs via 2-D device simulations. Sentaurus Structure Editor was used to define the TFET structure, and Sentaurus Device was used to simulate device operation using a dynamic nonlocal BTBT model based on Kane's model [13]. The properties of Ge are well characterized, so the default Ge material parameters were used in this work: $A = 2.8 \times 10^{15}$ $\mathrm{cm}^{-3} \cdot \mathrm{s}^{-1}$ and $B = 1.9 \times 10^7$ V/cm. The dynamic nonlocal BTBT model has been demonstrated to be in good agreement with experimental results [14].

III. Results and Discussion

A. GA versus GO Source Designs

$I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ is the figure of merit used to assess various TFET designs in this work. Typically, a TFET exhibits steeper subthreshold slope (*SS*) at lower currents [15]. Since steeper *SS* results in higher $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ for a given gate-voltage swing, TFETs are more advantageous for applications requiring low I_{OFF} and low operating voltage, e.g., for $V_{\mathrm{DD}} \leq 0.25$ V [5]. In this paper, I_{ON} is defined to be the drain current I_D at $V_{\mathrm{GS}} - V_{\mathrm{OFF}} = 0.25$ V for $V_{\mathrm{DS}} = 0.25$ V, where V_{OFF} is defined to be the value of the gate-to-source voltage (V_{GS}) that corresponds to $I_D = I_{\mathrm{OFF}} = 100$ fA$/\mu$m. (In other words, it is assumed that, in practice, gate-work-function engineering and delta doping can be used to tune V_T, as for a MOSFET, so that $V_{\mathrm{OFF}} = 0$ V.)

Fig. 2 shows how $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ varies with $L_{\mathrm{OV},S}$ and the DG, for the two values of N_{SRC} $(2 \times 10^{19}$ cm^{-3} and 4×10^{19} $\mathrm{cm}^{-3})$ that correspond to the optimized GA and GO source designs with $L_G = 30$ nm. Fig. 2(a) and (b) is $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ contour plots for $V_B = 0$ V, while Fig. 2(c) and (d) is $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ contour plots for $V_B = -1.7$ V. The hatched region in Fig. 2(b) shows the range of $L_{\mathrm{OV},S}$ and DG combinations that result in $I_{\mathrm{OFF}} > 100$ fA$/\mu$m due to the short-channel effect.

A comparison of Fig. 2(a) and (b) shows that the GA source design is optimal (i.e., provides for the highest $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$) when $V_B = 0$ V, since the contours peak when $L_{\mathrm{OV},S}$ is near 0 nm and the DG is close to 1 nm/dec. (This is a representative of the trend seen for the entire range of N_{SRC} values studied in this work, when $V_B = 0$ V.) Note that the design window for optimal performance is relatively narrow. This is because tunneling occurs primarily from the GA source region to the channel inversion layer, so that it is highly sensitive to the alignment between the source–channel junction and the gate edge: If the gate underlaps the source, then gate coupling to the channel at the source junction is degraded; if the gate overlaps the source, then the source depletion width (hence, tunneling distance) is increased.

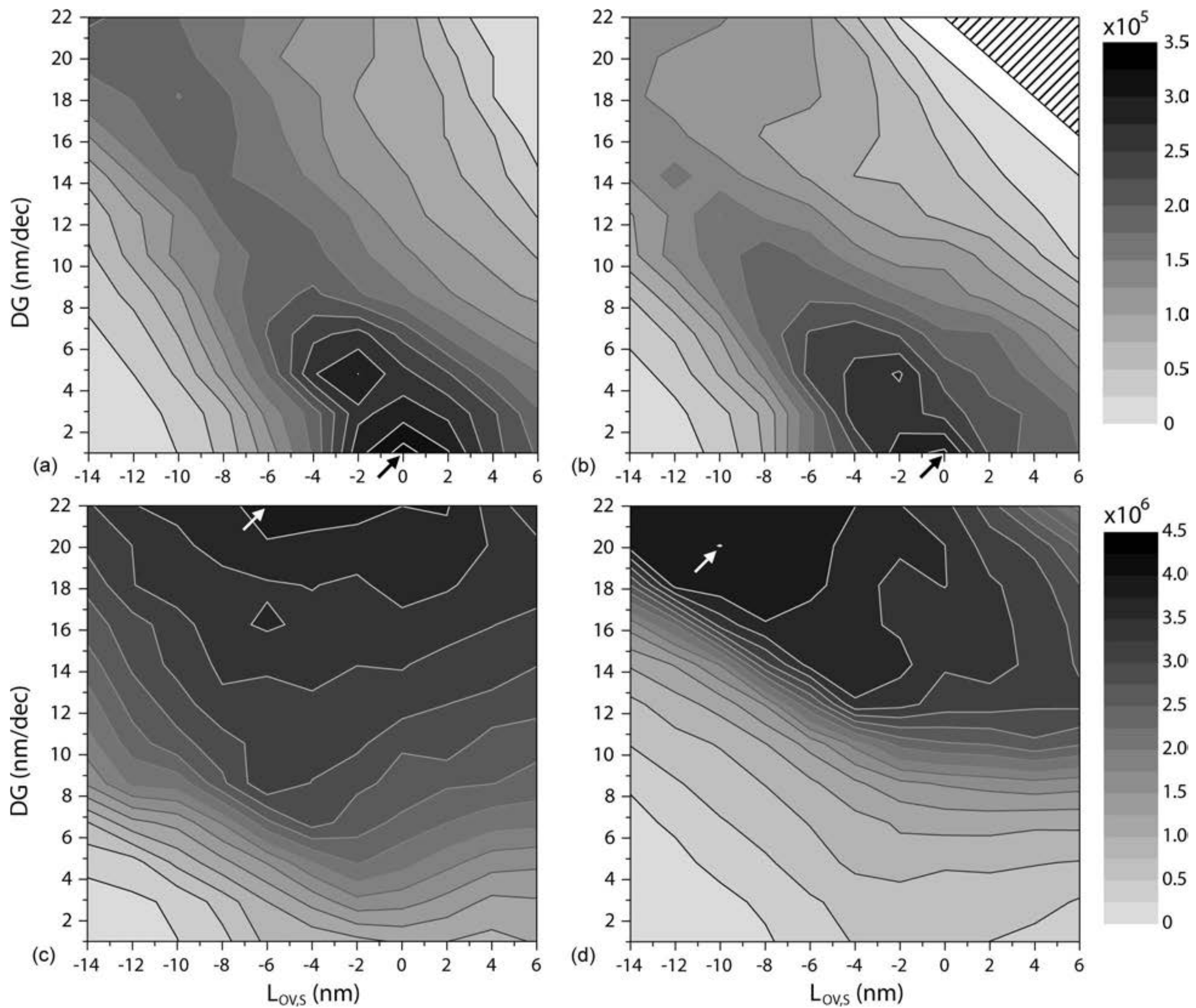

Fig. 2. $I_{\rm ON}/I_{\rm OFF}$ contour plots showing how GeOI TFET performance depends on the source doping gradient and the gate-to-source overlap, for different peak source-dopant-concentration ($N_{\rm SRC}$) values and applied back bias (V_B) values. (a) $N_{\rm SRC} = 2 \times 10^{19}$ cm^{-3} and $V_B = 0$ V. (b) $N_{\rm SRC} = 4 \times 10^{19}$ cm^{-3} and $V_B = 0$ V. (c) $N_{\rm SRC} = 2 \times 10^{19}$ cm^{-3} and $V_B = -1.7$ V. (d) $N_{\rm SRC} = 4 \times 10^{19}$ cm^{-3} and $V_B = -1.7$ V. The arrow indicates the maximum $I_{\rm ON}/I_{\rm OFF}$ point in each contour plot.

A comparison of Fig. 2(c) and (d) shows that the GO source design is optimal when $V_B = -1.7$ V, since the contours peak at larger values of the DG. [If $DG \times 1$ dec $> -L_{{\rm OV},S}$, then the source doping profile extends underneath the gate electrode, as in Fig. 1(b)]. Note that the design window for optimal performance is relatively wide. This is because tunneling occurs primarily within the GO source region, so that $I_{\rm ON}$ is largely dependent on the extent of the gate-to-source overlap: Many combinations of the DG and $L_{{\rm OV},S}$ result in the same overlap and hence comparable $I_{\rm ON}$; $I_{\rm ON}$ falls off with increasing $L_{{\rm OV},S}$ when the short-channel effect becomes significant.

As shown in Fig. 3, reverse back biasing is beneficial for both source designs (using the doping profiles optimized for $L_G = 30$ nm) but more so for the GO design so that it becomes superior to the GA design when $V_B < -0.25$ V. $I_{\rm ON}/I_{\rm OFF}$ reaches a peak at $V_B = -1.7$ V for the GO design, whereas it does not reach a peak for the GA design within the range of V_B values studied. To elucidate the reasons for this, Fig. 4 shows linear-scale contour plots of BTBT generation rate at $V_{\rm GS} - V_{\rm OFF} = 0.25$ V and $V_{\rm DS} = 0.25$ V, for four cases: the GA design and the GO design each at $V_B = 0$ V and $V_B = -1.7$ V. The dashed line in each plot indicates the horizontal position of the gate edge. The lower contours which extend to the left beyond the gate edge indicate the hole-generation rate, while the upper contours which extend to the right under the gate electrode indicate the electron generation rate. For the GA design [Fig. 4(a) and (b)], it can be seen that tunneling occurs primarily from the source region to the channel inversion layer; the application of a reverse back bias enhances (the vertical component of) the electric field and thereby improves $I_{\rm ON}/I_{\rm OFF}$. For the GO design, it can be seen that tunneling occurs primarily within the source region. With zero back bias, the GO design serves as poorly gated Zener diode [Fig. 4(c)]. Reverse back biasing enhances the vertical component of electric field, resulting in BTBT over a relatively wide region within the source underneath the gate electrode; the larger tunneling area results in larger $I_{\rm ON}$ for the reverse-back-biased GO design [Fig. 4(d)].

For a fixed value of L_G and a given drain doping profile, $I_{\rm ON}/I_{\rm OFF}$ for the GO design reaches a peak near

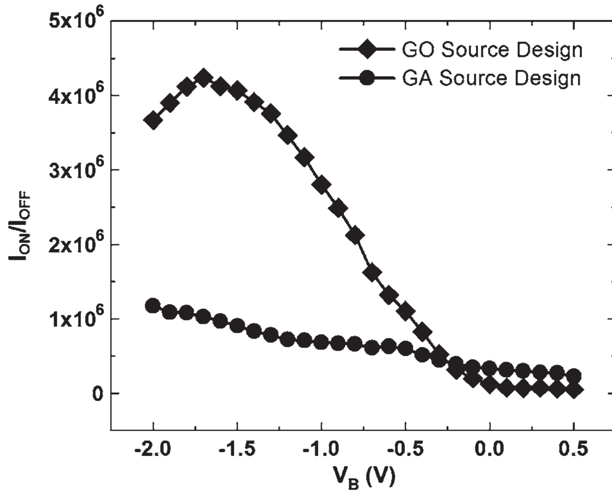

Fig. 3. Impact of back-bias voltage on $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ for the two GeOI TFET designs: GA source and GO source.

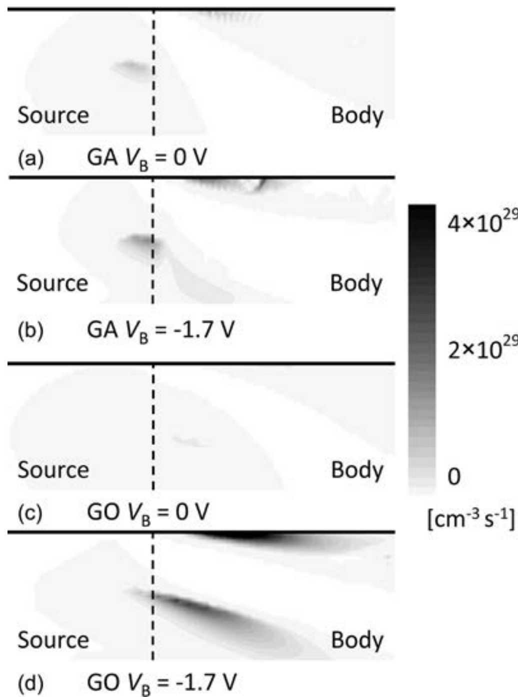

Fig. 4. GeOI TFET ON-state ($V_{\mathrm{GS}} - V_{\mathrm{OFF}} = 0.25$ V and $V_{\mathrm{DS}} = 0.25$ V) BTBT rate (linear scale) contour plots for (a) GA source design with $V_B = 0$ V, (b) GA source design with $V_B = -1.7$ V, (c) GO source design with $V_B = 0$ V, and (d) GO source design with $V_B = -1.7$ V.

$V_B = -1.7$ V. This is because a significant hole-accumulation region forms near the drain junction and thereby introduces significant series resistance which decreases I_{ON} for $V_B < -1.7$ V. (Although a similar peak is not observed for the GA design within the range of the V_B values studied, increasing drain-side series resistance should eventually limit the improvement in $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ for this design as well.) Further optimization of the drain doping profile may lead to greater $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ improvement for large reverse-back-bias voltages.

Fig. 5 compares the transfer characteristics for the two optimized source designs, with and without reverse back biasing. The GA design (optimized at $N_{\mathrm{SRC}} = 2 \times 10^{19}$ cm^{-3}, $L_{\mathrm{OV},S} = 0$ nm, and $DG = 1$ nm/dec) achieves $I_{\mathrm{ON}}/I_{\mathrm{OFF}} = 3.26 \times 10^5$ at $V_B = 0$ V and $I_{\mathrm{ON}}/I_{\mathrm{OFF}} = 1.03 \times 10^6$ at $V_B = -1.7$ V, representing more than 3× improvement with reverse back biasing. The GO design (optimized at $N_{\mathrm{SRC}} = 4 \times 10^{19}$ cm^{-3}, $L_{\mathrm{OV},S} = -10$ nm, and $DG = 20$ nm/dec) achieves $I_{\mathrm{ON}}/I_{\mathrm{OFF}} = 1.22 \times 10^5$ at $V_B = 0$ V and $I_{\mathrm{ON}}/I_{\mathrm{OFF}} = 4.24 \times 10^6$ at $V_B = -1.7$ V, representing more than 34× improvement with reverse back biasing. These results affirm that the GA design is superior when there is no applied back bias (solid dark curve in Fig. 5) and that the GO design becomes superior if a significant reverse back bias is applied (gray dotted line in Fig. 5).

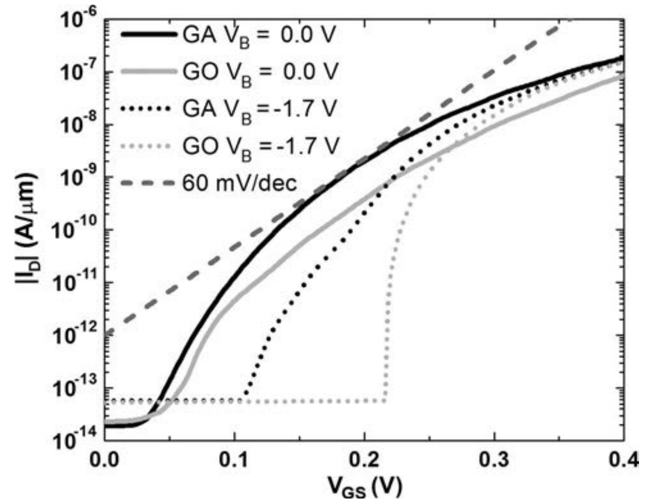

Fig. 5. Comparison of simulated GeOI TFET transfer characteristics for the GA and GO source designs, with and without reverse back biasing.

The OFF-state leakage current is slightly larger with $V_B = -1.7$ V for both the GA and GO designs, due to an increase in the volume of the space-charge region resulting in more recombination–generation current. It should be noted that the turn-on voltage (V_{OFF}) increases and that *SS* becomes steeper with reverse back biasing. This is somewhat analogous to the increase in V_T and the improved electrostatic integrity of a thin-body MOSFET with reverse back biasing [16]. For the GA design, a larger gate voltage is required to form an inversion layer in the lightly doped channel region (to which carriers tunnel from the source region) when a reverse back bias is applied, and an enhanced electric field in the ON state provides for greater BTBT current. For the GO design, a larger gate voltage is also required to invert the Ge surface (to allow BTBT to occur within the source region); however, since the source has a graded doping profile, this increase in required gate voltage is not uniform across the lateral extent of the source—it increases with decreasing dopant concentration. Since a larger gate voltage is required to invert the surface of a more heavily doped semiconductor when $V_B = 0$ V, the effect of the reverse back bias is to induce a graded shift in turn-on voltage so that band overlap occurs more uniformly across the source region, and hence, the TFET switches more abruptly.

B. Short-Channel Effect

Fig. 6 shows how GeOI TFET performance depends on L_G for the GA and GO source designs optimized for $L_G = 30$ nm.

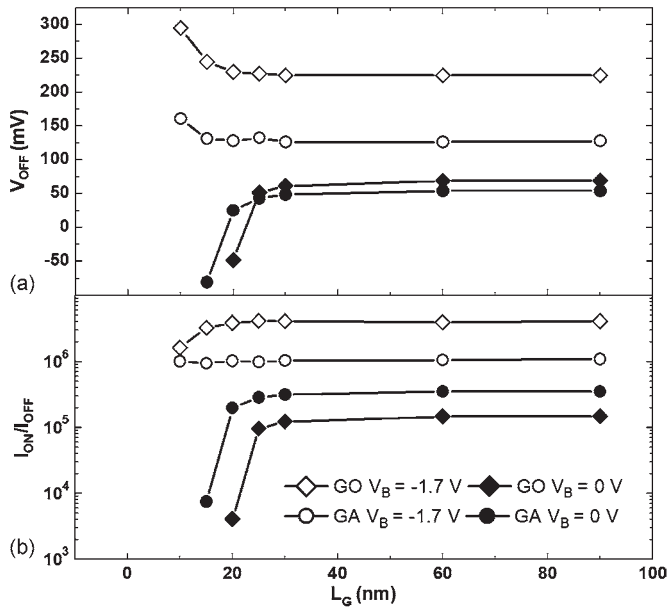

Fig. 6. Dependence of (a) $V_{\rm OFF}$ and (b) $I_{\rm ON}/I_{\rm OFF}$ on $L_G \geq 10$ nm for GeOI TFETs with GO or GA source designs, with or without reverse back bias. $V_{\rm OFF}$ is defined as $V_{\rm GS}$ when $I_D = 100$ fA/μm. Reverse back biasing mitigates the short-channel effect and therefore improves scalability. $I_{\rm ON}/I_{\rm OFF}$ ($V_B = -1.7$ V) decreases with decreasing L_G for the GO design due to a corresponding decrease in the gate area overlapping the tunneling area. $V_{\rm OFF}$ and $I_{\rm ON}/I_{\rm OFF}$ are not defined when I_D remains $>$ 100 fA/μm.

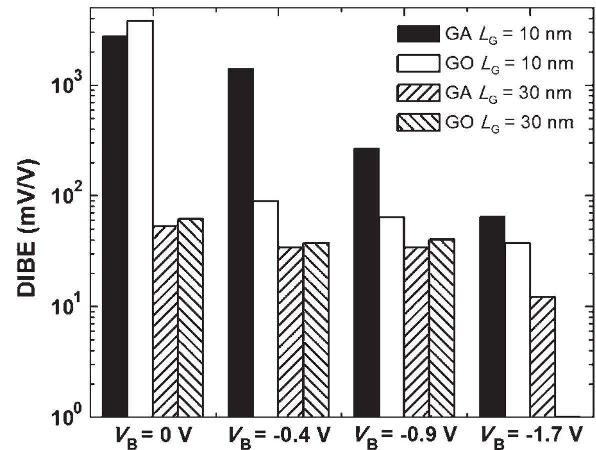

Fig. 7. Comparison of the DIBE on a log scale for GA versus GO source designs, at various values of back-bias voltage. DIBE is the change in $V_{\rm OFF}$ (in millivolts) for 0.025 V $\leq V_{\rm DS} \leq$ 0.25 V. For $L_G = 30$ nm, both designs show low DIBE (which disappears altogether for the GO design at $V_B = -1.7$ V). For $L_G = 10$ nm, reverse back biasing mitigates DIBE more effectively for the vertical tunneling (GO) design than for the lateral tunneling (GA) design, since the latter is inherently more susceptible to the influence of the drain bias on the lateral electric field.

Note that there is no gate-length dependence for $L_G > 30$ nm; in this regime, the drain bias has little influence on the BTBT rate. As L_G decreases below 30 nm, the lateral electric field induced at the tunneling junction by the drain voltage increases sufficiently to cause BTBT to occur at a smaller gate voltage. This is manifested as a decrease in $V_{\rm OFF}$ with decreasing L_G (Fig. 6(a), $V_B = 0$ V). As a result, the influence of the gate voltage is diminished, i.e., *SS* becomes less steep, and hence, $I_{\rm ON}/I_{\rm OFF}$ decreases (Fig. 6(b), $V_B = 0$ V). It is interesting to note that, although the GO design results in a much shorter electrical channel length, degradation in $I_{\rm ON}/I_{\rm OFF}$ occurs only slightly earlier (i.e., beginning at slightly longer L_G) because BTBT occurs in a more vertical direction so that drain-induced BTBT is not much more significant than for the GA design, as can be deduced from the comparison of drain-induced BTBT effect (DIBE) in Fig. 7.

Reverse back biasing provides for more dominant gate control of the BTBT current and thereby reduces the short-channel effect. As L_G decreases below 30 nm, the average p-type doping underneath the gate electrode increases so that the gate voltage required to induce BTBT (i.e., $V_{\rm OFF}$) increases. Also, for the GO design, $I_{\rm ON}/I_{\rm OFF}$ decreases with decreasing L_G due to decreased tunneling area. Reoptimizing the source and drain doping profiles for each value of $L_G < 30$ nm can help to mitigate these short-channel effects.

C. Design Optimization for Vertical Tunneling

From Fig. 4, it can be deduced that the highest $I_{\rm ON}$ is achieved when BTBT occurs within the source (i.e., in a more vertical direction), because the tunneling area can be readily increased by increasing the gate-to-source overlap and/or applying a reverse back bias, in this case. Many combinations of DG and $L_{{\rm OV},S}$ result in the same overlap, but a close examination of Fig. 2(c) and (d) reveals that higher $I_{\rm ON}/I_{\rm OFF}$ is achieved with a more graded source doping profile when a significant reverse back bias is applied. (For a fixed value of $DG \times 1$ dec $+ L_{{\rm OV},S} > 0$, higher $I_{\rm ON}/I_{\rm OFF}$ is achieved with larger DG rather than with larger $L_{{\rm OV},S}$, i.e., with a graded source rather than with a uniform source.) This is because lighter source doping at the channel junction reduces the likelihood of lateral (source-to-channel) BTBT which is associated with worse *SS* (refer to Fig. 5). To highlight this point, the impact of $N_{\rm SRC}$ is shown in Fig. 8, for the GA and GO source designs as well as a uniformly doped source design with $L_{{\rm OV},S} = 10$ nm and $DG = 1$ nm/dec. ($L_G = 60$ nm in this figure only, to avoid the short-channel effect for the uniformly doped source design.) $I_{\rm ON}/I_{\rm OFF}$ for the uniformly doped source design dips below that for the GO source design near $N_{\rm SRC} = 1 \times 10^{19}$ cm^{-3} as BTBT transitions from tunneling primarily within the source (as for the GO source design) to tunneling primarily from the source to the channel (as for the GA source design).

Fig. 9 shows the simulated GeOI TFET output characteristics for the GA and GO source designs, with and without reverse back biasing. The small-signal output resistance r_o is taken to be the inverse slope of a best fit line from 0.20 V $\leq V_{\rm DS} \leq$ 0.25 V for $V_{\rm GS} - V_{\rm OFF} = 0.25$ V. Reverse back biasing depletes the drain offset region, forming a barrier to electron flow; this barrier (rather than BTBT at the source) is modulated by the drain bias, so that r_o is reduced when $V_B = -1.7$ V. Despite this, intrinsic gain ($g_m r_o$, evaluated at $V_{\rm GS} - V_{\rm OFF} = V_{\rm DS} =$ 0.25 V) remains well above one, decreasing from 13.0 to 5.7 for the GA design and from 20.1 to 9.1 for the GO design when V_B is changed from 0 to -1.7 V. As can be seen in Fig. 9, reverse back biasing improves the linearity of the I_D V_D characteristic at low values of $V_{\rm DS}$, which is consistent with a reduction in DIBE (refer to Fig. 7).

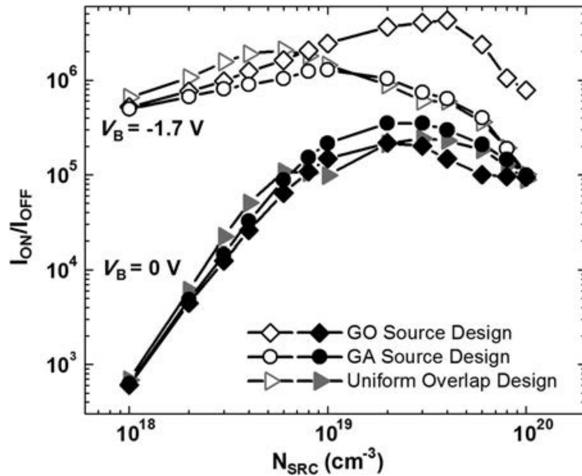

Fig. 8. Impact of peak source dopant concentration (N_{SRC}) on $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$, for GeOI TFETs with GA, GO, or uniform source ($L_{\mathrm{OV},S} = 10$ nm and $DG = 1$ nm/dec) designs. $L_G = 60$ nm to avoid the short-channel effect. The uniformly doped source design transitions from tunneling within the source to tunneling from the source to the channel near $N_{\mathrm{SRC}} = 10^{19}$ cm^{-3}. The GO design outperforms the other designs at $V_B = -1.7$ V, for $N_{\mathrm{SRC}} \geq 10^{19}$ cm^{-3}.

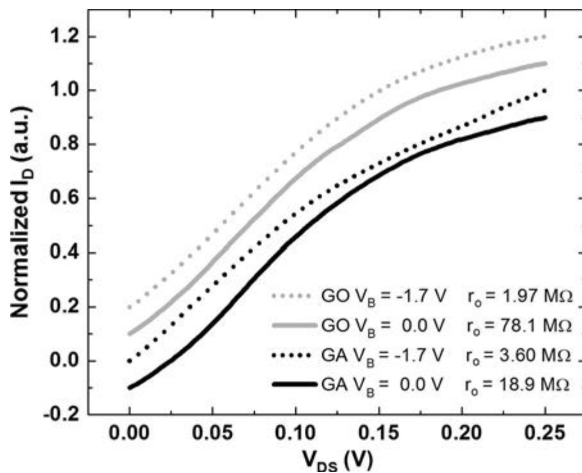

Fig. 9. Comparison of output current normalized to the maximum value at $V_{\mathrm{GS}} - V_{\mathrm{OFF}} = 0.25$ V and $V_{\mathrm{DS}} = 0.25$ V, as a function of the drain-to-source voltage. The output characteristics have been offset for clarity.

D. Impact of Ge Thickness

T_{Ge} should be sufficiently thick so as to avoid fully vertically depleting the source region underneath the gate if vertical BTBT within the source is desired. (Also, if T_{Ge} is too thin, quantum confinement effects can reduce the density of states for tunneling, even if lateral BTBT from the source to the channel is desired.) For a source doping level of 2×10^{19} cm^{-3}, T_{Ge} should be at least 10 nm to avoid full vertical depletion. As shown in Fig. 10, reverse-biased diode leakage is adequately suppressed at this thickness.

IV. Conclusion

Reverse back biasing of a planar GeOI TFET is beneficial for improving $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$, more so for a vertical tunneling design ($> 30\times$ enhancement) than for a lateral tunneling design ($\sim 3\times$ enhancement). For the reverse-back-biased vertical tunneling

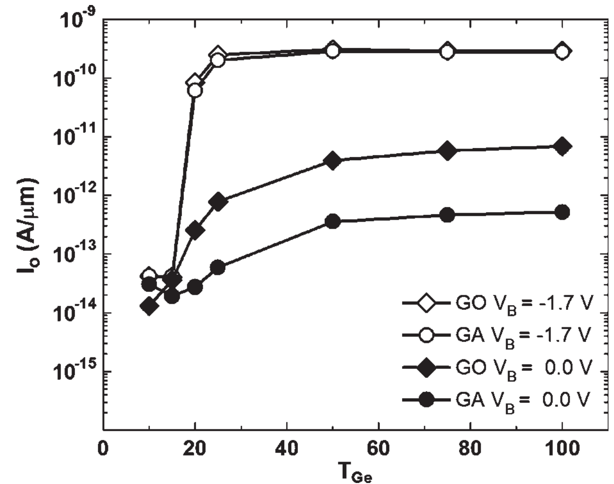

Fig. 10. OFF-state leakage current (I_D at $V_{\mathrm{GS}} = 0$ V) in a GeOI TFET as a function of the Ge thickness, for the different source designs with and without reverse back biasing. Reverse diode leakage current (due to BTBT at the drain junction) increases linearly with the diode area and is dramatically enhanced by reverse back biasing to increase the electric field.

design, a graded source doping profile provides for superior performance due to reduced short-channel effect and more uniform band overlap across the lateral extent of the source region. The results of this study indicate that reverse back biasing is a more effective performance booster for a GeOI TFET than for a SOI TFET [8]. This is because band overlap can be induced across a shorter distance within Ge, because of its smaller bandgap, so that more vertical tunneling can be induced with reverse back biasing in a thin-body Ge TFET versus a thin-body Si TFET. (Likewise, the benefit of reverse back biasing should be greater for semiconductor materials with even smaller bandgap.) Finally, reverse back biasing is also beneficial for improving TFET scalability, particularly if the source and drain doping profiles are co-optimized together with the gate length.

Acknowledgment

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