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# Nanoscale InGaSb Heterostructure Membranes on Si Substrates for High Hole Mobility Transistors

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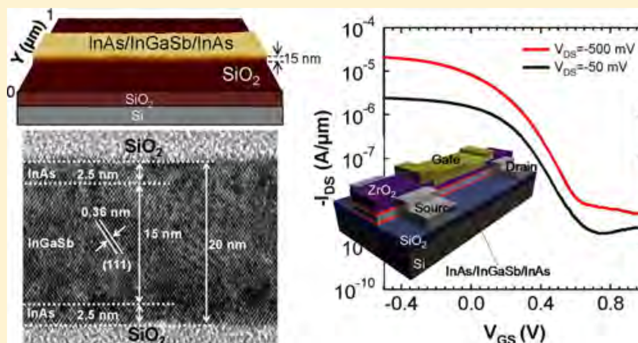
Supporting Information

**ABSTRACT:** As of yet, III–V p-type field-effect transistors (p-FETs) on Si have not been reported, due partly to materials and processing challenges, presenting an important bottleneck in the development of complementary III–V electronics. Here, we report the first high-mobility III–V p-FET on Si, enabled by the epitaxial layer transfer of InGaSb heterostructures with nanoscale thicknesses. Importantly, the use of ultrathin (thickness, ~2.5 nm) InAs cladding layers results in drastic performance enhancements arising from (i) surface passivation of the InGaSb channel, (ii) mobility enhancement due to the confinement of holes in InGaSb, and (iii) low-resistance, dopant-free contacts due to the type III band alignment of the heterojunction. The fabricated p-FETs display a peak effective mobility of ~820 $cm^2/(V\ s)$ for holes with a subthreshold swing of ~130 mV/decade. The results present an important advance in the field of III–V electronics.




**KEYWORDS:** *III–V-on-insulator, MOSFETs, XOI, two-dimensional membranes, heterojunction*

High-mobility III–V compound semiconductors have been extensively explored as a potential replacement for the active channel material of scaled transistors with the promise of delivering high ON currents at low voltages.[1−4] Integration on Si substrates is required in order to present a scalable, cost-effective platform. Conventionally, these materials are epitaxially grown on III–V wafers,[1,2,4] which have limited their use for consumer electronics due to the relatively high costs. In the past several years, direct growth of complex III–V multilayers has been demonstrated for enabling InGaAs-based n-FETs on Si substrates.[5] The large lattice mismatch of III–V semiconductors and Si, however, presents a challenge in the successful epitaxial growth of the layers with low defect densities.[6,7] This problem is especially prominent for Sb-based semiconductors,[6] such as $In_xGa_{1-x}Sb$, which are the most promising candidates for high hole mobility active layers.[2,8−10] For instance, InSb and GaSb have large lattice mismatches of ~19% and ~12% with Si, respectively.[2] Recently, epitaxial layer transfer (ELT)[11−13] of ultrathin InAs layers onto $Si/SiO_2$ substrates[14−16] has been demonstrated for integrating n-type III–V semiconductors on Si substrates. The approach is termed XOI, referring to the III–V-on-insulator device architecture that resembles the conventional Si-on-insulator (SOI) substrates. In the XOI framework, the choice of the active semiconductor layer is decoupled from the support substrate.[17] High electron mobility ($\mu_n$ = 4000−1000 $cm^2/(V\ s)$) InAs XOI n-FETs with performances better than conventional Si MOSFETs of comparable length scales have been demonstrated.[14] A challenge, however, remains in the fabrication of high hole mobility III–V p-FETs and more specifically on Si substrates. Recently, buried channel, strained InGaSb p-FETs on III–V substrates have been reported with an effective hole mobility of ~1230 $cm^2/(V\ s)$, higher than that of Si or unstrained Ge p-MOSFETs.[8,18] These results are promising, clearly demonstrating the need for integration of a high hole mobility III–V semiconductor, such as InGaSb, on Si in order to realize III–V CMOS electronics. In this work,

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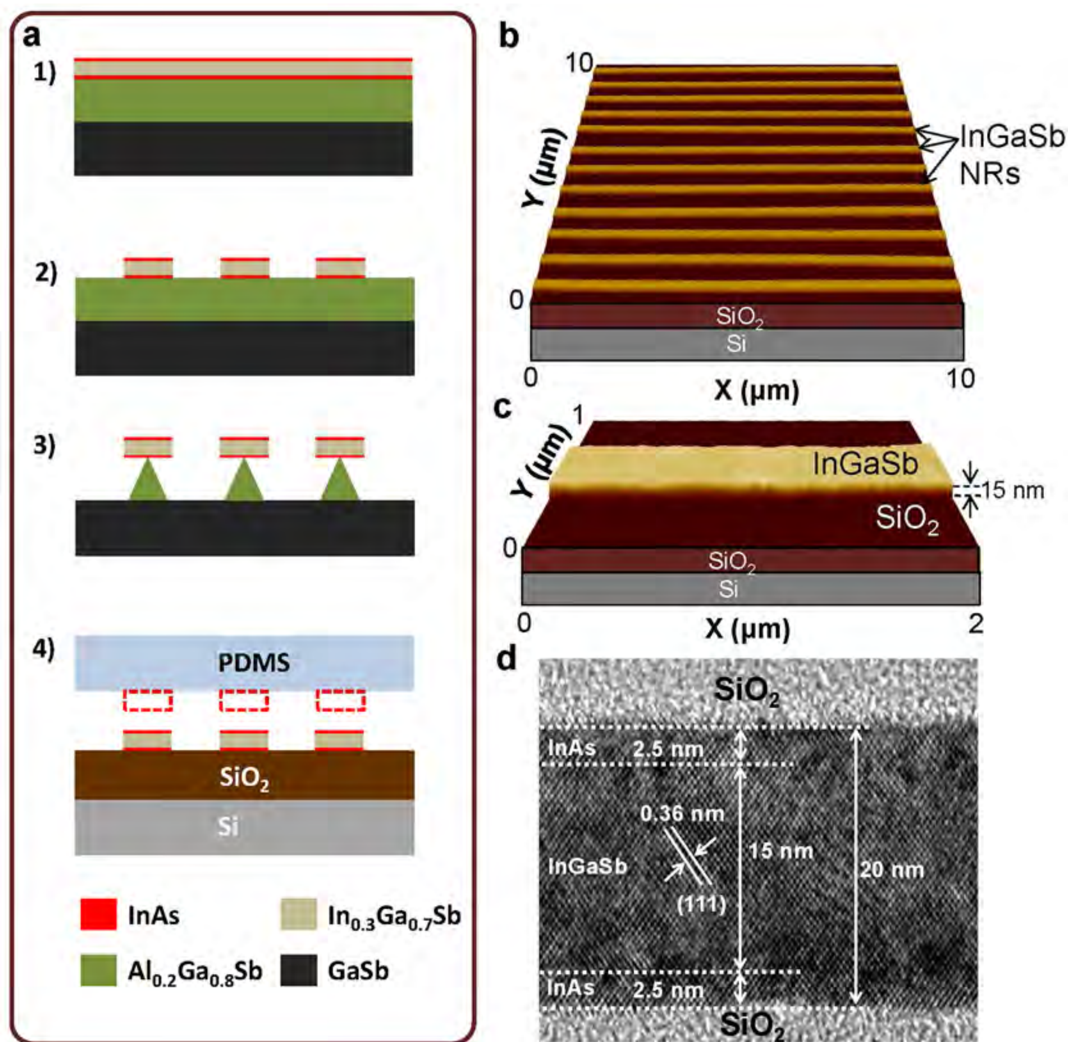


**Figure 1.** InAs/InGaSb/InAs heterostructure XOI. (a) Process schematic illustrating the fabrication of ultrathin InAs/InGaSb/InAs XOI substrates. The initial structure (1) is first prepatterned into NRs by lithography and wet etching (2). Afterward, the AlGaSb sacrificial layer is etched to partially release the NRs (3) which are subsequently transferred onto a Si/$SiO_2$ substrate by employing a PDMS slab (4). (b,c) AFM images of transferred InAs/InGaSb/InAs NRs on a Si/$SiO_2$ substrate with a width and height of ~350 and ~15 nm ($T_{InGaSb}$ = 10 nm), respectively. (d) TEM image of an InAs/InGaSb/InAs XOI ($T_{InGaSb}$ = 15 nm).

ELT of ultrathin InAs/$In_{0.3}Ga_{0.7}Sb$/InAs heterostructures is utilized for the fabrication of p-type XOI FETs on Si substrates. Here, InGaSb is used as the channel material with a ~2.5 nm thick InAs capping layer for passivation of the surface and for dopant-free, low-resistance contacts. Importantly, the use of this few layer thick interfacial InAs layer is essential for (i) fabrication of devices without significant InGaSb oxidation, (ii) hole confinement in the channel, and (iii) ohmic metal contact formation, without dopant profiling.

The process schematic for the fabrication of InAs/InGaSb/InAs heterostructure XOI is depicted in Figure 1a. First, $Al_{0.2}Ga_{0.8}Sb$ (thickness, 60 nm), InAs (thickness, 3 nm), $In_{0.3}Ga_{0.7}Sb$ (thickness, 7−15 nm), and InAs (thickness, 3 nm) layers are epitaxially grown on a (100) GaSb wafer by molecular beam epitaxy (MBE). In this stack, AlGaSb is the sacrificial layer for the ELT technique, and InAs layers are the surface cladding caps for InGaSb channel material. InAs/InGaSb/InAs layers were patterned into nanoribbon (NR) structures by lithography and wet etching (see Supporting Information). The NRs were subsequently picked and transferred onto a Si/$SiO_2$ receiver substrate by the use of a polydimethylsiloxane (PDMS) slab as previously demonstrated for the ELT of InAs.[14] Atomic force microscopy (AFM) images of the resulting NRs on a Si/$SiO_2$ substrate are shown in Figure 1b,c, clearly depicting that uniform layer transfer can be achieved with minimal surface roughness.

The high quality of the single crystalline InAs/InGaSb/InAs XOI layers is evident from transmission electron microscopy (TEM, Figure 1d). As shown, the InAs layers were slightly reduced in thickness (by ~0.5 nm) during the XOI transfer process, which is attributed to removal of a thin native oxide layer during the XOI processing steps. InAs cladding layers affect the energy band alignment of the system, as explained in detail below, while passivating the highly reactive InGaSb layer from oxidation during the ELT and subsequent device processing. For instance, the control samples prepared without the use of InAs cap resulted in the oxidation of the InGaSb layer by up to ~6 nm on each side (a loss of 12 nm total), as shown in Figure S1, Supporting Information.

Device simulation (NextNano) was used to calculate the energy band diagram of the InAs/InGaSb/InAs XOI heterostructure (Figure 2). The device consists of two distinct regions.

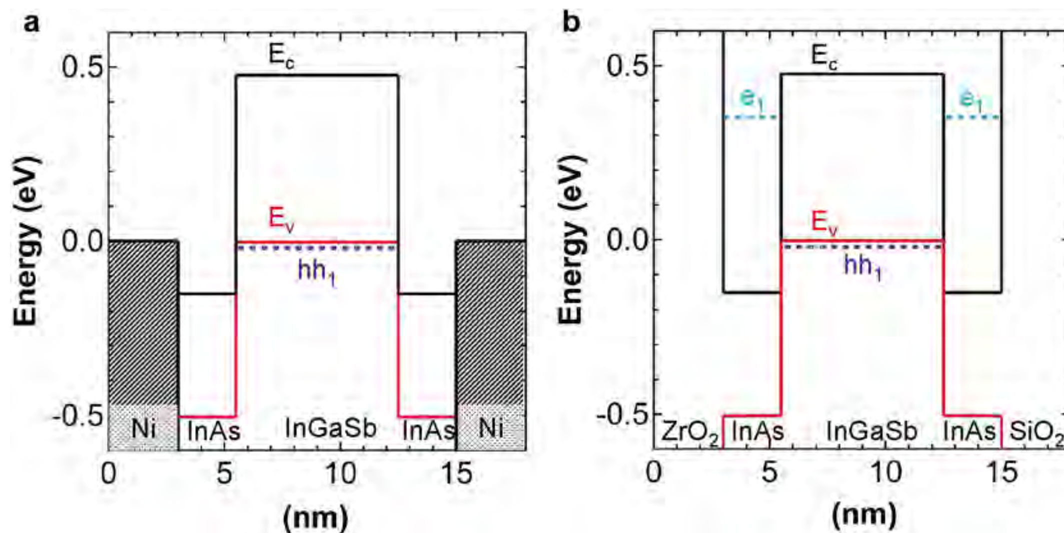


**Figure 2.** Simulated energy band diagrams of InAs/InGaSb/InAs heterostructure XOI. Energy band diagrams under (a) the metal contact and (b) the channel region at the flat band condition. The conduction and valence band edges, $E_c$ and $E_v$, and the ground state of electrons ($e_1$) and heavy holes ($hh_1$) are shown.

One is the region under the source/drain ($S/D$) metal (Ni) contacts where the conduction band of InAs is assumed to be ohmically contacted to the metal.[19] In this case, the electrons in the ultrathin InAs cap are not confined due to ohmic contact to the metal. Holes in InGaSb are partially confined. The InAs/InGaSb interface under the metal contact was found to exhibit a broken gap (i.e., type III) band alignment for the explored InGaSb thickness range (7–15 nm) with the ground state of electrons in InAs being below the ground state of holes in InGaSb (Figure 2a). This "broken gap" band structure results in a semimetallic behavior, thereby, allowing for dopant-free contact to the valence band of InGaSb with relatively low resistances, as discussed later in this paper. The second energy band diagram corresponds to the channel region (Figure 2b). Here, InAs cap layers are in contact with large band gap dielectrics ($ZrO_2$ on the top and $SiO_2$ on the bottom surfaces) which effectively serve as potential barriers for electrons. As a result, the 2.5 nm InAs cap is highly confined. In this case, the InAs/InGaSb exhibits a staggered gap band alignment (i.e., type II), with the ground state of electrons in InAs being above that of the holes in InGaSb. As a result, in this case, the material stack behaves like a conventional quantum-well device, especially for holes which are highly confined in the InGaSb channel. This results in a 2-D hole gas, where the carriers are separated from the surface by the thickness of the InAs cap, likely reducing the severity of surface scattering at the InAs/high-K interface.

The electrical properties of InAs/InGaSb/InAs heterostructure XOI were probed by fabricating back- and top-gated devices. Back-gated p-FETs were fabricated by patterning Ni (thickness, 40 nm) source ($S$) and drain ($D$) contacts. The heavily doped Si substrate was used as the global back-gate with a 50 nm thermally grown $SiO_2$ as the back-gate dielectric. The devices were then capped with ~8 nm $ZrO_2$ by atomic layer deposition (ALD) in order to isolate them from the ambient environment (i.e., humidity and other contaminants). Specifically, $ZrO_2$ was chosen since it has been shown previously that $ZrO_2$/InAs interface exhibits a low density of interface traps.[14] Figure 3a shows representative transfer characteristics of a back-gated InAs/InGaSb/InAs XOI p-FET with an active channel thickness of $T_{InGaSb}$ = 15 nm. Here, the device has a long channel length of $L \sim 3\ \mu$m in order to study the carrier mobility, where diffusive transport is necessary. The effective hole mobility, $\mu_p$, of the device was then extracted as a function of the vertical field (i.e., gate voltage) by using $\mu_p = g_D \times (L/W) \times (1/(C_g(V_{GS} - V_{th})))$, where $g_D = \left.\frac{dI_{DS}}{dV_{DS}}\right|_{V_{GS}}$, $C_g$ is the total gate capacitance in the ON state, $W$ is the channel width measured by scanning electron microscopy (SEM), and $V_{th}$ is the threshold voltage. The gate capacitance can be approximated as $C_g = (1/C_{ox} + 1/C_{InAs} + 1/C_Q)^{-1}$, where $C_{ox}$ is the gate oxide capacitance, $C_{InAs}$ is the capacitance of the InAs cap layer, and $C_Q$ is the quantum capacitance. Based on parallel plate capacitance–voltage ($C$–$V$) measurements, $C_{ox}$ is $\sim 6.9 \times 10^{-8}$ F/cm$^2$ for the 50 nm-thick $SiO_2$ back-gate dielectric. The detailed calculations of $C_Q$ and $C_{InAs}$ are presented in the Supporting Information. For back-gated devices with relatively thick oxides, $C_{ox} \ll C_Q$ and $C_{InAs}$, therefore, $C_g \approx C_{ox}$. The device shows a peak effective mobility of ~820 cm$^2$/(V s) at $V_{DS}$ = −0.1 V (Figure 3b). This hole mobility is better than those of strained Si (~260 cm$^2$/(V s))[20] and unstrained Ge p-FETs (~250 cm$^2$/(V s))[21] and comparable to strained 15 nm-thick Ge (~1000 cm$^2$/(V s))[21] and strained buried 12.5 nm-thick InGaSb on III–V substrates (~1000 cm$^2$/(V s)).[8]

The strain of InGaSb in the InAs/InGaSb/InAs stack layer is calculated to be ~0.65% compressive strain for $T_{InGaSb}$ = 15 nm and up to ~1.05% compressive strain for $T_{InGaSb}$ = 7 nm. For the strain calculations, the lattice constants of InGaSb and InAs cladding layers in the heterostructure are assumed to be identical with a net internal force of zero. Due to the smaller bulk lattice constant of InAs, the InGaSb is compressed, while the InAs cladding layers are stretched. The thickness ratio of the InGaSb and InAs layers affects the final strain in each layer. By controlling the strain, further improvement of mobility may be possible.[8,9] Next, the effect of $T_{InGaSb}$ on the electrical properties of the p-FETs was examined by keeping all other parameters constant. As seen from Figure 3c, the peak effective mobility decreases with the decrease of InGaSb thickness (see Figure S3, Supporting Information for mobility histograms), which may be attributed to the enhanced surface scattering


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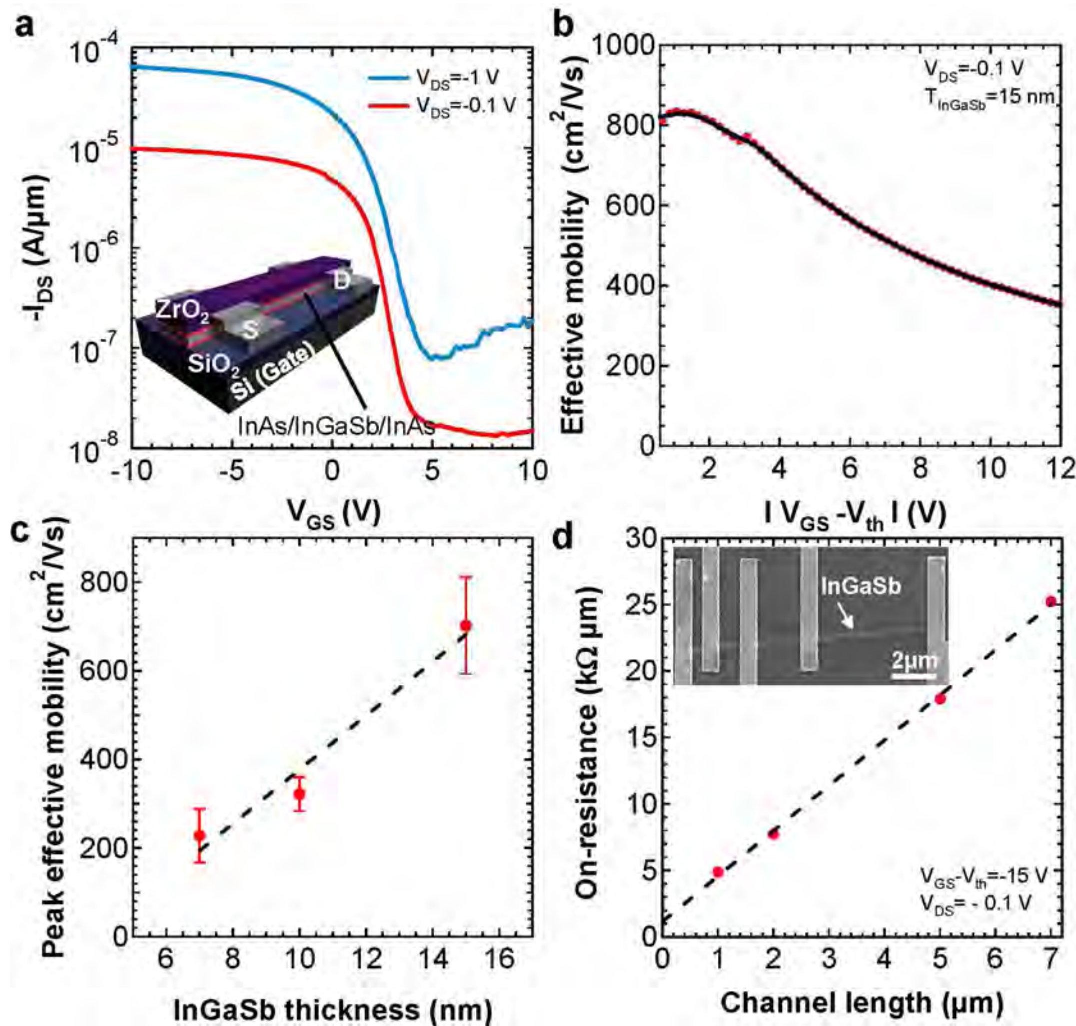


**Figure 3.** Electrical properties of back-gated XOI p-FETs. (a) Experimental transfer characteristics of a back-gated p-FET (50 nm $SiO_2$ gate dielectric) consisting of a single NR with $T_{InGaSb}$ = 15 nm. The inset shows a schematic of the device. (b) The effective hole mobility as a function of the back-gate voltage for the same device, showing a peak mobility of ~820 $cm^2/(V\ s)$ at $V_{DS}$ = −0.1 V. (c) Peak effective mobility as a function of InGaSb thickness, showing mobility reduction with thickness miniaturization. (d) The ON-state resistance as a function of the channel length. A contact resistance of ~580 Ω μm (per *S*/*D* contact) is extracted. The inset shows an SEM image of a single NR contacted with multiple electrodes with different spacing used for the TLM studies.

rates for thinner layers where most of the transport takes place closer to the surface.[22] Note that, as compared to the InAs capped devices, the uncapped InGaSb p-FETs (initial thickness, 20 nm; final thickness after processing, 7.5 nm) exhibit a hole mobility of only 50 $cm^2/(V\ s)$ (Figure S2, Supporting Information), highlighting the importance of the ultrathin InAs cap in obtaining high-performance devices.

Low contact resistance is particularly important when exploring basic carrier transport properties and device performance limits of a new material system. To characterize the contact resistance of our devices, transfer length method (TLM)[23] was utilized. Back-gated p-FETs with channel lengths of $L$ = 1−7 μm (measured by scanning electron microscopy) were fabricated and the ON-resistance at a vertical field of $V_{GS} - V_{th}$ = −15 V was extracted. The $y$-intercept of the ON-resistance versus $L$ (Figure 3d) is approximately equal to $2R_c$, where $R_c$ is the resistance associated with each contact (i.e., *S* or *D*). A contact resistance of ~580 Ωμm is extracted, which is impressive given that both InAs and InGaSb layers are undoped. The low-resistance contacts for holes is enabled by (i) the ease of ohmic contact formation to the conduction band of InAs[24] and (ii) the type-III band alignment of InAs/InGaSb heterojunction[19] underneath the metal contacts. This presents a novel approach for contacting Sb-based semiconductors.[10]

Figure 4a presents the temperature-dependent, $I_{DS} - V_{GS}$ characteristics for a back-gated InAs/InGaSb/InAs XOI FET with $T_{InGaSb}$ = 7 nm. As the temperature is lowered from room temperature to 100 K, $I_{OFF}$ decreases by >2 orders of magnitude. To further investigate the mechanism of the OFF-state leakage current generation, an Arrhenius plot of $I_{OFF}$ (chosen as the minimum current of the $I_{DS} - V_{GS}$ plot) is shown in Figure 4b. An activation energy ($E_A$) of ~0.26 eV is extracted, which is close to half of the bandgap of $In_{0.3}Ga_{0.7}Sb$ at both low and high fields of $V_{DS}$ = 50 and 300 mV. Such activation energy is typically attributed to trap-assisted tunneling and Shockley−Read−Hall generation/recombination. Presumably, trap states at the InAs/InGaSb interface[25] along with unintentional impurities incorporated during the growth result in the observed device leakage current. Thus, the performance of InAs capped InGaSb XOI may be further improved by optimizing the growth.


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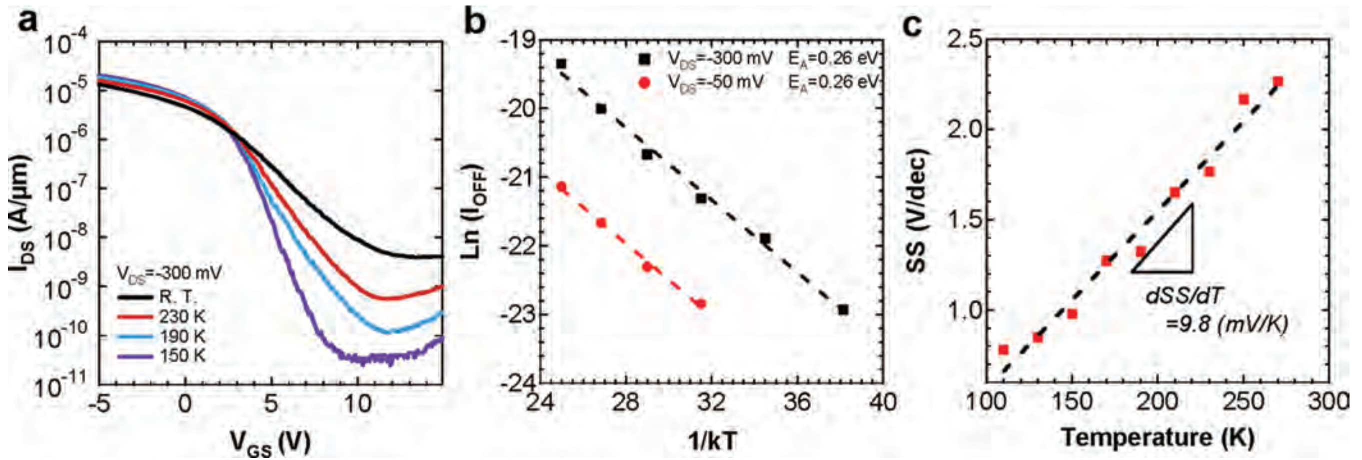


**Figure 4.** Temperature-dependent measurements of back-gated XOI p-FETs. (a) $I_{DS} - V_{GS}$ characteristics as a function of temperature at $V_{DS} = -0.1$ V for a device with $T_{InGaSb}$ = 7 nm. (b) OFF-state current as a function of $1/kT$, showing an activation energy of ∼0.26 eV. (c) Subthreshold swing vs temperature.

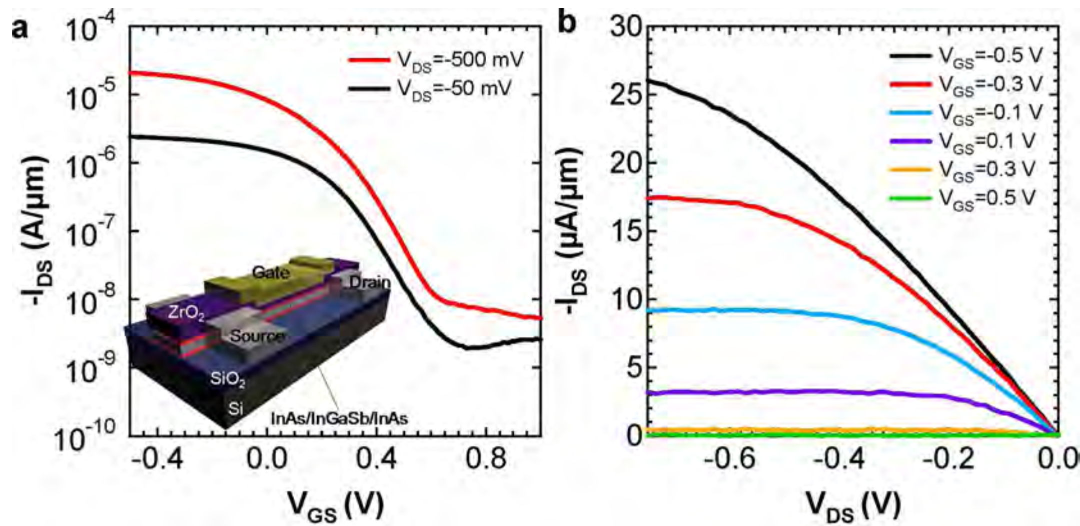


**Figure 5.** Top-gated XOI p-FETs. (a) Transfer and (b) output characteristics of a top-gated (10 nm $ZrO_2$ gate dielectric) InAs/InGaSb/InAs XOI FET with a channel length of ∼6.1 μm and $T_{InGaSb}$ = 7 nm. The Si substrate is grounded during the measurements.

To estimate the density of interface state traps ($D_{it}$), the change of the subthreshold swing (SS) with temperature was fitted with the analytical equation:

$$\frac{dSS}{dT} = \frac{2.3k}{q}\left(1 + \frac{C_{it}}{C_{ox1}} + \frac{C_{InGaSb}}{C_{ox1}} - \frac{\frac{C_{InGaSb}^2}{C_{ox1}C_{ox2}}}{1 + \frac{C_{it}}{C_{ox2}} + \frac{C_{InGaSb}}{C_{ox2}}}\right)$$

where $k$ is Boltzmann constant, $q$ is the electron charge, $C_{it} = q^2D_{it}$ is the interface trap capacitance, and $C_{InGaSb} = \varepsilon_{InGaSb}/T_{InGaSb}$ is the InGaSb body capacitance, $\varepsilon_{InGaSb}$ = 16 is the dielectric constant of InGaSb, and $C_{ox1}$ and $C_{ox2}$ are the capacitances of the active and nonactive gates, respectively (Figure 4c). To model the back gated devices, the equation was evaluated in the limit of $C_{ox2} \to 0$ and $C_{ox1}$ being the back-gate oxide capacitance. This analytical model is valid for an accumulation mode, thin body device,[26] such as the one studied here. The model assumes the carriers are directly beneath the gate, ignoring the finite distance from the surface due to quantization effects. Furthermore, the effect of the quantum capacitance is not considered, which is a valid assumption for our back-gated FETs with a relatively thick back-gate oxide as $C_Q \gg C_{ox}$. The effect of body leakage was also ignored. The $D_{it}$ of the device is determined to be ∼1.4 × $10^{13}$ $cm^{-2}$ $eV^{-1}$, which is similar to most previous reports for Sb-based III–V FETs[27] but higher than the recent report of 3 × $10^{11}$ $cm^{-2}$ $eV^{-1}$ by Nainani, et al.[28]

In a parallel approach, $D_{it}$ was extracted from $C-V$ measurements using the conductance method.[29] For this study, top-gated devices with the gate electrode underlapping the $S/D$ contacts were fabricated with 10 nm of $ZrO_2$ as the gate dielectric (see Supporting Information for detail). The $D_{it}$ using this technique is determined to be ∼2 × $10^{13}$ $cm^{-2}$ $eV^{-1}$, which is consistent with the value obtained from the SS analysis technique presented above, further validating the results. This $D_{it}$ value is comparable to other previously fabricated Sb-based III–V FETs.[27] In the future, interface properties of the InGaSb XOI devices need to be further improved, for example, through the use of surface treatment prior to the gate stack formation and/or optimization of the gate dielectric layer.

Figure 5 shows the representative electrical characteristics of a top-gated p-FET with $T_{InGaSb}$ = 7 nm. Here, the top-gate overlaps the $S/D$ and the channel length is ∼6.1 μm. This long-channel


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device at an operating voltage of $V_{DS} = \Delta V_{GS} = 0.5$ displays $I_{ON}/I_{OFF}$ of ~450 when using $I_{OFF} = 10$ nA. The subthreshold swing is SS ~ 130 mV/decade with a peak transconductance, $g_m$ of ~36 $\mu$S/$\mu$m at $V_{DS} = -0.5$ V. The peak effective hole mobility is ~480 cm$^2$/(V s) (bias dependence of the mobility is shown in Figure S5, Supporting Information) based on the measured gate capacitance of ~$9.5 \times 10^{-7}$ F/cm$^2$ directly obtained from $C-V$ characterization (Figure S4b, Supporting Information). Note that based on the measured $R_c$, the voltage drop at $S/D$ contacts is ~5% at high gate fields, which would lead to a slight underestimation of the extracted mobility. This extracted mobility is higher than that of the back-gated FETs of similar $T_{InGaSb}$ (Figure 3c). The higher mobility of top-gated FETs is attributed to the lower surface scattering rates at the top surface of XOI as compared to the bottom interface. Specifically, the top dielectric ($ZrO_2$) is covalently bonded to the semiconductor surface since it is deposited by ALD, while the bottom dielectric layer ($SiO_2$) is bonded by van der Waals interactions. Overall results here are comparable or better than previously reported InGaSb p-FETs fabricated on GaAs substrates.[8] To test the stability of InGaSb XOI p-FETs, transfer characteristics were measured at $V_{DS} = -0.5$ V over multiple cycles. As evident in Figure S6, Supporting Information, minimal change in the electrical properties is observed even after 2000 cycles of testing. The result is indicative of the high stability of the explored material system. Note that top-gated FETs with $Al_2O_3$ gate dielectric (deposited by ALD) were also fabricated and tested but exhibited worse SS as compared to devices with $ZrO_2$ dielectrics, presumably due to lower interface qualities. Therefore, for all devices here, we utilized $ZrO_2$ gate dielectrics.

In the future, short channel devices need to be explored to better benchmark the performance of InGaSb XOI p-FETs against those of the state-of-the-art Si MOSFETs and InSb quantum well FETs.[18] Scalability of the XOI processing needs to be explored in the future, although recent studies have demonstrated high-yield and large-area layer transfer of various semiconductor thin films onto hard and soft substrates.[30] In addition, materials and device optimization is needed to further enhance the performance of the devices, including the hole mobility. Specifically, the effects of cap material and thickness on the device properties require additional exploration. However, the results shown here present an effective hole mobility enhancement of ~5× over conventional Si p-MOSFETs. Importantly, the employed method may lead to the realization of complementary heterogeneous III–V electronics on Si substrates by utilizing high mobility InGaSb and InAs ultrathin layers as the p- and n-type materials, respectively, through a multistep transfer process.

## ■ ASSOCIATED CONTENT

### Ⓢ Supporting Information

Sample preparation and characterization of InGaSb without InAs capping layers, input parameters for the band diagram calculation, device variation of the mobility, stability of transfer characteristics, capacitance measurements, and $D_{it}$ extraction. This material is available free of charge via the Internet at http://pubs.acs.org.

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### Notes

The authors declare no competing financial interest.

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**Nanoscale InGaSb heterostructure membranes on Si substrates for high hole mobility transistors**

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# Supporting Information

## Sample preparation

Polymethylmethacrylate (PMMA):S1805 (70:30 volume ratio) line-patterns with a pitch and width of ~840 nm and ~350 nm, respectively, were lithographically formed on the MBE grown source substrates, followed by the wet etching of the InAs/InGaSb/InAs stack. Specifically, for the InAs layers, a mixture of citric acid (1g/mL in DI $H_2O$) and hydrogen peroxide (30%) at a volume ratio of (1:20) was used (etch rate, ~1 nm/sec), whereas for the InGaSb layer, a hydrochloric acid (3.7% in DI $H_2O$) and hydrogen peroxide (30%) mixture at a volume ratio of (200:1) was used (etch rate, ~1 nm/sec). Next, the NRs were partially released from the source wafer through the selective wet etching of the AlGaSb sacrificial layer in $NH_4OH$ (1.5 % in DI $H_2O$; etch rate, ~1.8 nm/min). The partially released NRs were picked and transferred to a PDMS (~2 mm thick) slab. A 10 sec HF (1:50 in DI $H_2O$) treatment ensures a high quality interface between InAs and $SiO_2$ by removing any residual AlGaSb from the back surface of the NRs. Subsequently, the layers were transferred onto a Si/$SiO_2$ substrate by the direct contact of PDMS onto the receiver substrate. Finally, the PMMA/S1805 resist layer was stripped in acetone. Note that the $In_{0.3}Ga_{0.7}Sb$ composition is determined after MBE growth using Refection High Energy Electron Diffraction (RHEED) oscillations followed by X-ray measurements on calibration structures.

During device processing, $ZrO_2$ was deposited on the top surface of InAs/InGaSb/InAs XOI layers by atomic layer deposition at 130 ºC by using tetrakis(ethylmethylamido)zirconium precursor and water. The deposition rate was ~1.1Å/cycle. Subsequently, forming gas anneal (5 % $H_2$ in Ar) at 130 ºC for 30 min was performed. The forming gas anneal was found to be critical in improving the InAs/high-κ interface quality, and resulted in a lower *SS*.

## TEM imaging of *uncapped* InGaSb XOI

Figure S1 shows a TEM image of uncapped (i.e., without InAs cladding layers) $In_{0.3}Ga_{0.7}Sb$ XOI, with an original (as-grown) InGaSb thickness of ~20 nm. Due to the high chemical reactivity of InGaSb, the surface is oxidized by up to ~6 nm on each side during the XOI processing, resulting in a final active layer thickness of ~7.5 nm.

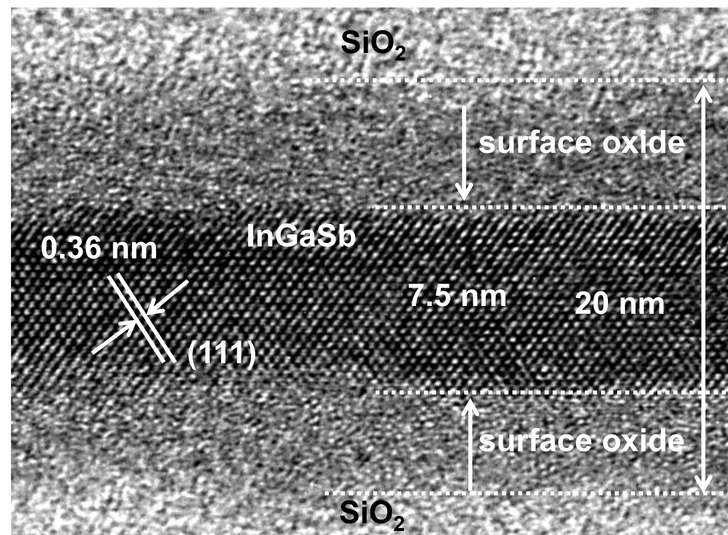


**Figure S1**. A cross-sectional TEM image of an uncapped InGaSb XOI.

## Electrical characteristics of *uncapped* InGaSb XOI *p*-FETs

Representative electrical properties of back-gated, uncapped InGaSb XOI *p*-FETs (active layer thickness of ~7.5 nm with ~6 nm of native oxide on each side) are shown in Fig. S2. After device fabrication, ~8 nm $ZrO_2$ was deposited by ALD as an encapsulation layer. The extracted peak effective mobility is ~ 50 $cm^2/Vs$, which is 3-4x lower than that of 7 nm-thick InGaSb heterostructure XOI *p*-FETs with InAs cap layers ($\mu_p$~200 $cm^2/Vs$, Fig. 3c).

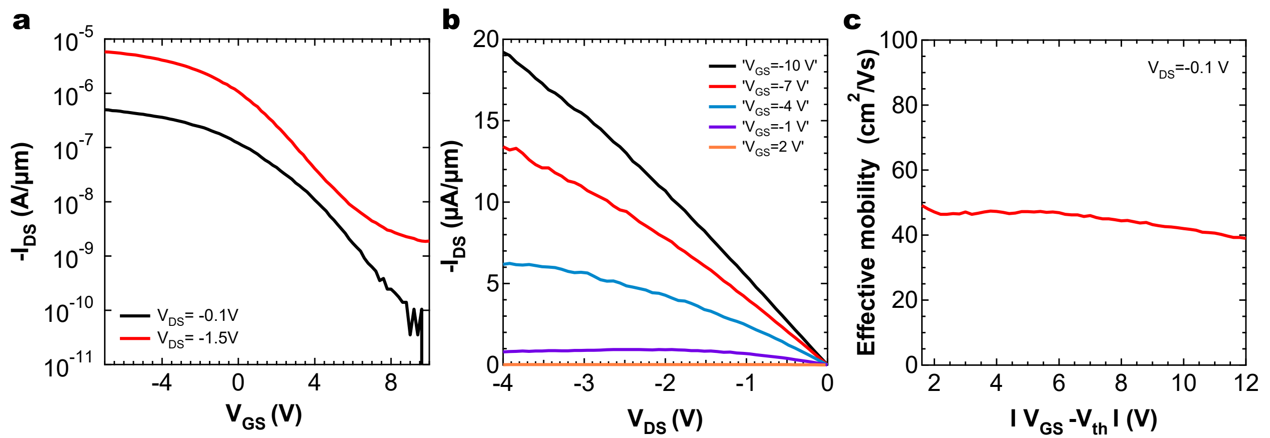


**Figure S2.** Electrical transport properties of a back-gated InGaSb *p*-FET *without* InAs cap layers. The channel length for this device is ~5.5 μm. **a,** Transfer characteristics at $V_{DS}$=-0.1 and -1.5 V, and **b,** $I_{DS}$-$V_{DS}$ curves at different back-gate voltages. **c,** Effective hole mobility as a function of the gate field at $V_{DS}$=-0.1 V.

## Input parameters for the band structure calculations

Conduction band masses for the band diagram calculation using Nextnano are $0.026m_0$, $0.039m_0$ and $0.0135m_0$ for InAs, GaSb and InSb, respectively, where $m_0$ is free electron mass. To match with $In_{0.3}Ga_{0.7}Sb$, the mass was calculated based on the each mass value of GaSb and InSb by Nextnano.

## Device-to-Device Variation of the Mobility of InAs/InGaSb/InAs XOI p-FETs

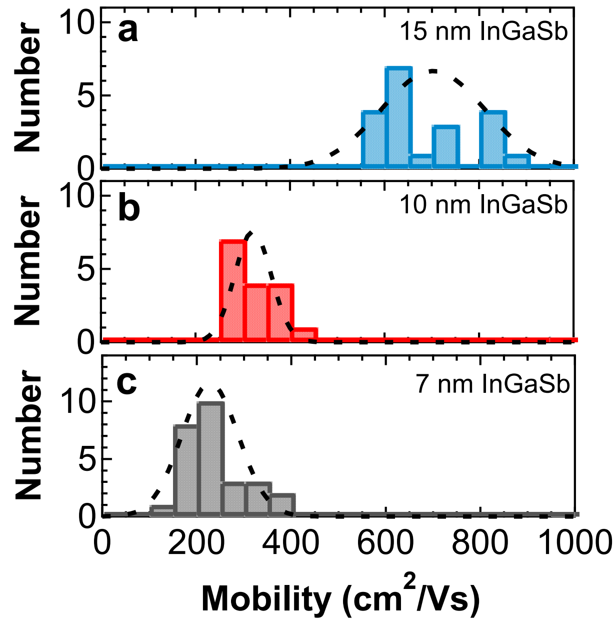


**Figure S3**. Histogram plots of the peak effective hole mobility of **a,** 15 nm-, **b,** 10 nm- and **c,** 7 nm-thick InGaSb back-gated FETs at $V_{DS}$=-100 mV. Standard deviation $\sigma$ is ~109, 38 and 60 cm$^2$/Vs for $T_{InGaAs}$ of 15, 10 and 7 nm, respectively.

## Capacitance-voltage and *Gp/ω*-frequency measurements

In conventional MOSFETs, the body and the S/D contacts are of different polarity, and the ON-state of the device corresponds to the gate voltage regime at which the body is inverted (i.e., inversion regime). In contrast, in the InGaSb XOI p-FETs explored here, the body is p-type and the contacts provide the direct injection of holes into the body. Thereby, the ON-state of the device corresponds to the accumulation regime and the device is OFF under the inversion mode. Thus, although *C-V* characteristics can be measured, direct extraction of the charge density is not possible in the InGaSb XOI FETs. However, through *C-V* and conductance-frequency (*G-f*) measurements, the total gate capacitance, $C_g$, and $D_{it}$ values can be extracted, both of which are valuable device characterization parameters. Specifically, from the measured gate capacitance, the mobility of the XOI devices can be accurately assessed while the extracted $D_{it}$ values provide insight into the interface quality.

The capacitance-voltage (*C-V*) characteristics of top-gated InGaSb XOI devices were measured between the gate (G) and source/drain (S/D) electrodes at 200 K (Fig. S4). Here, $T_{InGaSb}$=7 nm, the S/D spacing is ~5 μm, the gate length is ~3.2 μm, the top dielectric layer is ~10 nm-thick $ZrO_2$, and the bottom oxide is ~1.6 μm-thick $SiO_2$. An underlapped gate geometry was used to reduce the parasitic capacitances between the G and S/D electrodes. To reduce the series resistance of underlapped regions, a global back gate bias of -70 V was applied to the p+ Si substrate during the *C-V* and *G-f* measurements. Figure S4b shows *C-V* characteristics of the device at different frequencies from 5 kHz to 1 MHz. The gate capacitance in the accumulation regime (i.e., ON-state; $V_g$=-2V) was measured to be $C_g$~$9.5\times10^{-7}$ F/cm$^2$ based on the low-frequency (5 kHz) *C-V* data (Fig. S4b). This capacitance value was used to extract the effective mobility of the top-gate devices from the I-V measurements (Fig. S5).

The behavior in the accumulation, depletion and inversion regions of the measured *C-V* (Fig. S4b) is discussed in the following text. The dispersion in accumulation can be accounted for by the frequency dispersion of the dielectric constant of InAs and InGaSb. The gate capacitance in strong accumulation can be approximated as $C_g = (1/C_{ZrO2} + 1/C_{InAs} + 1/C_{Q\text{-}DOS} + 1/C_{Q\text{-}cent})^{-1}$, where the quantum capacitance, $C_{Q\text{-}DOS}$, arises from the density-of-state (DOS) capacitance, and $C_{Q\text{-}cent}$, arises from the charge centroid capacitance. For a single hole subband, $C_{Q\text{-}DOS}$ is calculated from $dQ/dE_f$, where $Q = \int_{-\infty}^{E_v} g(E)d(E)dE$, $g(E)$ is the 2-D density of states, and $f(E)$ is the Fermi function. The capacitance is calculated to be $C_{Q\text{-}DOS} \sim 2.7\times10^{-5}$ F/cm$^2$. Using the SCHRED simulator, the hole charge centroid, $t_{cent}$, was calculated to be ~1.5 nm from the top interface. Using a parallel plate approximation with $\varepsilon_{InGaSb}=16.03$, $C_{Q\text{-}cent} = \frac{\varepsilon_{InGaSb}\varepsilon_0}{t_{cent}} \sim 9.5\times10^{-6}$ F/cm$^2$. The capacitance of the $ZrO_2$/InAs stack was calculated with $t_{InAs}$ = 2.5 nm, $\varepsilon_{InAs}=15.1$, $t_{ZrO2}$ = 10 nm, $\varepsilon_{ZrO2}=16$. The series combination of the $ZrO_2$/InAs gate stack with $C_{Q\text{-}cent}$ and $C_{Q\text{-}DOS}$ gives a calculated low-frequency $C_g$ of $9.7\times10^{-7}$ F/cm$^2$ in strong accumulation, which is in good agreement with the measured capacitance value of ~$9.5\times10^{-7}$ F/cm$^2$ (Fig. S4b). In the inversion region, the dispersion is due to the lack of a contact to the conduction band. Thus, as in a conventional MOS capacitor, the electrons are unable to respond to the high-frequency signal, causing the dispersion observed. The feature at $V_g$ ~1.5 V is attributed to inversion of the heavily quantized InAs capping layer.

In addition, *G-f* measurements were also carried out to extract $D_{it}$ values for the present device using the conductance method[1]. To extract $D_{it}$ from the measured conductance ($G_m$) and capacitance ($C_m$) values, we first extract the series resistance ($R_s$) by using equation (1) as a function of excitation frequency $\omega = 2\pi f$.

(1) $$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2}$$

Here, $C_{ma}$ and $G_{ma}$ are the measured capacitance and conductance in strong accumulation respectively. Then, the series resistance correction factor ($a$) was calculated using equation (2).

(2) $$a = G_m - (G_m^2 + \omega^2 C_m^2) R_s$$

The corrected conductance ($G_c$) and capacitance ($C_c$) were then calculated from equations (3) and (4), respectively.

(3) $$G_c = \frac{(G_m^2 + \omega^2 C_m^2) a}{a^2 + \omega^2 C_m^2}$$

(4) $$C_c = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{a^2 + \omega^2 C_m^2}$$

Finally, $G_p/\omega$ was calculated using equation (5), and the $D_{it}$ was extracted by taking the maximum $G_p/\omega$ for a given gate voltage in equation (6).

(5) $$\frac{G_p}{\omega} = \frac{\omega G_c C_{ox}^2}{G_c^2 + \omega^2 (C_{ox} - C_c)^2}$$

(6) $$D_{it} = \frac{2.5}{q} \frac{G_p}{\omega}$$

Figure S4c shows the calculated $G_p/\omega$ vs frequency. The $D_{it}$ of the device is extracted to be ~$2\times10^{13}$ $cm^2/Vs$.

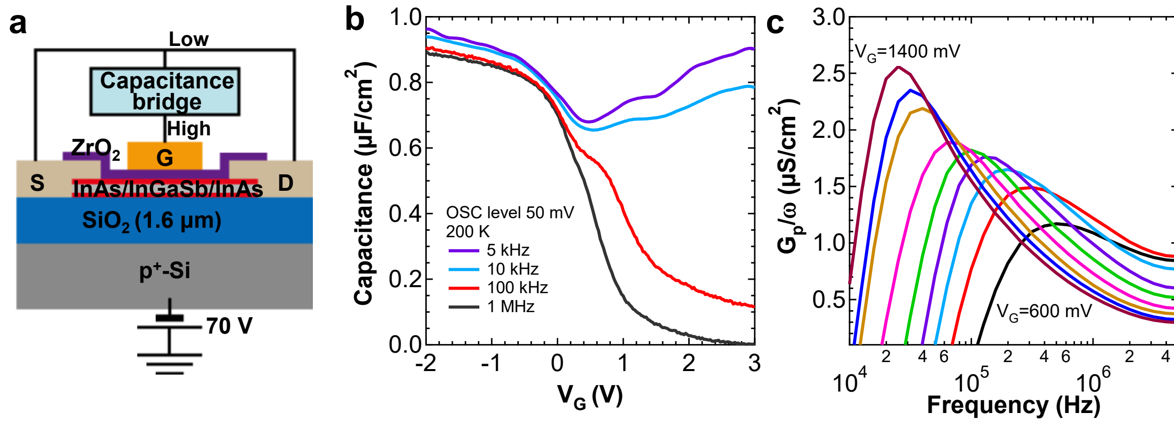


**Figure S4. a,** Device schematic used for the C-V and conductance measurements. **b,** Measured *C-V* curves at different frequencies (5 kHz-1 MHz) at a sample temperature of 200 K. **c,** $G_p/\omega$-$f$ curves used to extract the surface state $D_{it}$.

## Effective Hole Mobility of Top-Gated InGaAs XOI FETs ($T_{InGaSb}$ = 7 nm)

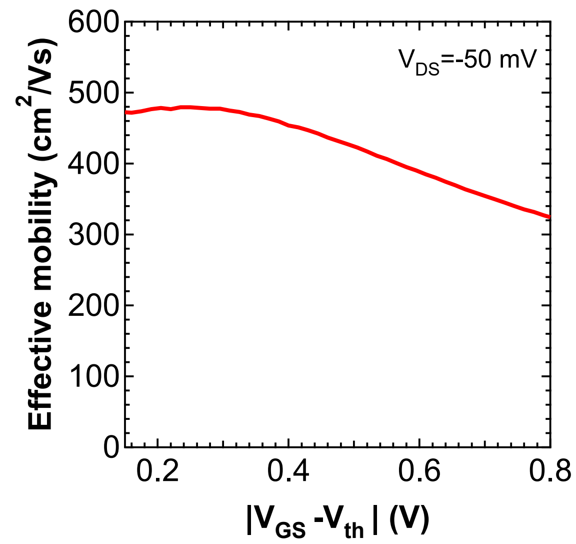


**Figure S5.** Effective mobility as a function of the gate field for a 7 nm-thick InGaSb XOI *p*-FET. The result is for the same device shown in Fig. 5.

## Stability of top-gated InGaSb XOI FETs

Figure S6 shows the $I_{DS}$-$V_{GS}$ curves of a 7 nm-thick InAs/InGaSb/InAs top-gated FET after multiple cycles of measurement, up to 2000 times, at $V_{DS}$=-0.5 V. The device is highly stable with minimal change in the device characteristics over multiple cycles of operation.

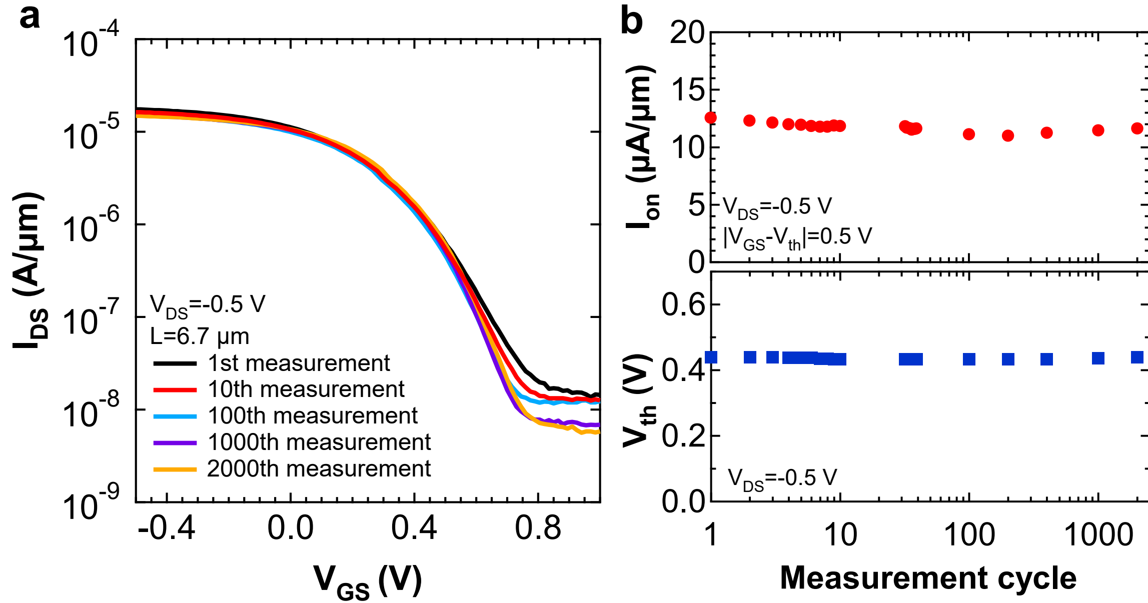


**Figure S6**. **a,** Transfer characteristics of a top-gated device after multiple cycles of measurements at $V_{DS}$=-0.5 V. **b,** $I_{ON}$ at $| V_{GS}-V_{th}|$ =0.5 V and **c,** $V_{th}$ as a function of measurement cycle at $V_{DS}$=-0.5 V.

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