Integration of Nanoelectromechanical Relays With Silicon nMOS

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***Abstract*—Electrostatically actuated nanoelectromechanical (NEM) relays are integrated with silicon nMOS devices. An nMOSFET successfully drives a NEM relay with the MOSFET serving as a pass transistor to control the state of the relay. Silicon MOSFET-NEM relay integration opens up the possibility for applications, where the zero OFF-state leakage, the sharp on/off transition, and/or the hysteresis of the NEM relay can be used to complement the capabilities of CMOS.**

***Index Terms*—Microelectromechanical devices, MOSFETs, nanotechnology, relay.**

I. Introduction

THREE terminal nanoelectromechanical (NEM) relays [see Fig. 1(d)] operate similarly to CMOS transistors, with the current flow between the source and the drain terminals controlled by gate biasing. However, they differ in that they have: 1) zero OFF-state leakage, with all three terminals separated by an air gap in the OFF-state; 2) sharp on/off transition, determined by the making and breaking of the contact between the source and the drain; and 3) hysteresis, with the turn-on voltage (pull-in voltage $V_{\rm pi}$) being larger than the turn-off voltage (pull-out voltage $V_{\rm po}$) [1], [2]. With standby power of CMOS circuits already optimized to be comparable to the active power with device scaling [3], the first two properties make NEM relays attractive devices for low standby power applications. However, the replacement of all CMOS transistors with NEM relays is problematic because the turn-on speed of relays is limited by the mechanical movement of the beam. The switching speed of fabricated relays have been measured to be on the order of 100 ns [2], [4], whereas that of scaled NEM relays is projected to be on the order of 1 ns [5]. This is still at least 10^3 times slower than current CMOS devices [6]. Therefore, applications have been proposed, where a combination of NEM relays and CMOS is used to capitalize on the benefits of each. These include power gating using MEMS switches (50% battery life increase expected) [7], CMOS-NEM field-programmable gate array (37% leakage power and 28% critical path delay reduction expected) [8], and CMOS-NEM static random access memory (85% static power, 60% write delay, and 10% read delay reduction expected) [1].

To realize the proposed hybrid CMOS-NEM relay applications, CMOS and electrostatically actuated NEM relays must function together, integrated on the same chip. Low-temperature CMOS-compatible processes for fabricating NEM relays have been reported [2], [4], including actual fabrication of contacting switches in the CMOS back-end-of-line [9]. However, experimental demonstrations of interaction between CMOS and integrated M/NEMS have been limited to contact-

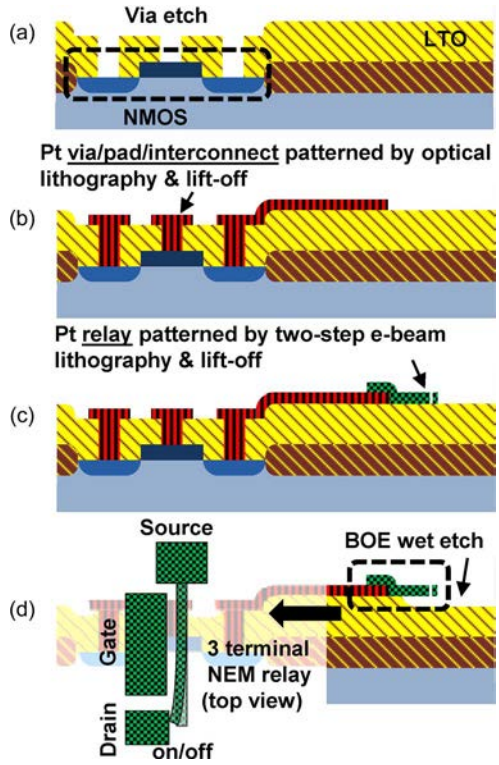

Fig. 1. Process flow of the NEM relay nMOS integration. (a) LTO deposition on a preprocessed nMOS and via etch. (b) Pt via, pad, and interconnect patterned by optical lithography and liftoff. (c) Pt NEM relay and relay-to-pad/interconnect connection patterned by e-beam lithography and liftoff. (d) RTA at 300 °C, followed by 6 : 1 BOE wet etch and CPD. A top view of the laterally actuated three-terminal NEM relay is shown in the OFF- and ON-states.

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less MEMS devices [10], [11] and thermally actuated resistive switches [12]. This paper demonstrates, for the first time, electrical interaction between an integrated silicon MOSFET and an electrostatically actuated NEM relay, where the NEM relay is fabricated at CMOS-compatible temperatures, and the MOSFET and the NEM relay operate at the same voltages, opening up the possibility of realizing NEM-CMOS hybrid circuits.

II. NEM Relay Fabrication on CMOS

Laterally actuated platinum (Pt) relays are fabricated using e-beam lithography on top of the nMOS fabricated at the Stanford Nanofabrication Facility. The nMOS has a minimum gate length of 1 μm and a supply voltage of around 5 V. A silicon MOS technology capable of a relatively high power supply voltage is used so that the same supply voltage is used for both the MOSFETs and the NEM relays (whose supply voltage scaling is currently limited by lithographical limits). As relays continue to scale to sub-1 V actuation voltages with gap sizes on the order of 10 nm [2], [5], conventional MOSFETs with 1 V power supply can be used.

Details of the process flow (see Fig. 1) are as follows. A low-temperature oxide (LTO) passivation layer is deposited on top of unpassivated silicon MOSFETs, where via holes are etched to contact the MOSFET electrodes. Using optical lithography and Pt sputter deposition (with Ti adhesion layer) followed by liftoff, the vias, interconnects, and pads are simultaneously formed. Then, the NEM relays are fabricated using e-beam lithography and 60-nm Pt evaporation deposition (with a 5-nm Ti adhesion layer) followed by liftoff. Because a highly anisotropic deposition is required for liftoff of small features, evaporation is chosen as the suitable deposition method. However, as a result of it being anisotropic, a step is formed between the NEM relay and the pads/interconnects, which can result in an open circuit. Thus, a second e-beam liftoff process with Pt sputtering deposition (which is a more isotropic deposition method) around this step is performed to ensure good electrical connection. These lithography steps are followed by a 2-min rapid thermal anneal (RTA) at 300 °C, which allows the beam to remain horizontally flat after release. Without this step, the stress gradient of the Pt beam causes the beam to curl up upon release. Finally, a 1-min timed oxide etch in 6:1 buffered oxide etch (BOE) is performed to release the beam, followed by critical point drying (CPD) to avoid stiction. The fabricated relay has a beam width of approximately 80 nm, a beam-to-gate gap of approximately 100 nm, and a beam length of approximately 3.5 μm (see Fig. 2).

Although the NEM relay is on a layer above Si MOSFETs, it is currently not placed directly over the MOSFETs because a flat surface is needed for e-beam lithography. Area reduction by stacking relays directly above MOSFETs can be achieved with an additional chemical–mechanical polishing (CMP) step to planarize the surface before relay fabrication.

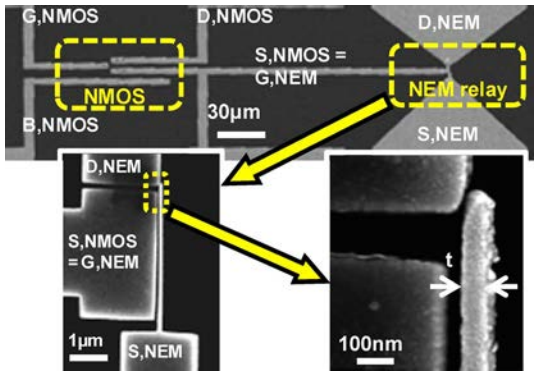

Fig. 2. Scanning electron microscope image of a NEM relay fabricated on an nMOS. Zoomed-in image shows the NEM relay with ∼80 nm beam thickness (t) and ∼ 3.5 μm beam length.

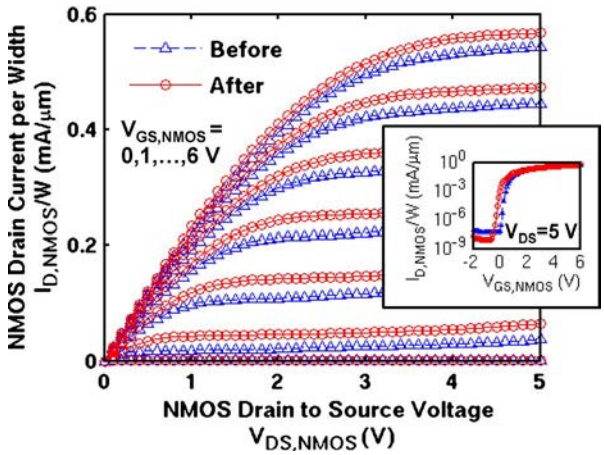

Fig. 3. $I_{D,\mathrm{nMOS}}$ versus $V_{DS,\mathrm{nMOS}}$ before and after NEM relay fabrication by postprocessing, sweeping $V_{GS,\mathrm{nMOS}}$. The nMOS transistor is shown to be functional, with good gate control. (Inset) $I_{D,\mathrm{nMOS}}$ versus $V_{GS,\mathrm{nMOS}}$ shows a V_{TH} shift of ∼0.3 V.

III. Results and Discussion

Successful integration of NEM relays with nMOS transistors must demonstrate the following: 1) the functionality of nMOS transistors after postprocessing of NEM relays, 2) the capability of the nMOS transistors to electrically bias the NEM relays, and 3) the functionality of the NEM relays.

The nMOS is tested after NEM relay fabrication, and the $I_{D,\mathrm{nMOS}} - V_{DS,\mathrm{nMOS}}$ characteristics (see Fig. 3) confirm that the nMOS maintains functionality and good gate control even after processing, although the threshold voltage shifted by approximately 0.3 V (see Fig. 3 inset). The nMOS characteristics show changes throughout the processing steps, but no apparent trend has been observed, requiring further investigation.

The test setup used to demonstrate the combined functionality of the NEM relay and nMOS is shown in Fig. 4(a). The nMOS serves as a pass transistor and drives the gate of the NEM relay. When the nMOS is turned off (with $V_{GB,\mathrm{nMOS}} = 0$), S,nMOS (or G,NEM) becomes a floating node, leaving the NEM relay in the OFF-state (the capacitance of the floating node, dominated by the pad capacitance, is on the order of 1 pF). When the nMOS is turned on (with $V_{GB,\mathrm{nMOS}} = 6\ \mathrm{V} \sim (V_{DD} + V_{\mathrm{TH,nMOS}})$), S,nMOS (or G,NEM) charges/discharges to $V_{DB,\mathrm{nMOS}}$. When $V_{DB,\mathrm{nMOS}} > V_{\mathrm{pi}}$,

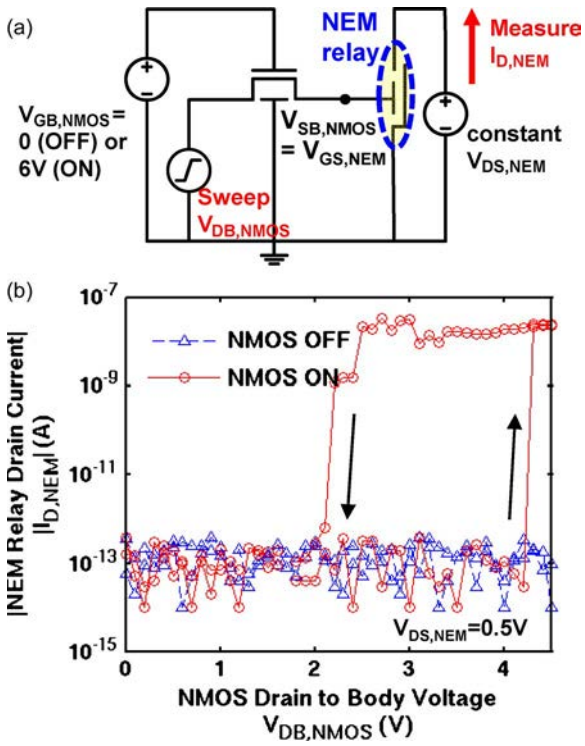

Fig. 4. (a) Test setup to demonstrate successful NEM relay–nMOS integration, with the nMOS serving as a pass transistor. When the nMOS is turned off, S,nMOS (or G,NEM) becomes a floating node, leaving the NEM relay in the OFF-state. When the nMOS is turned on, $V_{DB,\mathrm{nMOS}}$ is passed onto $V_{SB,\mathrm{nMOS}} = V_{GS,\mathrm{NEM}}$. A double sweep of $V_{DB,\mathrm{nMOS}}$ turns the NEM relay on/off, which can be detected by measuring $I_{D,\mathrm{NEM}}$. (b) $I_{D,\mathrm{NEM}}$ versus $V_{DB,\mathrm{nMOS}}$ with $V_{DS,\mathrm{NEM}} = 0.5$ V. When $V_{GB,\mathrm{nMOS}} = 0$, the NEM relay stays in the OFF-state, whereas when $V_{GB,\mathrm{nMOS}} = 6$ V, $V_{DB,\mathrm{nMOS}}$ is passed onto $V_{SB,\mathrm{nMOS}} = V_{GS,\mathrm{NEM}}$, and the NEM relay actuates with $V_{\mathrm{pi}} = 4.3$ V and $V_{\mathrm{po}} = 2.1$ V.

the beam actuates, and current flows between the drain and the source of the NEM relay $(I_{D,\mathrm{NEM}})$. $V_{DS,\mathrm{NEM}} < V_{DD}$ is applied because the contacts are susceptible to failure when a high bias is applied between the contacts. This issue needs to be resolved for the suggested hybrid circuits [1], [7], [8] to be realized.

The $I_{D,\mathrm{NEM}} - V_{DB,\mathrm{nMOS}}$ characteristics [see Fig. 4(b)] demonstrate successful integration of NEM relays with the nMOS. When the nMOS is turned off, the relay does not actuate. However, when the nMOS is turned on, the relay turns on at $V_{DB,\mathrm{nMOS}} = 4.3$ V (cf. 2-D simulated V_{pi} of 4.8 V [1]) and turns off at $V_{DB,\mathrm{nMOS}} = 2.1$ V with $V_{DS,\mathrm{NEM}} = 0.5$ V. The test was repeatable up to eight cycles (with $V_{DS,\mathrm{NEM}} = 0.1$ or 0.5 V) with consistent V_{pi} and varying V_{po}. The beam failed to pull out on the 9th cycle but was functional on the next cycle.

The leakage current in the OFF-state is a few hundred fA (noise level of the measurement setup). The turn-on and -off transitions are abrupt, changing by 46 orders of magnitudes, when measured in 100-mV steps. Finer voltage steps of 5 mV shows an inverse subthreshold slope of approximately 0.8 mV/dec, limited by the noise level of the measurement setup.

Two main issues need further study, including high contact resistance (on the order of 10 MΩs) and limited reliability of the NEM relay. Previous works using different materials and/or structures have shown < 3 kΩ ON-resistance with $> 10^8$ cycles [13] and < 100 kΩ ON-resistance with $> 10^9$ cycles [2], suggesting that gaining further fundamental understanding of material issues coupled with optimized mechanical design may lead to a satisfactory solution.

IV. Conclusion

This paper presents the first experimental demonstration of integrated MOSFET-electrostatically actuated NEM relay electrical data, opening up the possibility of realizing circuits that have low leakage without loss of speed by combining NEM relays and CMOS. After NEM relay fabrication by post-processing on Si nMOS, the functionality of the MOSFET, the capability of the nMOS transistor to electrically bias the NEM relay, and the functionality of the NEM relay are successfully demonstrated by electrical results. To realize useful NEM relay-CMOS integrated circuits, further work needs to be done to enhance the reliability and to decrease the contact resistance of the relays.

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