Design Requirements for Steeply Switching Logic Devices

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***Abstract*—Many steeply switching logic devices have recently been proposed to overcome the energy efficiency limitations of CMOS technology. In this paper, circuit-level energy–performance analysis is used to derive the design requirements for these alternative switching devices. Using a simple analytical approach, this paper shows that the optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ ratios are set only by circuit-level parameters as well as the device transfer characteristic OFF-state $S_{\rm off}$, ON-state $S_{\rm on}$, and effective $S_{\rm eff}$ inverse slopes. For a wide variety of switching device characteristics and circuit parameters, the optimal $E_{\rm dyn}/E_{\rm leak}$ ratio is approximately $(K/2)(S_{\rm eff}/S_{\rm off}) - 0.56(S_{\rm on}/S_{\rm off}) - 0.56$, where K ranges from 6.23 to 11.9. Based upon this theoretical framework, simple requirements for $S_{\rm off}$, $S_{\rm on}$, and $S_{\rm eff}$ are established in order for an alternative switching device to be more energy efficient than a MOSFET. The results reemphasize that merely focusing on achieving the steepest local inverse slope S is insufficient, since energy dissipation is set mainly by $S_{\rm eff}$ and not by S. Finally, the general shape of the energy–delay curve is also set by these inverse slopes, with its steepness directly proportional to $S_{\rm on}/S_{\rm off}$. This analytical approach provides a simple method to assess the promise of any new device technology in potentially overcoming the energy efficiency limitations of CMOS technology.**

***Index Terms*—Low power electronics, subthreshold slope, transistor, 60 mV/dec.**

I. Introduction

MOSFET scaling has led to dramatic improvements in integrated-circuit functionality and speed along with reductions in cost and energy per function. However, the nonscalability of the thermal voltage and hence the transistor threshold voltage V_T have now led to a power crisis. Specifically, due to the inability to scale V_T, in the most recent generations of CMOS technology, the supply voltage $V_{\rm dd}$ has remained relatively constant. As a result, chip power consumption has increased along with transistor count [1], [2], and because of practical limits for heat dissipation, power density constraints now pose a serious challenge for CMOS chip design.

To increase transistor density without increasing power density, $V_{\rm dd}$ must be reduced. Ideally, voltage scaling should not come at the expense of switching performance, gauged by the ON-state drive current to OFF-state leakage current ratio $I_{\rm on}/I_{\rm off}$. For this reason, alternative switching device designs that can potentially achieve higher $I_{\rm on}/I_{\rm off}$ than the MOSFET at low $V_{\rm dd}$ have been proposed. The proposed devices include tunneling transistors (TFETs) [3]–[11], impact-ionization MOS (IMOS) devices [12], [13], MOSFETs with nanoelectromechanical gate electrodes (NEMFETs) [14]–[16], nanoelectromechanical (NEM) relays [18], ferroelectric FETs [19], [20], and feedback FETs [21], all of which can achieve a local subthreshold swing below 60 mV/dec at room temperature. However, many of these devices exhibit this steep switching behavior only across a small range of currents. Furthermore, some of these devices (e.g., NEMFET [14], [15], NEM relays [17], [18], and IMOS [13]) do not begin to conduct current until sometime after the gate turn-ON voltage is applied, resulting in an additional component of delay.

Despite the fact that many such alternative devices have been proposed, relatively few studies [1], [5], [22] have been carried out to predict the potential energy–delay benefits of using these devices (as opposed to standard MOSFETs) in digital circuits. To assess the potential energy benefits, as well as the range of performance over which such benefit is sustained, a circuit-level energy–delay comparison is needed. To set the background for this comparison, this paper first reviews the energy–performance tradeoffs for generic digital logic devices. As the analysis will show, the energy–performance optimization results in requirements on the values of $I_{\rm on}/I_{\rm off}$ and dynamic energy to leakage energy ratio $E_{\rm dyn}/E_{\rm leak}$ for an alternative switching device to provide an advantage over the MOSFET. These values can be expressed by a simple analytical equation that only depends on the circuit's topology (as shown in previous works [23]–[26]) and the steepness and shape of the device's switching characteristic. The advantage of the analytical approach taken here (versus the simulation based approaches used in previous studies) is that it elucidates the dependences of the optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ on the shape of the device transfer characteristic (log I_d versus $V_{\rm gs}$). This result can be used to derive requirements for an alternative switching device to be more energy efficient than a MOSFET. Furthermore, the general shape of the energy–delay curve can be obtained in a straightforward manner to determine the performance range over which the alternative switching device is advantageous.

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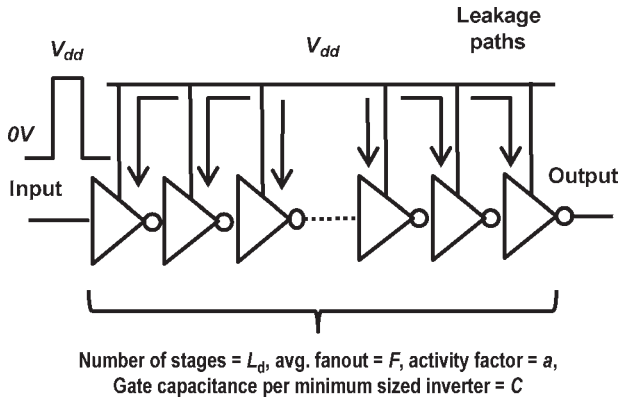

Fig. 1. L_d stage inverter chain used to assess relative energy–delay performance.

II. Energy–Delay Tradeoffs for Digital Logic

This section reviews the energy–delay tradeoff in digital logic circuits to provide the theoretical framework for subsequent discussion of requirements and implications for alternative switching devices.

The tradeoff between energy and delay for the majority of digital logic gates on a chip is similar to that of an inverter. Therefore, at least for switching devices that similarly behave to MOSFET, a representative comparison of energy–delay characteristics can be made using a simple inverter chain (Fig. 1). The total energy consumed per operation by an inverter chain with logic depth L_d, average activity factor a, electrical fanout F, and capacitance per stage C can be computed by adding the dynamic and leakage energy components

$$E = E_{\rm dyn} + E_{\rm leak} = aL_dFCV_{\rm dd}^2 + L_dFI_{\rm off}V_{\rm dd}t_{\rm delay}. \quad (1)$$

For devices with MOSFET-like output characteristics, the propagation delay through L_d stages is

$$t_{\rm delay} = \frac{L_dFCV_{\rm dd}}{2I_{\rm on}} \quad (2)$$

where $I_{\rm on}$ is approximately the drain-to-source current per stage[1] at $V_{\rm gs} = V_{\rm dd}$, $V_{\rm ds} = V_{\rm dd}$ [27], and $I_{\rm off}$ is the drain-to-source current per stage $V_{\rm gs} = 0$ V and $V_{\rm ds} = V_{\rm dd}$.

For switching devices that have nonsaturating or weakly saturating output characteristics (i.e., whose drain current significantly varies as $|V_{\rm ds}|$ varies from $V_{\rm dd}$ to $V_{\rm dd}/2$), the effective ON-state current $I_{\rm eff}$ rather than $I_{\rm on}$ should be used in delay estimation [27]–[30]. Assuming $I_{\rm eff}$ is set by $I_{\rm on}$ through a linear scaling parameter γ_I, the switching delay is

$$t_{\rm delay} = \frac{L_dFCV_{\rm dd}}{2I_{\rm eff}} = \gamma_I\frac{L_dFCV_{\rm dd}}{2I_{\rm on}}, \quad \text{where } I_{\rm eff} = I_{\rm on}/\gamma_I. \quad (3)$$

Finally, some devices (e.g., NEMFET [14], [15] and IMOS [12], [13]) do not begin to conduct current until sometime after the gate turn-ON voltage is applied. This causes an additional component of delay referred to herein as the setup delay $t_{\rm su}$[2]

$$t_{\rm delay} = t_{\rm RC} + t_{\rm su} \approx \frac{L_dFCV_{\rm dd}}{2I_{\rm on}}(1+\gamma_{\rm su}), \quad \text{where } \gamma_{\rm su} \equiv t_{\rm su}/t_{\rm RC}. \quad (4)$$

Using equations (2)–(4), the propagation delay can therefore be expressed in a general form

$$t_{\rm delay} \approx \gamma\frac{L_dFCV_{\rm dd}}{2I_{\rm on}} \quad (5)$$

where γ is a linear fitting parameter that accounts for nonideal effects.

An energy–delay optimal design minimizes the energy dissipation (1) subject to a given delay target (4). For CMOS circuits, dynamic energy is reduced quadratically by decreasing $V_{\rm dd}$ linearly. To avoid increasing delay, V_T must be decreased along with $V_{\rm dd}$ to maintain constant ON-state drive resistance (i.e., the ratio between supply voltage and ON-state current $V_{\rm dd}/I_{\rm on}$) [1], [22]–[24], but this results in increased $I_{\rm off}$ and hence increased leakage energy. Alternative switching devices that are MOSFET-like [2]–[16], [19]–[21] also typically have an equivalent "threshold voltage," and in this analysis, it is assumed that device designers can freely adjust this parameter (e.g., by adjusting the gate work function) to directly tradeoff the ON-state drive current for reduced OFF-state leakage current.[3] As derived in Appendix I, a closed-form solution exists for this constrained optimization problem, which results in several switching device requirements that are discussed in the following sections.

III. Optimization of $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ Ratios

The optimal tradeoff between energy and delay is achieved by selecting $V_{\rm dd}$ and V_T to minimize the energy dissipation for a given delay, i.e., to achieve an optimal balance between dynamic energy and leakage energy. As derived in Appendix I, a generalized switching device design is optimized if $I_{\rm on}/I_{\rm off}$ satisfies the following condition:

$$\frac{I_{\rm on}}{I_{\rm off}} = -\gamma\frac{L_dF}{4a}\frac{S_{\rm eff}}{S_{\rm off}}lambertW\left(-\frac{4a}{\gamma L_dF}\frac{S_{\rm off}}{S_{\rm eff}}\exp\left(\frac{S_{\rm off}+S_{\rm on}}{S_{\rm eff}}\right)\right) = \beta\frac{\gamma L_dF}{4a} \quad (6)$$

where $\beta \equiv -(S_{\rm eff}/S_{\rm off})lambertW(-4a/(\gamma L_dF)\times(S_{\rm off}/S_{\rm eff})\times\exp((S_{\rm off}+S_{\rm on})/S_{\rm eff}))$, and $x = lambertW(y)$ is the solution to the equation $y = xe^x$, and the parameters $S_{\rm on}$,

[1] In comparing the energy–delay tradeoff, we assume the same widths for different logic devices.

[2] Note that $t_{\rm su}$ and $t_{\rm RC}$ would likely scale differently with $V_{\rm dd}$. However, since this paper aims to provide a simple analytical formulation for assessing the promise of any alternative switching device, a constant $\gamma_{\rm su}$ is assumed to greatly simplify the derivation. As the next section will show, the optimal $I_{\rm on}/I_{\rm off}$ linearly increases with increasing γ, whereas the optimal $E_{\rm dyn}/E_{\rm leak}$ is almost independent of γ; therefore, so long as γ does not greatly vary within a range of $V_{\rm dd}$ and V_T, the final results are typically insensitive to this simplifying assumption.

[3] A notable exception is a switching device that has zero OFF-state current, e.g., a relay. The energy efficiency of such a device is limited by other factors, and hence, the analysis in this paper is not directly applicable to a relay.

$S_{\rm off}$, and $S_{\rm eff}$ are the inverse slopes in the ON-state ($V_{\rm gs}=V_{\rm dd}$ and $V_{\rm ds}=V_{\rm dd}$), OFF-state ($V_{\rm gs}=0$ V and $V_{\rm ds}=V_{\rm dd}$), and overall, respectively, i.e.,

$$S_{\rm off}\equiv\left(\left.\frac{\partial log_{10}I_d}{\partial V_{\rm gs}}\right|_{V_{\rm gs}=0}\right)^{-1},$$
$$S_{\rm on}\equiv\left(\left.\frac{\partial log_{10}I_d}{\partial V_{\rm gs}}\right|_{V_{\rm gs}=V_{\rm dd}}\right)^{-1},\quad S_{\rm off}\equiv\frac{V_{\rm dd}}{log_{10}(I_{\rm on}/I_{\rm off})}. \tag{7}$$

Because $lambertW(y)\approx 1.1155\times ln(-y)-1.093$, as also detailed in Appendix I, the optimal $I_{\rm on}/I_{\rm off}$ ratio can be approximated by

$$\frac{I_{\rm on}}{I_{\rm off}}\equiv\beta\frac{L_d\cdot F\gamma}{4a}$$
$$\cong\gamma\frac{L_d\cdot F}{4a}\left[\left(1.1155\ln\left(\gamma\frac{L_dF}{4a}\frac{S_{\rm eff}}{S_{\rm off}}\right)+1.093\right)\frac{S_{\rm eff}}{S_{\rm off}}-1.1155\frac{S_{\rm on}}{S_{\rm off}}-1.1155\right] \tag{8a}$$
$$=\gamma\frac{L_d\cdot F}{4a}\left(K\frac{S_{\rm eff}}{S_{\rm off}}-1.1155\frac{S_{\rm on}}{S_{\rm off}}-1.1155\right) \tag{8b}$$

where $K=1.1155\ln(\gamma L_dF/(4a)\times(S_{\rm eff}/S_{\rm off}))+1.093$, which ranges from 6.23 to 11.9 for $100<\gamma L_df/(4a)\times(S_{\rm eff}/S_{\rm off})<10\,000$. Thus, the optimum value of $I_{\rm on}/I_{\rm off}$ primarily depends on the circuit topology as well as $S_{\rm on}/S_{\rm off}$ and $S_{\rm eff}/S_{\rm off}$, which are measures of the relative steepness of the device transfer characteristic.[4]

With this optimal current ratio, $E_{\rm dyn}/E_{\rm leak}$ can be estimated by rewriting the total energy dissipation per operation (1) as

$$E=aL_dFCV_{\rm dd,opt}^2\left(1+\gamma\frac{L_dF}{a}\frac{I_{\rm off}}{2I_{\rm on}}\right)$$
$$=aL_dFCV_{\rm dd,opt}^2\left(1+\frac{2}{\beta}\right) \tag{9}$$

where $V_{\rm dd,opt}$ is the supply voltage for which the performance target is achieved with minimum total energy: $V_{\rm dd,opt}=S_{\rm eff}\times\log_{10}(I_{\rm on}/I_{\rm off})$. Therefore, the optimal $E_{\rm dyn}/E_{\rm leak}$ can readily be obtained as

$$\frac{E_{\rm dyn}}{E_{\rm leak}}=\frac{a}{\gamma L_dF}\frac{2I_{\rm on}}{I_{\rm off}}=\frac{\beta}{2}\approx\frac{K}{2}\frac{S_{\rm eff}}{S_{\rm off}}-0.56\frac{S_{\rm on}}{S_{\rm off}}-0.56. \tag{10}$$

This result indicates that the optimal ratio of dynamic to leakage energy ratio for a digital logic block is also directly set by β, which is mostly dependent upon $S_{\rm off}$, $S_{\rm on}$, and $S_{\rm eff}$, and only weakly dependent on logic style. To confirm and explain the fundamental reasoning behind prior findings obtained through numerical methods and/or analysis in specific regions of operation, this analytical formulation will next be applied to the MOSFET. The analysis will then be extended to provide new insights for alternative switching device designs.

A. Optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ for MOSFET

Energy–delay optimization of complementary MOSFET (CMOS) digital circuits has extensively been described in studies such as [23]–[26]. Nose and Sakurai [23] as well as others [24]–[26] have shown via an analysis restricted to superthreshold operation and numerical examples that the required optimal $E_{\rm dyn}/E_{\rm leak}$ for CMOS digital circuits is 3–5. The same conclusions can be reached more quickly using (10) by noting that for a state-of-the-art MOSFET [31], $S_{\rm off}$ is ~100 mV/dec. In today's CMOS digital circuit designs operating with supply voltage in the range of 0.5–1.1 V, the MOSFET ON-state drive current is approximately proportional to the gate overdrive: $I_{\rm on}\propto(V_{\rm dd}-V_T)$, and hence the on-state inverse slope can readily be estimated as $S_{\rm on}\approx(\partial\log_{10}(V_{\rm dd}-V_T)/\partial V_{\rm dd})^{-1}=(\ln 10)(V_{\rm dd}-V_T)$. For this range of supply voltage, $V_{\rm dd}-V_T$ is roughly 0.2–0.75 V, and hence, $S_{\rm on}$ ranges from 460 mV/dec to 1.73 V/dec. Finally, these devices typically achieve $I_{\rm on}/I_{\rm off}$ in the range from 1000 to 10000 in this supply voltage range, and thus, $S_{\rm eff}$ is also roughly constant at 133–275 mV/dec. For example, if $a/(L_d\times F)\sim 0.01/(30\times 4)$ with $\gamma\sim 1$, β ranges from 7.5 to 10, and the optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ values are

$$\frac{I_{\rm on}}{I_{\rm off}}=-\gamma\frac{L_dF}{4a}\frac{S_{\rm eff}}{S_{\rm off}}lambertW\left(-\frac{4a}{L_dF\gamma}\frac{S_{\rm off}}{S_{\rm eff}}\exp\left(\frac{S_{\rm off}+S_{\rm on}}{S_{\rm eff}}\right)\right)$$
$$\approx(1.94\ to\ 2.52)\times\frac{L_dF}{a} \tag{11a}$$
$$\frac{E_{\rm dyn}}{E_{\rm leak}}=\frac{a}{\gamma L_dF}\frac{2I_{\rm on}}{I_{\rm off}}=\frac{\beta}{2}\approx 4\ to\ 5 \tag{11b}$$

reaffirming that for CMOS digital circuits, the optimal MOSFET $I_{\rm on}/I_{\rm off}$ primarily depends on the circuit topology, and that the optimal $E_{\rm dyn}/E_{\rm leak}$ is relatively constant.

MOSFETs today mostly operate in strong inversion ($V_{\rm gs}>V_T$) in the ON-state, with $V_{\rm dd}\approx 1$ V. Most of the alternative switching devices have relatively low $I_{\rm on}$ at this supply voltage (e.g., $<10\ \mu$A/μm for TFETs [5], as compared with ~ 1 mA/μm for MOSFETs [30]). These devices therefore will only be competitive with MOSFETs operating in the subthreshold region (with $V_{\rm gs}<V_T$) that dissipate the minimum energy required for a CMOS digital circuit to perform an operation [25], [26]. Since $S_{\rm off}=S_{\rm on}=S_{\rm eff}\sim 100$ mV/dec for a MOSFET operating in the subthreshold region, $\beta=7.8$, and the optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ values for subthreshold CMOS technology are

$$\frac{I_{\rm on}}{I_{\rm off}}=-\gamma\frac{L_dF}{4a}lambertW\left(-\frac{4a}{L_dF\gamma}e^2\right)\approx 2.02\frac{L_dF}{a} \tag{12a}$$
$$\frac{E_{\rm dyn}}{E_{\rm leak}}=\frac{a}{\gamma L_dF}\frac{2I_{\rm on}}{I_{\rm off}}=\frac{\beta}{2}\approx 4.04 \tag{12b}$$

[4]In general, $S_{\rm off}$, $S_{\rm on}$, and $S_{\rm eff}$ depend on $I_{\rm on}$ and $I_{\rm off}$; therefore (7) and (8) must iteratively be solved to reach the energy–delay optimum.

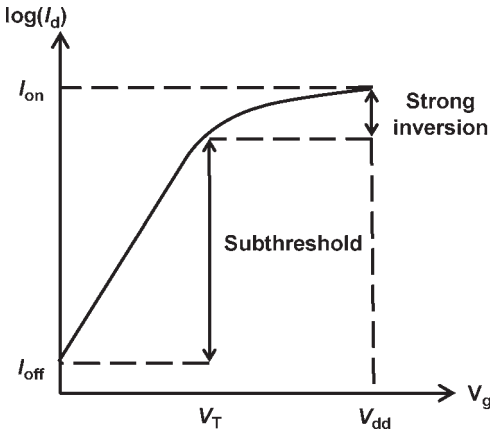

Fig. 2. Most of the change in $\log_{10}(I_d)$ for a MOSFET occurs in the subthreshold region. $\log_{10}(I_{\rm on}/I_{\rm off})$ is relatively insensitive to small changes in $V_{\rm dd}$.

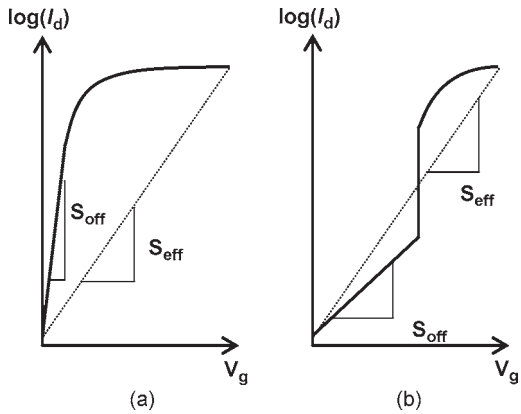

Fig. 3. Alternative switching devices generally fall into two categories: (a) devices with steep OFF-state inverse slope but relatively shallow ON-state inverse slope, i.e., $S_{\rm eff} \gg S_{\rm off}$, and (b) devices with an abrupt switching behavior, i.e., $S_{\rm eff} \ll S_{\rm off}$.

which is consistent with previously published work [25], [26].

These results confirm that the optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ ratios are roughly constant for a MOSFET, regardless of whether it operates in the subthreshold or strong inversion region. The simple analysis elucidates the fundamental reason for this: $S_{\rm on}$, $S_{\rm off}$, and $S_{\rm eff}$ of a MOSFET are roughly fixed (with $S_{\rm off} \sim S_{\rm eff}$) across a wide range of $V_{\rm dd}$, and most of the change in $I_{\rm on}/I_{\rm off}$ (as a function of $V_{\rm dd}$) occurs in the subthreshold region. Therefore, even for operation in strong inversion, the optimal $I_{\rm on}/I_{\rm off}$ is relatively insensitive to small changes in $V_{\rm dd}$, as illustrated in Fig. 2.

B. Optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ for Alternative Switching Devices

The same analytical formulations can easily be extended to provide new insights into the design of alternative switching devices. In general, these devices fall into two categories: 1) those with $S_{\rm eff} \gg S_{\rm off}$ [Fig. 3(a)], and 2) those with $S_{\rm eff} \ll S_{\rm off}$ [Fig. 3(b)]. For both types of devices, it makes intuitive sense to adjust the threshold voltage such that the ON-to-OFF transition is steep near $V_{\rm gs} = 0$ V. For devices with $S_{\rm eff} \gg S_{\rm off}$, an increase in threshold voltage is preferred as it provides for a large decrease in leakage energy at the expense of a smaller increase in dynamic energy (since a higher $V_{\rm dd}$ would be needed to achieve the required performance). Assuming this device has lower $S_{\rm eff}$ than CMOS, the total energy is therefore minimized for a higher value of $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$. For devices with $S_{\rm eff} \ll S_{\rm off}$, e.g., a device whose transfer characteristic is relatively flat at low $V_{\rm gs}$ and sharply increases at higher $V_{\rm gs}$, both the threshold voltage and the supply voltage can be reduced to lower the dynamic energy without paying a significant penalty in the leakage energy; the total energy is therefore minimized for a lower value of $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ than for the MOSFET.

Many devices will clearly fall into one of the two previous categories (sharper $S_{\rm off}$ versus sharper $S_{\rm eff}$), but the framework still provides interesting insights into the requirements of devices with the same $S_{\rm eff}$ as well as the same $S_{\rm off}$ (as shown in Fig. 4). For these devices, the optimal $I_{\rm on}/I_{\rm off}$ is determined

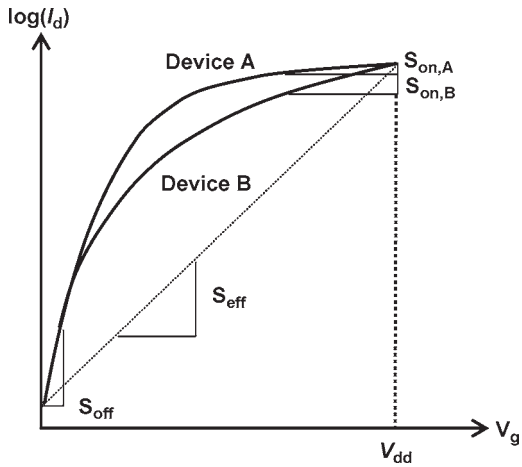

Fig. 4. Alternative switching devices with the same $S_{\rm off}$ and $S_{\rm eff}$ but with different $S_{\rm on}$ have different optimal values of $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$.

by $S_{\rm on}$, with a larger $S_{\rm on}$ resulting in a lower $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$. This is because for the same reduction in $V_{\rm dd}$, a device with high $S_{\rm on}$ would require a larger reduction in threshold voltage than its low $S_{\rm on}$ counterpart to achieve the required performance.

Finally, for alternative switching devices with nonideal switching characteristics (i.e., $\gamma > 1$), a higher $I_{\rm on}/I_{\rm off}$ (by a factor of γ) is necessary to compensate for the increase in delay and hence leakage energy due to these nonidealities. Furthermore, an alternative switching device may have substantially different gate capacitance (denoted as C') than a comparably sized MOSFET [28]. In this case, if the interconnect capacitance is not a dominant component of the load capacitance, the switching energy and delay are increased by the capacitance ratio C'/C. The optimal $I_{\rm on}/I_{\rm off}$ remains unchanged, but $I_{\rm on}$ needs to be C'/C times higher (if $C' > C$) for the same delay target.

To illustrate how the aforementioned methodology can be used to assess the optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ of an alternative switching device, we next use the TFET as an example and compare it against the MOSFET. Fig. 5 shows the $I_{\rm ds}$–$V_{\rm gs}$ characteristics of a typical TFET technology, which

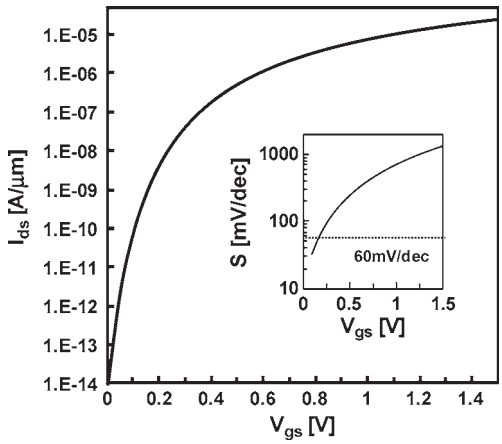

Fig. 5. $I_{\rm ds}$–$V_{\rm gs}$ characteristics of a typical exemplary TFET technology using the model discussed in [5]. Inset: inverse slope S is less than 60 mV/dec at low current levels but degrades at higher current levels.

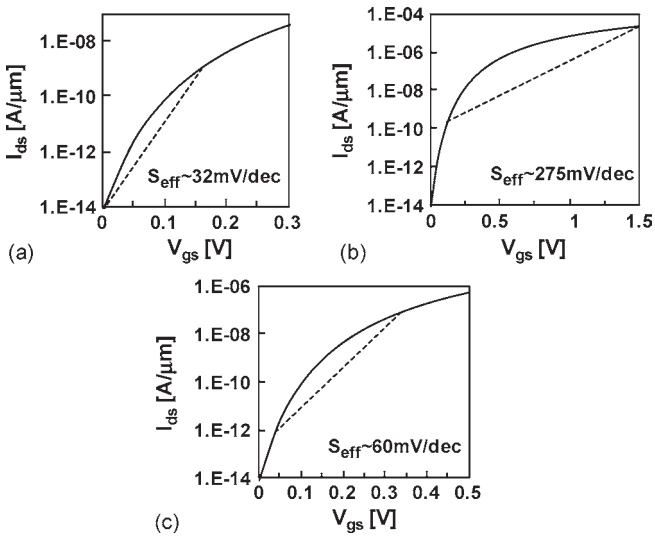

Fig. 6. Effective inverse slope for a TFET to reach the required $I_{\rm on}$ and $I_{\rm on}/I_{\rm off}$ increases with $I_{\rm on}$ (a–c).

shows a very small local subthreshold swing at low current levels (∼30–40 mV/dec at $I_{\rm ds} \sim 1-10$ pA) but a degraded swing as $I_{\rm ds}$ increases [3]–[11]. For supply voltage $V_{\rm dd}$ in the range of 0.5–1 V, $S_{\rm on}$ ranges from 260 to 800 mV/dec, with $I_{\rm on}/I_{\rm off}$ ranging from 5×10^5 to 10^7. Furthermore, $S_{\rm eff}$ is roughly constant at 80–140 mV/dec.

Due to the Miller effect, it has previously been reported that TFET has 3× larger effective gate capacitance than a comparably sized MOSFET [28] and therefore $C'/C \sim 2-3$. For $a/(L_d \times F) \sim 0.01/(30 \times 4)$ with $\gamma \sim 1$, β ranges from 19.4 to 21.3, and the optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ values are therefore

$$\frac{I_{\rm on}}{I_{\rm off}} = -\gamma \frac{L_d F}{4a} \frac{S_{\rm eff}}{S_{\rm off}} lambertW \times \left(-\frac{4a}{L_d F \gamma} \frac{S_{\rm off}}{S_{\rm eff}} \exp\left(\frac{S_{\rm off} + S_{\rm on}}{S_{\rm eff}} \right) \right) \approx (4.83 - 5.33) \times \frac{L_d F}{a} \tag{13a}$$

$$\frac{E_{\rm dyn}}{E_{\rm leak}} = \frac{a}{\gamma L_d F} \frac{2 I_{\rm on}}{I_{\rm off}} = \frac{\beta}{2} \approx 9.7 - 10.6 \tag{13b}$$

which verifies that devices with $S_{\rm eff} \gg S_{\rm off}$ have higher optimal $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ values. With these analytical formulations and example, it should now be clear that for a given performance target and circuit topology, optimal values of $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$ exist that minimize the total energy. For most steeply switching devices, the dynamic to leakage energy ratio is approximately $(E_{\rm dyn}/E_{\rm leak}) = (K/2)(S_{\rm eff}/S_{\rm off}) - 0.56(S_{\rm on}/S_{\rm off}) - 0.56$, with K ranging from 6.23 to 11.9.

IV. Effective Inverse Slope Requirements and Implications

Since the conditions for an alternative switching device to achieve optimal energy–delay are known, the energy dissipation for any switching device can analytically be derived. This allows requirements for $S_{\rm eff}$, $S_{\rm off}$, and $S_{\rm on}$ to be established for an alternative switching device to be more energy efficient than a MOSFET.

Intuitively, since the optimal $I_{\rm on}/I_{\rm off}$ is fixed for a given logic style and device technology, the energy dissipation is gauged by the supply voltage required to reach the current ratio and the performance target. As detailed in Appendix II, an alternative switching device is more energy efficient than a MOSFET only if it can satisfy the following condition:

$$S_{\rm eff} \times \sqrt{\left(1 + \frac{2}{\beta}\right)} < 60 \text{ mV/dec for the optimal } I_{\rm on}/I_{\rm off}. \tag{14}$$

This result highlights that although some previous works [2]–[20] mainly have focused on achieving the steepest subthreshold swing, this is not sufficient to ensure that the device will be more energy efficient than a MOSFET [1]. The TFET in [5] can be used as an example to illustrate this point.

Since $\beta \gg 1$ for a TFET, the energy dissipation of a TFET is gauged by $S_{\rm eff} \times \sqrt{(1 + (2/\beta))} \approx S_{\rm eff}$. As shown in Fig. 6, for low-performance applications, a TFET can achieve smaller $S_{\rm eff}$ (∼40 mV/dec) values than the MOSFET while maintaining the optimal $I_{\rm on}/I_{\rm off} \sim 10^5$ (13a), and hence, it can be more energy efficient. However, for high-performance applications requiring high $I_{\rm on} > 10$ μA/μm, a TFET has a larger $S_{\rm eff}$ value (∼275 mV/dec) and hence would consume more energy than a MOSFET. In other words, the steep local swing of the TFET is only beneficial as long as it provides lower $S_{\rm eff}$ than a MOSFET. For this particular TFET, the crossover point occurs at a delay of ~ 1 μs when $V_{\rm dd}/I_{\rm on} = 0.3$ V/7.39E-08 A/μm and $\gamma \times L_d \times F \times C' \sim 1 \times 30 \times 4 \times 3 \times 0.85$ fF.

As this example illustrates, an alternative switching device may offer energy advantages only over some range of performance. Accurately estimating this range requires a comparison of the entire energy–performance tradeoff curve (Fig. 7) of the device against that of the MOSFET, i.e., the previously described energy-optimization process must be repeated for different values of delay. Fortunately, if the optimization process

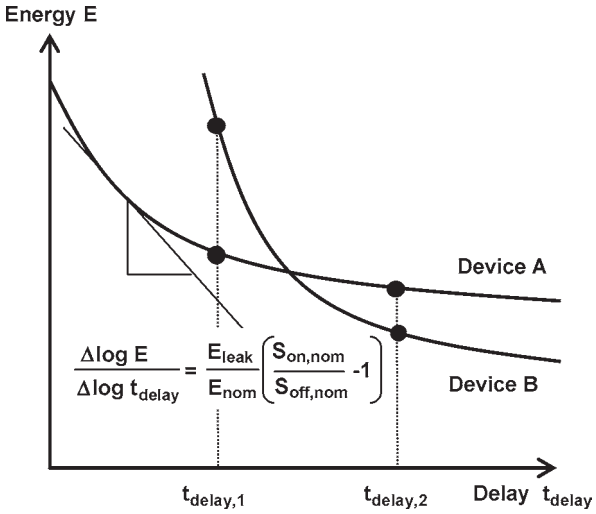

Fig. 7. Energy–delay tradeoff curves for two switching devices. Device B is more energy efficient than Device A only for low performance applications; the slope of the energy–delay tradeoff curve is set by the I_d–V_{gs} characteristic.

already has been carried out for one particular delay target, an easier approach can be taken by noting that the slope of the tradeoff curve on a log–log plot is related to the Lagrangian multiplier (or the optimal normalized sensitivity). As analytically derived in Appendix II, this slope is

$$\begin{aligned}\frac{\Delta logE}{\Delta log t_{\rm delay}} &\approx \frac{t_{\rm delay}}{E}\left(\frac{dE}{dt_{\rm delay}}\right)\\ &= -\left(\frac{E_{\rm leak,nom}}{E_{\rm nom}}\right)\left(\frac{S_{\rm on,nom}}{S_{\rm off,nom}}-1\right)\\ &= -\frac{2}{\beta+2}\left(\frac{S_{\rm on,nom}}{S_{\rm off,nom}}-1\right)\end{aligned} \tag{15}$$

where the subscript nom indicates the nominal values for an optimized device. For devices such as the TFET, which have $S_{\rm on} \gg S_{\rm off}$, a large reduction in $V_{\rm dd}$ ($\Delta V_{\rm dd} \approx V_{\rm dd,nom} \times \Delta \log t_{\rm delay}$) leads to a substantial reduction in dynamic energy at the expense of a smaller increase in delay. Therefore, as (15) indicates, this results in a steeper energy–delay tradeoff curve for TFET technology than for MOSFET technology [1], [22].

V. Conclusion

Circuit-level energy–performance analysis is necessary to assess the promise of any new device technology for potentially overcoming the energy efficiency limitations of CMOS technology. This paper presents an analytical approach to establish simple requirements for $I_{\rm on}/I_{\rm off}$ and $E_{\rm dyn}/E_{\rm leak}$, resulting in simple analytical expressions that show that these ratios are set only by circuit-level parameters as well as the device transfer characteristic OFF-state $S_{\rm off}$, ON-state $S_{\rm on}$, and effective $S_{\rm eff}$ inverse slopes. The advantage of this analytical approach is that it elucidates the dependencies of the optimal ratios on these parameters. For most alternative switching devices, the optimal $E_{\rm dyn}/E_{\rm leak}$ ratio is approximately $(K/2)(S_{\rm eff}/S_{\rm off}) - 0.56(S_{\rm on}/S_{\rm off}) - 0.56$, where K ranges from 6.23 to 11.9. Based upon this theoretical framework, simple requirements for $S_{\rm off}$, $S_{\rm on}$, and $S_{\rm eff}$ are established for an alternative switching device to be more energy efficient than a MOSFET. The results reinforce that merely focusing on achieving the steepest subthreshold swing is insufficient, since energy dissipation is set mainly by $S_{\rm eff}$ and not by the steepest swing. Finally, the general shape of the energy–delay curve is also set by these inverse slopes, with its steepness directly proportional to $S_{\rm on}/S_{\rm off}$. This analytical approach provides a simple method to assess the promise of any new device technology and to estimate the range of performance over which the alternative device can potentially overcome the energy efficiency limitations of CMOS technology.

Appendix I
Energy–Delay Optimization of a Generalized Switching Device[5]

To minimize energy consumption subject to a delay constraint, the method of Lagrange multipliers [24], [32], [33] can be used. The Lagrange function is defined as

$$L(V_{\rm dd}, I_{\rm on}) = E(V_{\rm dd}, I_{\rm on}) - \lambda D(V_{\rm dd}, I_{\rm on}) \tag{A.1}$$

where $E(V_{\rm dd}, I_{\rm on})$ is the energy consumption

$$\begin{aligned}E(V_{\rm dd}, I_{\rm on}) &= aL_dFV_{\rm dd}^2C + L_dFI_{\rm off}V_{\rm dd}t_{\rm delay}\\ &= aL_dFV_{\rm dd}^2C + \gamma\frac{C(L_dFV_{\rm dd})^2}{2}\frac{I_{\rm off}}{I_{\rm on}}\end{aligned} \tag{A.2}$$

and $D(V_{\rm dd}, I_{\rm on})$ is the delay constraint

$$D(V_{\rm dd}, I_{\rm on}) = t_{\rm delay} - \gamma\frac{L_dFC}{2I_{\rm on}}V_{\rm dd}. \tag{A.3}$$

For a variety of switching devices, the OFF-state leakage current $I_{\rm off}$ depends only on $I_{\rm on}$ and $V_{\rm dd}$. Differentiating $L(V_{\rm dd}, I_{\rm on})$ with respect to $V_{\rm dd}$ to find the minimum energy consumption

$$\begin{aligned}L(V_{\rm dd}, I_{\rm on}) &= aL_dFV_{\rm dd}^2C + \gamma\frac{C(L_dFV_{\rm dd})^2}{2}\frac{I_{\rm off}}{I_{\rm on}}\\ &\quad - \lambda\left(t_{\rm delay} - \gamma\frac{L_dFC}{2I_{\rm on}}V_{\rm dd}\right)\\ \frac{\partial L}{\partial V_{\rm dd}} &: 2aL_dFV_{\rm dd}C + \gamma C(L_dF)^2V_{\rm dd}\frac{I_{\rm off}}{I_{\rm on}}\\ &\quad + \gamma\frac{C(L_dFV_{\rm dd})^2}{2I_{\rm on}}\frac{\partial I_{\rm off}}{\partial V_{\rm dd}} + \lambda\gamma\frac{L_dFC}{2I_{\rm on}} = 0\end{aligned} \tag{A.4}$$

which can be simplified to

$$\frac{4aV_{\rm dd}}{\gamma} + 2L_dFV_{\rm dd}\frac{I_{\rm off}}{I_{\rm on}} + \frac{L_dF(V_{\rm dd})^2}{I_{\rm on}}\frac{\partial I_{\rm off}}{\partial V_{\rm dd}} = -\frac{\lambda}{I_{\rm on}}. \tag{A.5}$$

[5]Note that the energy–delay optimization for logic circuit is highly analogous to the price theory in microeconomics [32]–[34]. With this, designers may apply these well-developed economic theories (e.g., the Slustky equation [32], [33]) to gain insights in digital logic design. To achieve this goal, techniques are required that are beyond the scope of this paper.

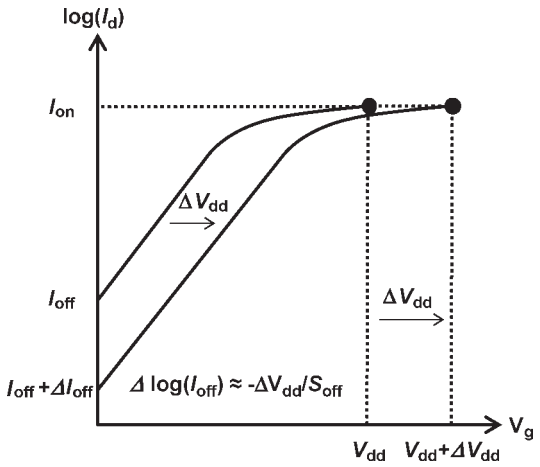

Fig. 8. Derivation of $(\partial I_{\rm off}/\partial V_{\rm dd})$ for fixed $I_{\rm on}$. If the supply voltage $(V_{\rm dd})$ is increased, then the threshold voltage V_T must be increased so that the OFF-state leakage current $I_{\rm off}$ decreases.

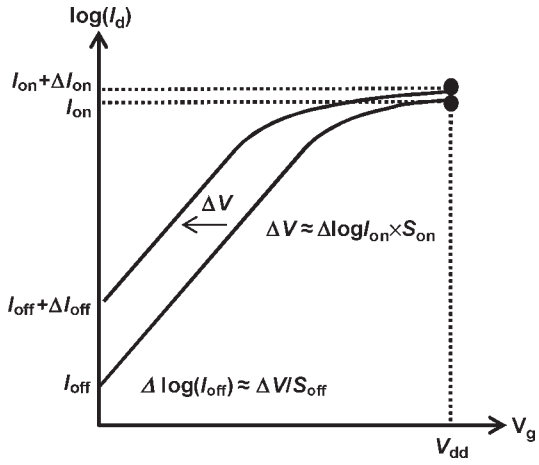

Fig. 9. Derivation of $(\partial I_{\rm off}/\partial I_{\rm on})$ for fixed $V_{\rm dd}$. If the ON-state drive current $I_{\rm on}$ is increased by reducing the threshold voltage V_T, then the OFF-state leakage current $I_{\rm off}$ increases.

Note that V_T must be increased together with $V_{\rm dd}$ to maintain the same $I_{\rm on}$ (Fig. 8). As a result, $I_{\rm off}$ decreases, and $(\partial I_{\rm off}/\partial V_{\rm dd})$ is inversely proportional to $S_{\rm off}$, i.e.,

$$\frac{\partial I_{\rm off}}{\partial V_{\rm dd}} = -\ln(10) I_{\rm off} S_{\rm off}^{-1}. \tag{A.6}$$

Substituting (A.6) into (A.5)

$$\frac{4aV_{\rm dd}}{\gamma} + 2L_d F V_{\rm dd}\frac{I_{\rm off}}{I_{\rm on}} - \frac{L_d F (V_{\rm dd})^2}{I_{\rm on}}\ln(10) I_{\rm off} S_{\rm off}^{-1} = -\frac{\lambda}{I_{\rm on}}. \tag{A.7}$$

Differentiating $L(V_{\rm dd}, I_{\rm on})$ with respect to $I_{\rm on}$ to find the minimum energy consumption

$$\frac{\partial L}{\partial I_{\rm on}} : \frac{C(L_d F V_{\rm dd})^2}{2}\frac{\partial}{\partial I_{\rm on}}\frac{I_{\rm off}}{I_{\rm on}} - \lambda\left(\frac{L_d F C}{2I_{\rm on}^2}V_{\rm dd}\right) = 0$$

$$L_d F V_{\rm dd}\frac{\partial}{\partial I_{\rm on}}\frac{I_{\rm off}}{I_{\rm on}} = \lambda\left(\frac{1}{I_{\rm on}^2}\right) \tag{A.8}$$

$$L_d F V_{\rm dd}\left(\frac{I_{\rm on}\frac{\partial I_{\rm off}}{\partial I_{\rm on}} - I_{\rm off}}{I_{\rm on}^2}\right) = \lambda\left(\frac{1}{I_{\rm on}^2}\right)$$

$$L_d F V_{\rm dd}\left(\frac{\partial I_{\rm off}}{\partial I_{\rm on}} - \frac{I_{\rm off}}{I_{\rm on}}\right) = \lambda\left(\frac{1}{I_{\rm on}}\right). \tag{A.9}$$

Note that for a fixed $V_{\rm dd}$, $I_{\rm on}$ is increased by decreasing V_T (Fig. 9). As a result, $I_{\rm off}$ increases, i.e.,

$$\Delta log_{10} I_{\rm off} = \Delta V \times S_{\rm off}^{-1} \tag{A.10}$$

where

$$\Delta V \cong \Delta log_{10} I_{\rm on} \times S_{\rm on} \tag{A.11}$$

and $(\partial I_{\rm off}/\partial I_{\rm on})$ is proportional to $S_{\rm on}/S_{\rm off}$, i.e.,

$$\frac{\partial I_{\rm off}}{\partial I_{\rm on}} = \frac{I_{\rm off}}{I_{\rm on}}\frac{S_{\rm on}}{S_{\rm off}}$$

$$L_d F V_{\rm dd}\frac{I_{\rm off}}{I_{\rm on}}\left(\frac{S_{\rm on}}{S_{\rm off}} - 1\right) = \lambda\left(\frac{1}{I_{\rm on}}\right). \tag{A.12}$$

Equating (A.7) and (A.9)

$$\frac{4aV_{\rm dd}}{\gamma} + 2L_d F V_{\rm dd}\frac{I_{\rm off}}{I_{\rm on}} - \frac{L_d F (V_{\rm dd})^2}{I_{\rm on}}\ln(10) I_{\rm off} S_{\rm off}^{-1} = -L_d F V_{\rm dd}\frac{I_{\rm off}}{I_{\rm on}}\left(\frac{S_{\rm on}}{S_{\rm off}} - 1\right). \tag{A.13}$$

After simplification and substituting (7) into (A.13)

$$\frac{4a}{L_d F\gamma} + 2\frac{I_{\rm off}}{I_{\rm on}} - \frac{V_{\rm dd}}{I_{\rm on}}\ln(10) I_{\rm off} S_{\rm off}^{-1} = -\frac{I_{\rm off}}{I_{\rm on}}\left(\frac{S_{\rm on}}{S_{\rm off}} - 1\right) \tag{A.14}$$

$$\frac{4a}{L_d F\gamma} + \left(1 + \frac{S_{\rm on}}{S_{\rm off}}\right)\frac{I_{\rm off}}{I_{\rm on}} - \frac{I_{\rm off}}{I_{\rm on}} V_{\rm dd}\ln(10) S_{\rm off}^{-1} = 0 \tag{A.15}$$

$$\frac{4a}{L_d F\gamma} + \left(1 + \frac{S_{\rm on}}{S_{\rm off}}\right)\frac{I_{\rm off}}{I_{\rm on}} - \frac{I_{\rm off}}{I_{\rm on}}\left(\frac{log_{10}(I_{\rm on}/I_{\rm off})}{S_{\rm eff}^{-1}}\right)\ln(10) S_{\rm off}^{-1} = 0. \tag{A.16}$$

After simplification, (A.16) becomes

$$\frac{4a}{L_d F\gamma}\frac{S_{\rm off}}{S_{\rm eff}}\frac{I_{\rm on}}{I_{\rm off}} + \left(\frac{S_{\rm off} + S_{\rm on}}{S_{\rm eff}}\right) - \ln\left(\frac{I_{\rm on}}{I_{\rm off}}\right) = 0 \tag{A.17}$$

$$-\frac{4a}{L_d F\gamma}\frac{I_{\rm on}}{I_{\rm off}}\frac{S_{\rm off}}{S_{\rm eff}}\exp\left(-\frac{4a}{L_d F\gamma}\frac{I_{\rm on}}{I_{\rm off}}\frac{S_{\rm off}}{S_{\rm eff}}\right) = -\frac{4a}{L_d F\gamma}\frac{S_{\rm off}}{S_{\rm eff}}\exp\left(\frac{S_{\rm off} + S_{\rm on}}{S_{\rm eff}}\right). \tag{A.18}$$

The optimal $I_{\rm on}/I_{\rm off}$ is therefore expressed by (6), which is repeated here

$$\frac{I_{\rm on}}{I_{\rm off}} = -\gamma\frac{L_d \cdot F}{4a}\frac{S_{\rm eff}}{S_{\rm off}} lambertW \left(-\frac{4a}{L_d F\gamma}\frac{S_{\rm off}}{S_{\rm eff}}\exp\left(\frac{S_{\rm off} + S_{\rm on}}{S_{\rm eff}}\right)\right) \tag{A.19}$$

$$\frac{I_{\rm on}}{I_{\rm off}} \cong -\gamma\frac{L_dF}{4a}\frac{S_{\rm eff}}{S_{\rm off}}\left(1.1155\ln\left(\frac{4a}{L_dF\gamma}\frac{S_{\rm off}}{S_{\rm eff}}\exp\left(\frac{S_{\rm off}+S_{\rm on}}{S_{\rm eff}}\right)\right)-1.093\right)$$
$$\frac{I_{\rm on}}{I_{\rm off}} \cong \gamma\frac{L_dF}{4a}\frac{S_{\rm eff}}{S_{\rm off}}\left(-1.1155\frac{S_{\rm off}+S_{\rm on}}{S_{\rm eff}}+1.1155\ln\left(\frac{L_dF\gamma}{4a}\frac{S_{\rm eff}}{S_{\rm off}}\right)+1.093\right)$$
$$\frac{I_{\rm on}}{I_{\rm off}} \cong \gamma\frac{L_dF}{4a}\left(-1.1155\frac{S_{\rm off}+S_{\rm on}}{S_{\rm off}}+\frac{S_{\rm eff}}{S_{\rm off}}\left(1.1155\ln\left(\frac{\gamma L_dF}{4a}\frac{S_{\rm eff}}{S_{\rm off}}\right)+1.093\right)\right)$$
$$\frac{I_{\rm on}}{I_{\rm off}} \cong \gamma\frac{L_dF}{4a}\left(-1.1155\frac{S_{\rm on}}{S_{\rm off}}+\frac{S_{\rm eff}}{S_{\rm off}}\left(1.1155\ln\left(\frac{\gamma L_dF}{4a}\frac{S_{\rm eff}}{S_{\rm off}}\right)+1.093\right)-1.1155\right) \quad \text{(A.20)}$$

where $lambertW(y)$ is the solution to the equation $y = xe^x$. Note that for $-1/e < y < 0$, $lambertW(y) \approx 1.1155 \times ln(-y) - 1.093$. Therefore, (A.19) can be approximated by (8b) as (A.20), shown at the top of the page.

Appendix II
Energy Dissipation and Energy–Delay Tradeoff

To compute the energy dissipation, the optimal $I_{\rm on}/I_{\rm off}$ (A.20) is first substituted into the energy equation (9). Although the optimal supply voltage $V_{\rm dd,opt}$ to reach the required $I_{\rm on}/I_{\rm off}$ can only be obtained numerically, it is clearly proportional to $S_{\rm eff}$, since $V_{\rm dd,opt} = S_{\rm eff} \times \log_{10}(I_{\rm on}/I_{\rm off})$. Therefore, using (9) and (10), the dynamic and leakage components of energy can be expressed as

$$E_{\rm dyn} = aL_dFCV_{\rm dd,opt}^2 \propto S_{\rm eff}^2\left[log_{10}\left(\frac{I_{\rm on}}{I_{\rm off}}\right)\right]^2 \sim S_{\rm eff}^2 \quad \text{(A.21)}$$

$$E_{\rm leak} = E_{\rm dyn} \times \frac{2}{\beta}. \quad \text{(A.22)}$$

Substituting (A.21) into (A.22), the leakage components of energy can be expressed as

$$E_{\rm leak} \propto \frac{2}{\beta}S_{\rm eff}^2 \quad \text{(A.23)}$$

where $\beta \equiv -(S_{\rm eff}/S_{\rm off})lambertW(-4a/(\gamma L_dF) \times (S_{\rm off}/S_{\rm eff}) \times \exp((S_{\rm off}+S_{\rm on})/S_{\rm eff})) \approx K(S_{\rm eff}/S_{\rm off}) - 1.1155(S_{\rm on}/S_{\rm off}) - 1.1155$, and $K \equiv 1.1155\ln(\gamma(L_dF/4a)(S_{\rm eff}/S_{\rm off})) + 1.093$.

Therefore, the total energy can roughly be estimated as

$$E = E_{\rm dyn} + E_{\rm leak} \propto S_{\rm eff}^2\left(1+\frac{2}{\beta}\right). \quad \text{(A.24)}$$

For a MOSFET, $S_{\rm eff}^2(1+(2/\beta)) \sim S_{\rm eff}^2 \sim (60\ \text{mV/dec})^2$. Therefore, an alternative switching device is more energy efficient than a MOSFET only if it can satisfy the following condition:

$$S_{\rm eff} \times \sqrt{\left(1+\frac{2}{\beta}\right)} < 60\ \text{mV/dec at the optimal } I_{\rm on}/I_{\rm off}. \quad \text{(A.25)}$$

Once the energy–delay optimization process has already been carried out for one particular delay target, the slope of the energy–delay tradeoff curve on a log–log plot is related to the Lagrangian multiplier (or the optimal normalized sensitivity) [31], [32], which can be obtained and expressed by

$$\lambda = \frac{dE}{dt_{\rm delay}} = -I_{\rm on}L_dFV_{\rm dd}\frac{I_{\rm off}}{I_{\rm on}}\left(\frac{S_{\rm on}}{S_{\rm off}}-1\right) \quad \text{(A.26)}$$

which is interpreted as the energy reduction per delay cost at the optimal design point. Therefore, the normalized sensitivity, which is defined as $(t_{\rm delay}/E_{\rm nom}) \times (dE/dt_{\rm delay})$, can be expressed by

$$\frac{\Delta logE}{\Delta logt_{\rm delay}} \approx \frac{t_{\rm delay}}{E}\frac{dE}{dt} = -\frac{\frac{\gamma C}{2}(L_dFV_{\rm dd})^2\frac{I_{\rm off}}{I_{\rm on}}}{E_{\rm nom}}\left(\frac{S_{\rm on,nom}}{S_{\rm off,nom}}-1\right)$$
$$\frac{\Delta logE}{\Delta logt_{\rm delay}} \approx \frac{t_{\rm delay}}{E}\frac{dE}{dt} = -\left(\frac{E_{\rm leak}}{E_{\rm norm}}\right)\left(\frac{S_{\rm on,nom}}{S_{\rm off,nom}}-1\right) = -\frac{2}{\beta+2}\left(\frac{S_{\rm on,nom}}{S_{\rm off,nom}}-1\right) \quad \text{(A.27)}$$

where the subscript nom indicates the nominal values for an optimized device.

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