Ultrathin body InAs tunneling field-effect transistors on Si substrates

Alexandra C. Ford,[1,2] Chun Wing Yeung,[1] Steven Chuang,[1,2] Ha Sul Kim,[1,2] Elena Plis,[3] Sanjay Krishna,[3] Chenming Hu,[1] and Ali Javey[1,2,a)]
[1]*Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, California 94720, USA and Berkeley Sensor and Actuator Center, University of California at Berkeley, Berkeley, California 94720, USA*
[2]*Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, USA*
[3]*Department of Electrical and Computer Engineering, Center for High Technology Materials, University of New Mexico, Albuquerque, New Mexico 87106, USA*

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An ultrathin body InAs tunneling field-effect transistor on Si substrate is demonstrated by using an epitaxial layer transfer technique. A postgrowth, zinc surface doping approach is used for the formation of a p^+ source contact which minimizes lattice damage to the ultrathin body InAs compared to ion implantation. The transistor exhibits gated negative differential resistance behavior under forward bias, confirming the tunneling operation of the device. In this device architecture, the ON current is dominated by vertical band-to-band tunneling and is thereby less sensitive to the junction abruptness. The work presents a device and materials platform for exploring III–V tunnel transistors. © *2011 American Institute of Physics*. [doi:10.1063/1.3567021]

Recently, a method to directly integrate ultrathin layers of compound semiconductor-on-insulator has been developed by using an epitaxial layer transfer technique.[1,2] This compound semiconductor-on-insulator platform, so called "XOI" in analogy to silicon-on-insulator, offers the advantages of combining III–V semiconductors with well-established Si technology. The use of ultrathin III–V layers-on-insulator offers the benefit of reduced leakage currents due to both smaller junction areas and no junction leakage path to the semiconductor body, thereby permitting lower OFF-state currents critical to the use of low band-gap semiconductors like InAs.[1,3] Furthermore, the XOI platform potentially offers the advantage of allowing the combination of different III–V active layers with low defect density on insulator unconstrained by the original III–V growth substrates. This allows for the study of fundamental materials parameters and the exploration of various device architectures. By utilizing the XOI concept, here, we report an ultrathin body InAs tunneling field-effect transistor (TFET) on a Si substrate.

TFETs hold promise to potentially replace or complement metal-oxide-semiconductor field-effect transistors due to their improved subthreshold swing (SS) and reduced power consumption as projected by simulation and supported in part by preliminary experimental results.[4–10] Small band-gap III–V semiconductors like InAs are ideal for use in tunneling devices, as the small direct band gap provides a low effective tunneling barrier and the low effective mass results in a high tunneling probability to achieve high ON currents.[11] Use of III–V semiconductors also allows for a spectrum of materials with tunable band alignments which could potentially enable heterojunction device exploration with extremely low effective tunneling barrier.[12]

A schematic of the InAs XOI TFET fabrication process is shown in Fig. 1. InAs nanoribbons (NRs) ~18 nm in height and ~350 nm in width were transferred to 60 nm low-stress silicon nitride on p^+ Si substrates through a previously described epitaxial layer transfer process [Fig. 1(a)].[1] Photolithography followed by electron-beam evaporation of 80 nm SiO_x and liftoff was used to pattern SiO_x masks to

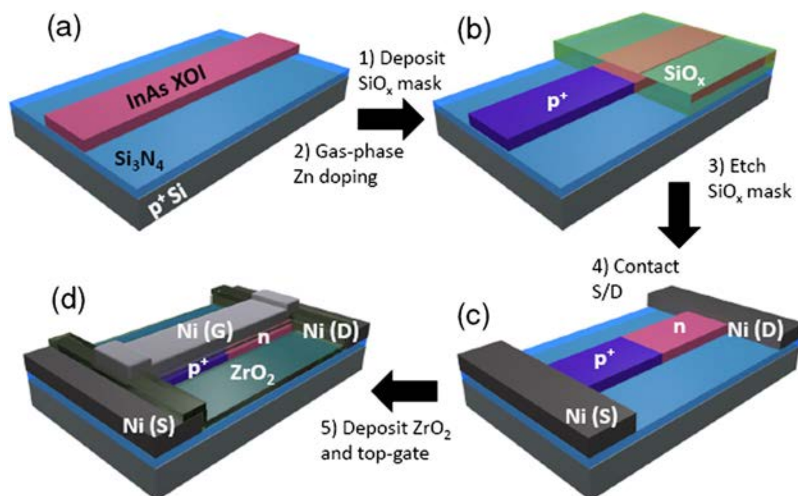

FIG. 1. (Color online) Schematic of the InAs XOI TFET fabrication process. (a) InAs strips (~18 nm thick and ~350 nm wide) were transferred to low-stress nitride on p^+ Si substrates. (b) SiO_x masks were deposited followed by gas phase doping of Zn to form the p^+ S contacts. (c) Ni S/D contacts were formed. (d) For the gate dielectric, 8 nm ZrO_2 was deposited by atomic layer deposition and a Ni top-gate (G) overlapping S/D was formed.

a)Author to whom correspondence should be addressed. Electronic mail: ajavey@eecs.berkeley.edu.

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partially cover the InAs NRs [Fig. 1(b)]. The unmasked, exposed segments of the InAs NRs were then doped p^+ with zinc using a surface diffusion method at temperatures of 390–410 °C for ~30 s to 1 min.[13] The diffusion length $[x=2(Dt)^{1/2}$, where D and t are the diffusion coefficient and time, respectively] of Zn in InAs is 130–180 nm for the doping temperatures ($D=1.4\times10^{-12}$ cm^2/s at 400 °C) and times used, resulting in a nonabrupt lateral junction.[14] The diffusion length is longer than the InAs thickness of ~18 nm, resulting in the entire depth of InAs getting doped. The SiO_x masks were then etched in 50:1 HF and the p^+ source (S) and n^+ drain (D) Ni contacts were formed by photolithography, Ni evaporation, and liftoff [Fig. 1(c)]. Undoped InAs is intrinsically n-type, making the TFET p^+-n structure possible without the intentional use of an n-type dopant. Following S/D metal contact formation, 8 nm ZrO_2 was deposited by atomic layer deposition at 130 °C for the gate dielectric and a Ni top-gate (G) overlapping S/D was formed [Fig. 1(d)].

Confirmation of p^+ doping was obtained by fabricating back-gated InAs NR devices that were blank-doped (i.e., unpatterned). The p^+ blank-doped devices (channel length $L=5$ μm) have ON current densities of ~15 μA/μm at $V_{DS}=1$ V and $V_{GS}=-4$ V, with minimal back-gate dependence. The electrically active [Zn] is estimated to be $\sim1\times10^{19}$ cm^{-3} which is in good agreement with the previously reported result for Zn-doped InAs nanowires and bulk substrates.[13,14]

The room temperature I-V characteristics of a representative TFET device (channel length $L\sim2.5$ μm) are shown in Fig. 2. The device has SSs of ~170 and 190 mV/decade for $V_{DS}=0.01$ and 0.1 V, respectively [Fig. 2(a)]. The SS exceeding 60 mV/decade is likely the result of surface trap states, and/or trap-assisted tunneling (TAT).[15,16] Figure 2(b) shows the room temperature output characteristics of the same device. The ON current density is ~0.5 μA/μm at $V_{DS}=V_{GS}=1$ V. The device is forward biased for negative V_{DS}, and under positive V_{GS}, negative differential resistance (NDR) behavior is observed, clearly confirming the interband tunneling operation of the device. The NDR peak-to-valley ratio of 1.3 at room temperature is obtained at $V_{GS}=1$ V which is in good agreement with previously reported InAs tunnel diodes.[17,18]

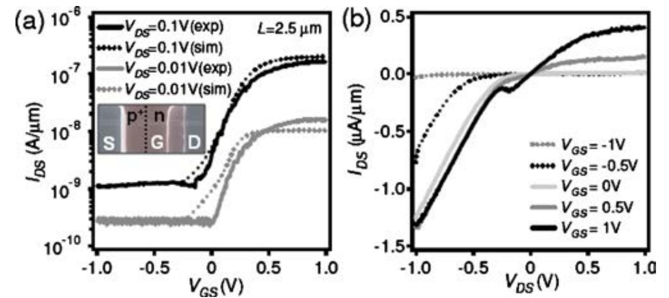

FIG. 2. (Color online) Room temperature (a) transfer and (b) output characteristics of a representative InAs XOI TFET (channel length $L\sim2.5$ μm).

To better understand the device operation, two-dimensional device simulations using TCAD SENTAURUS were performed. The dynamic nonlocal path band-to-band model is used. Standard Shockley–Read–Hall (SRH) recombination and drift-diffusion models were used for carrier transport, and Fermi statistics were assumed. An electrically active [Zn] of 1×10^{19} cm^{-3} for the p^+ source, intrinsic InAs electron concentration of 1×10^{17} cm^{-3} for the channel, equivalent oxide thickness of 2 nm, and Zn lateral diffusion length (junction abruptness) of 180 nm were used. To take into account the effects of quantization, a band gap of 0.385 eV and electron effective mass of $0.026m_o$ were used. The simulated transfer characteristics of the TFET are plotted alongside the experimental results in Fig. 2(a) and are in good agreement. From the Kane and Keldysh models in the uniform electric-field limit,[19] the fitted A and B parameters for the simulation were 7×10^{16} cm^{-3} s^{-1} and 1.3×10^6 V/cm, respectively. The fitted B parameter is in good agreement with the calculated value of 1.3×10^6 V/cm but the fitted A parameter differs substantially from the calculated value of 9×10^{19} cm^{-3} s^{-1} by approximately three orders of magnitude. This large discrepancy is likely the result of the density of interface traps, D_{it}, at the ZrO_2/InAs interface being un-

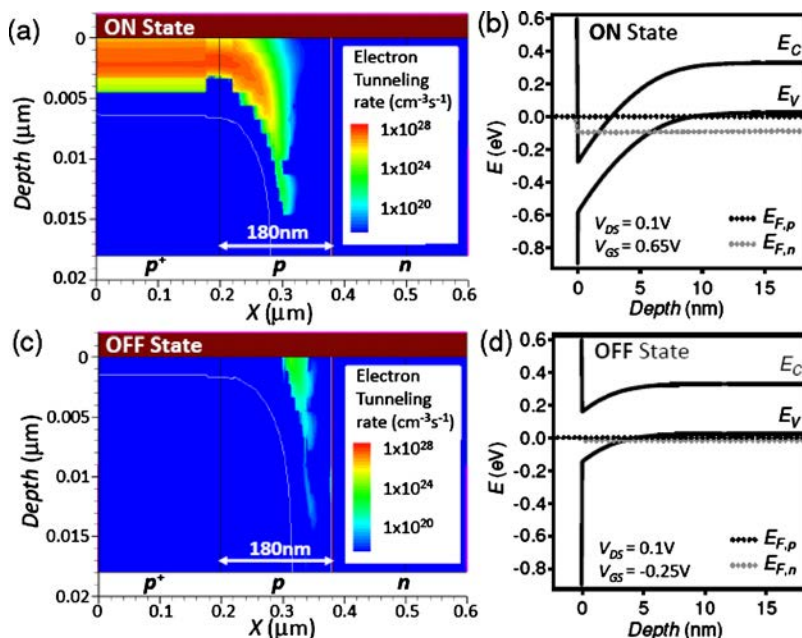

FIG. 3. (Color online) Simulated band-to-band tunneling contour plots and the corresponding vertical band diagrams for the device in [(a) and (b)] ON ($V_{GS}=0.65$ V) and [(c) and (d)] OFF ($V_{GS}=-0.25$ V) states at $V_{DS}=0.1$ V.

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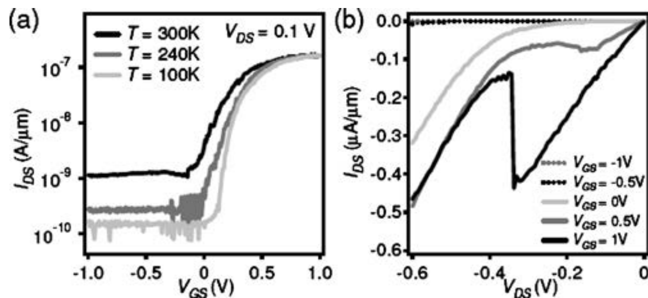

FIG. 4. Temperature dependent (a) transfer characteristics of a representative TFET for $V_{DS}=0.1$ V, and (b) output characteristics at 100 K for the NDR operation mode.

accounted for in the simulation. The electric field in the actual device is therefore lower than in the simulation as a result of reduced gating efficiency due to D_{it}. It is also possible that there are other effects due to quantum confinement that are not fully taken into account by the simulation.

The simulated band-to-band tunneling contour plots and the corresponding vertical band diagrams for the device in the ON ($V_{GS}=0.65$ V) and OFF ($V_{GS}=-0.25$ V) states at $V_{DS}=0.1$ V are shown in Fig. 3. The band-to-band tunneling current has vertical and lateral contributions with the vertical contribution being more dominant as clearly shown on the contour plot [Fig. 3(a)]. Figure 3(b) shows the vertical band diagram for the ON state. Since the p^+ S overlaps the gate, it is inverted at the surface for positive V_{GS}. This surface inversion is particularly easy to achieve at a small V_{GS} swing for a small band-gap semiconductor, like InAs. The vertical depletion width of <10 nm is significantly smaller than the lateral junction abruptness of ~ 180 nm achieved by zinc doping, resulting in the vertical tunneling being the dominant current component.

To better characterize the XOI TFETs, temperature dependent electrical measurements were performed. Figure 4(a) shows the temperature dependent transfer characteristics of a device for $V_{DS}=0.1$ V. The OFF-state current and SS decrease with decreasing temperature while the ON current is nearly independent of temperature. The OFF-state current in our device is most likely dominated by the SRH generation-recombination current, which is strongly dependent on temperature through the intrinsic carrier concentration, and the background thermal radiation effect.[16,20] In addition, at low temperatures, interface traps freeze out, subsequently resulting in the reduction in TAT and SS. Specifically, SS is ~ 60 mV/decade at 100 K and increases with temperature to ~ 190 mV/decade at 300 K. Figure 4(b) shows the temperature dependent output characteristics at 100 K for the NDR operation mode. The NDR peak-to-valley current ratio increases at low temperatures and is ~ 3 at 100 K. This compares well to the peak-to-valley ratio of 2 at 150 K reported in the literature for an InGaAs TFET.[16]

The best reported III–V TFET to date has an ON current density of ~ 50 μA/μm, ON/OFF ratio $>10^4$ and SS ~ 93 mV/decade at $V_{DS}=1.05$ V for a channel length $L=100$ nm.[15] This TFET is based on a MBE grown InGaAs n^+-n-i-p^+ structure on InP substrate. The figures of merit presented here are respectable given that a nonideal dopant, zinc, was used for the p^+ S formation with a long channel length of ~ 2.5 μm. Of particular importance, the InAs XOI TFET reported here is fabricated on a Si substrate which presents a viable route for future manufacturing. The XOI TFETs can be further improved by scaling the device dimensions, improving the surface properties, using a slower diffusing dopant, or other more optimal III–V materials stack, including heterojunctions.

The demonstration of an ultrathin body InAs TFET on a Si substrate shows the possibility of integrating high performance III–V materials with existing Si technology for various device architectures. Furthermore, the ability to pattern-dope III–V ultrathin layers after the growth provides an opportunity to explore a wide range of device geometries in the future. The device presented here utilizes vertical band-to-band tunneling as the dominant ON current contribution, making the device performance less sensitive to the lateral junction abruptness. This effect is particularly evident for small band-gap InAs. In the future, InAs XOI devices with abrupt lateral junctions can be fabricated to examine the device performance as a function of lateral versus vertical tunneling current components.

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