Nanoscale Semiconductor "X" on Substrate "Y" – Processes, Devices, and Applications

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Recent advancements in the integration of nanoscale, single-crystalline semiconductor 'X' on substrate 'Y' (XoY) for use in transistor and sensor applications are presented. XoY is a generic materials framework for enabling the fabrication of various novel devices, without the constraints of the original growth substrates. Two specific XoY process schemes, along with their associated materials, device and applications are presented. In one example, the layer transfer of ultrathin III–V semiconductors with thicknesses of just a few nanometers on Si substrates is explored for use as energy-efficient electronics, with the fabricated devices exhibiting excellent electrical properties. In the second example, contact printing of nanowire-arrays on thin, bendable substrates for use as artificial electronic-skin is presented. Here, the devices are capable of conformably covering any surface, and providing a real-time, two-dimensional mapping of external stimuli for the realization of smart functional surfaces. This work is an example of the emerging field of "*translational nanotechnology*" as it bridges basic science of nanomaterials with practical applications.

1. Introduction

In this Progress Report, recent advancements in the heterogeneous integration of single-crystalline semiconductors on non-conventional and often non-crystalline substrates for various applications are presented, mainly focusing on the work conducted in our laboratory at University of California, Berkeley. The approach decouples the choice of the active semiconductor layer from the support substrate, and thus allows for integration of, in principal, any functional semiconductor 'X' on any support substrate 'Y'. This concept, which we abbreviate as X-on-Y or XoY, presents a versatile material, processing and device technology platform for enabling new applications such as artificial electronic skin (e-skin),[1–4] paper-like displays,[5,6] or energy-efficient electronics (**Figure 1**).[7] XoY architecture has been commonly utilized for synthetic nanoscale electronic materials, such as carbon nanotubes,[8–12] graphene,[13–15] and nanowires[1,16–21] in the past where the use of a foreign handling support is a necessity. More recently, the concept has been applied to epitaxial thin films with nano- or micrometer-scale dimensions.[7,22] Besides the enabled technologies, XoY facilitates the exploration of the fundamental science associated with the interfaces of highly dissimilar materials which often have drastic effects on the device properties. While the approach is generic for both micro- and nano-scale semiconductors, in this report, we focus only on films and wires with nano-scale dimensions, where the physical and chemical properties can be drastically altered by various size-effects.

The XoY concept requires the successful transfer of crystalline semiconductor structures with clean and well-defined interfaces on the substrate, and preserved electronic and optical properties. In this regard, selective transfer techniques based on bottom-up and top-down fabricated nanostructures to both mechanically rigid and flexible substrates have been widely explored in the past. One specific approach is the epitaxial layer transfer (ELT) technique,[23–26] where a rubber stamp is used to lift-off partially released structures from an epitaxial growth substrate followed by their transfer to a receiver substrate. The first report of ELT dates back to 1975 when GaAs layers with micro-scale thicknesses were successfully transferred onto glass substrates for the fabrication of photocathodes and subsequently night vision goggles.[27] In 1978, the first GaAs solar cell on glass was demonstrated by the use of ELT.[28] Yablonovitch et al. used a similar process in the late 1980s for the fabrication of thin film GaAs diode lasers and other optoelectronic devices on glass substrates.[29] In the 2000s, Rogers and colleagues extended the use of ELT for the fabrication of mechanically flexible and stretchable electronics, photodiodes and solar cells.[23–25] Recently, a similar ELT technique was used by our group for the well-controlled transfer of ultrathin layers of III–V compound semiconductors, with thicknesses down to just a few nanometers, to Si/SiO_2 substrates[7]. These ultrathin films function as highly quantized, two-dimensional semiconductors with novel properties. The presented approach has enabled the fabrication of high-performance, energy-efficient III–V transistors

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on Si substrates, combining the high electron mobility of III–V semiconductors with the well-established Si technology.[7,30] Although, production-scale layer transfer has not been demonstrated yet, preliminary works have shown that the process can work at the wafer-scale[31,32] through the proper understanding and optimization of the transfer parameters.[26]

Another XoY fabrication process scheme involves the transfer and assembly of bottom-up semiconducting nanostructures, such as nanowires (NWs) to the desired substrates. Various NW assembly techniques including microfluidic channel,[33] Langmuir Blodgett,[34–36] magnetic[37] or electric-field alignment[38,39] have been demonstrated, although they are mainly limited to small-scales and often lack the desired uniformity. Direct NW transfer from a growth substrate by a print-and-slide technique has successfully demonstrated the assembly of aligned NWs on a large scale, up to a few cm^2 areas.[1,40–45] This method has found its use for flexible electronics and sensors, where tremendous progress has been made in integrating inorganic, nanoscale semiconductors with device performances superior to those obtained from their organic counterparts.

In the work presented in this report, integration of nanoscale inorganic semiconductors, specifically, ultrathin layers and NWs on both rigid and flexible substrates for use in high speed, energy-efficient transistors, and flexible electronics and sensors is demonstrated. In particular, the freedom in the choice of the semiconductor material 'X' and substrate 'Y' elucidates the functionality, feasibility and versatility of the 'XoY' platform for use in future tailored integrated systems. This work focuses on "*translational nanotechnology*" which centers on application development based on nanomaterials.

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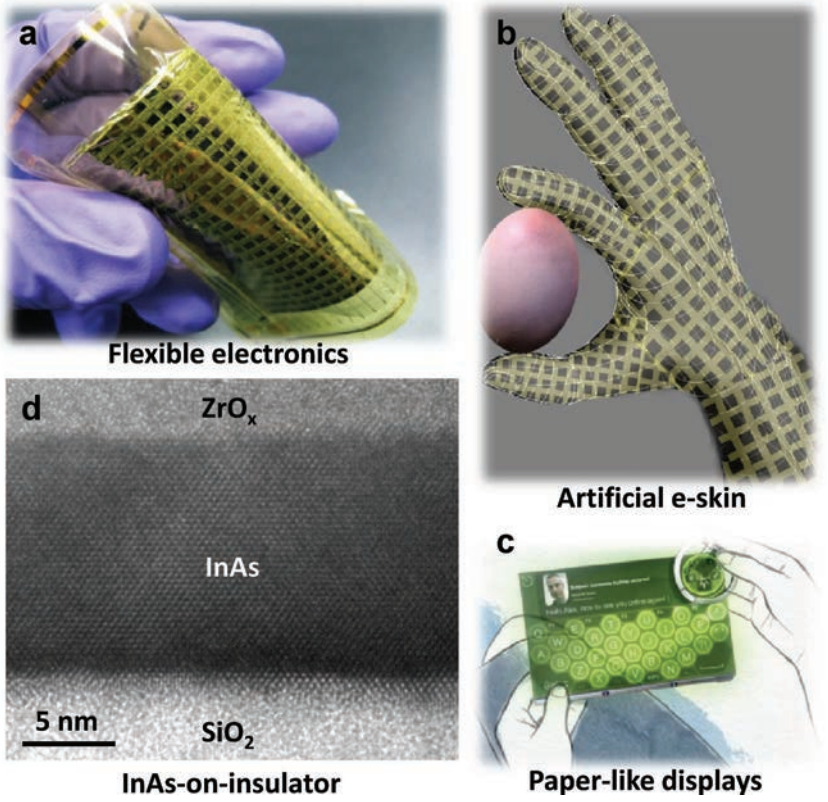

Figure 1. Examples of various applications enabled by the XoY concept, (a) Flexible electronics,[1] (b) Artificial electronic-skin,[1] (c) Paper-like displays (copyright Nokia, Morph concept; reproduced with permission from Nokia),[6] and (d) Ultrathin III–V compound semiconductors on Si/SiO_2 substrates for low-power electronics.[7]

2. Ultrathin III–V Layers on SI Substrates for Energy-Efficient Electronics

In the past several years, III–V compound semiconductors have been widely explored as high electron mobility components in high speed electronics.[46] Previously, the devices were primarily fabricated on III–V wafers, but this approach is not cost-effective, and thus has limited their commercial use for consumer electronics. Recently, there has been a strong drive to integrate ultrathin layers of compound semiconductors on Si substrates for low power MOSFETs with the enabled integrated circuits (ICs) operating at voltages as low as $V_{DD} \sim 0.5$ V, which is ~2x lower than that of the current state-of-the-art Si ICs.[47–52] However, there are significant challenges in the fabrication process. Specifically, given the large lattice mismatch of Si and III–V semiconductors, heteroepitaxial growth techniques often require the deposition of a thick buffer layer for compensating the large lattice mismatch followed by the deposition of the active layer (**Figure 2**a).[47] This process is challenging and often results in active III–V layers with high defect densities, although significant progress has been made in this regard in the recent years. In a different approach, we have focused on the

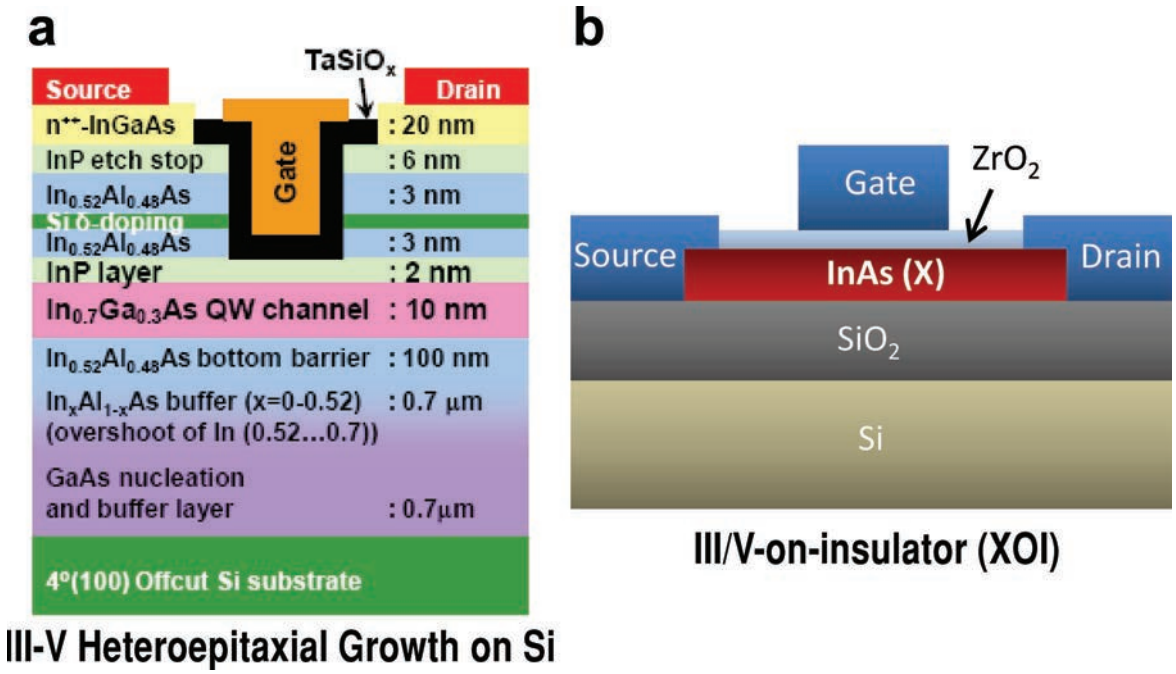

Figure 2. Integration of III–V compound semiconductors on Si substrates by (a) Direct heteroepitaxial growth involving a number of buffer layers. Reproduced with permission from[47]. Copyright 2009 IEEE. (b) Epitaxial layer transfer technique, resulting in III–V on insulator substrates. Reproduced with permission.[7]

transfer of ultrathin III–V layers grown on a III–V source wafer to a Si/SiO_2 receiver substrate using a modified ELT technique (Figure 2b).[7] The approach is an example of the previously discussed XoY concept, in this case, combining the high mobility III–V layers with the well-established silicon technology. The resulting substrates resemble the conventional silicon-on-insulator (SOI) substrates, with the top Si layer replaced with a III–V layer. Thereby, we refer to this III/V-on-insulator technology as XOI. Of particular importance for the realization of high performance XOI MOSFETs is the use of ultrathin layers that are fully or partially depleted. This is particularly important for low bandgap semiconductors, such as InAs (bandgap, E_g ~ 0.36 eV), which exhibit excellent electron mobilities. For such low bandgap semiconductors, an ultrathin body XOI device structure drastically improves the OFF-state leakage currents by removing the body effects and reducing the parasitic source/drain junction areas.

2.1. Epitaxial Layer Transfer Methodology

The process schematic for transferring ultrathin InAs layers (thickness down to ~4 nm) onto Si/SiO_2 substrates is demonstrated in **Figure 3**a.[7] In this approach, the source wafer consists of an InAs/AlGaSb/GaSb stack where InAs is the active layer, AlGaSb is the sacrificial layer and GaSb is the support substrate. The InAs layer is first patterned into ribbons with widths between 300 nm to 5 μm using lithography and wet etching.

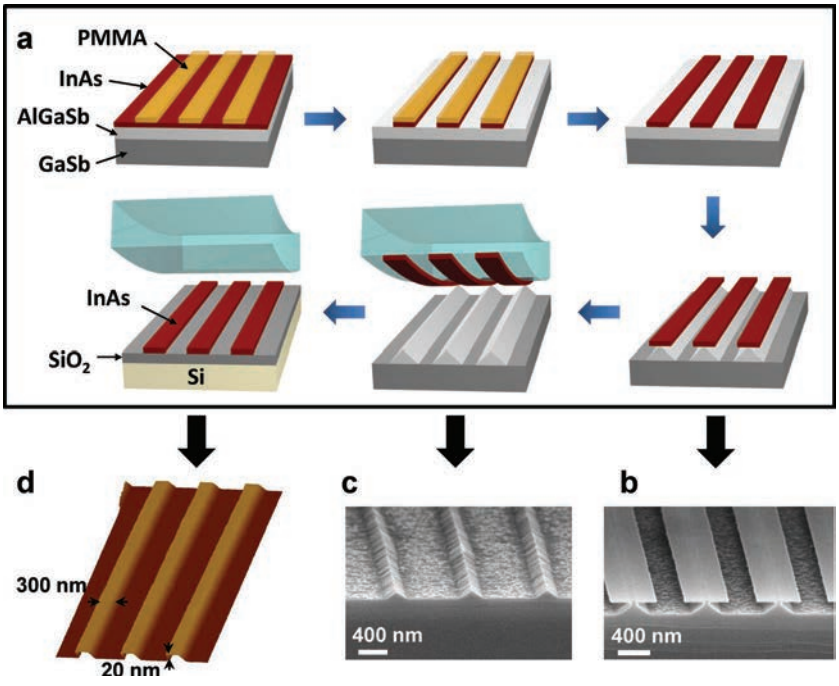

Figure 3. (a) Process schematic for layer transfer of ultrathin III–V semiconductors on to Si/SiO_2 substrates. (b) SEM image of InAs nanoribbons on a partially etched AlGaSb sacrificial layer. (c) SEM image of a partially etched AlGaSb sacrificial layer after InAs nanoribbon transfer. (d) AFM image of transferred InAs nanoribbons with a height of ~20 nm on a Si/SiO_2 substrate. Reproduced with permission.[7]

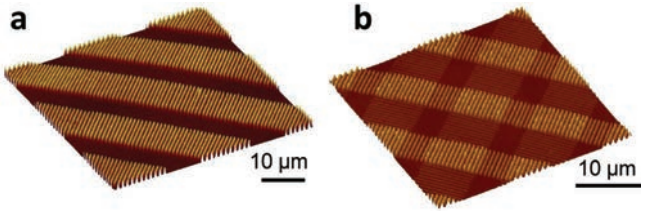

Figure 4. AFM images of ordered arrays of InAs nanoribbons on Si/SiO_2 substrates obtained by (a) a single-step ELT process of ~20 nm thick InAs, and (b) a two-step ELT process of ~20 nm thick (bottom layer) and ~50 nm thick (top layer) InAs, with the layer transfers offset by 90° to form the crossbar patterns. Reproduced with permission.[7]

Next, the AlGaSb sacrificial layer is selectively etched using NH_4OH, in order to partially release the InAs ribbons, as demonstrated in the scanning electron microscope (SEM) image in Figure 3b. The partially released nano- or micro-ribbons were then removed from the GaSb growth substrate by the use of an elastomeric polydimethylsiloxane (PDMS) slab (~2 mm thick), leaving behind only the partially etched sacrificial layer (Figure 3c). HF surface cleaning of the InAs ribbons on PDMS was then performed to ensure the removal of residual sacrificial layer on the back surface. Next the PDMS slab with InAs ribbons were brought in contact with a clean Si/SiO_2 substrate and gently removed. Here, the adhesion force between InAs and SiO_2 surface is found to be higher than that of InAs/PDMS, resulting in the successful transfer of InAs ribbons to the Si/SiO_2 substrate. In Figure 3d, an AFM image depicting transferred InAs nanoribbons with a height of ~18 nm on a Si/SiO_2 substrate is shown. Clearly, the process enables the fabrication of highly uniform InAs XOI substrates (**Figure 4**a). The process also allows for the multi-step transfer of different III–V components on the Si substrate, which adds another capability for multi-functional and/or CMOS circuits. As a proof of concept, a two-step ELT was used to fabricate InAs crossbar structures with the bottom and top layer thicknesses of ~20 and ~50 nm, respectively (Figure 4b).

While we demonstrate the process only for InAs material system, the approach is generic to any III–V compound semiconductor. Here, the etch selectivity between the active and sacrificial layers, and the interface between the insulator and active layers are critical points in order to achieve a successful transfer. For instance, a high etch selectivity between InAs and AlGaSb layers is obtained by using a mixture of citric acid and hydrogen peroxide for InAs etching and ammonium hydroxide for AlGaSb sacrificial layer etching. Moving forward, multi-layer transfer may be utilized to enable the fabrication of p- and n-FETs based on the optimal III–V semiconductors for holes and electrons, respectively, to enable the fabrication of III–V CMOS circuits on Si substrates.

2.2. Strain Engineering of Ultrathin XOI Layers

Strain has a significant effect on the optical and electronic properties of materials, and therefore plays a critical role in the performances of III–V based electronics. Specifically, strain drastically tunes both the band structure (e.g., bandgap) and mobility of semiconductors.[53–55] In the past, by properly adjusting the built-in strain, mobility enhancements of ~2x or more have been observed in various semiconductors.[56] For the XOI platform, this issue is addressed by introducing a cap layer during the ELT process, which depending on its thickness can control the strain from fully relaxed to that of the original as-grown layer (**Figure 5**a).[57]

Ultrathin InAs layers grown on GaSb/AlGaSb substrates are strained by ~0.62%, as determined by the inherent lattice mismatch of InAs and GaSb. When the InAs layers are transferred from the growth substrate, the strain is fully released, resulting in unstrained InAs-on-insulator structures. This is expected since during the ELT process, InAs ribbons are free-standing without being constrained to the lattice structure of the original growth substrate. The relaxed state of InAs XOI was depicted by Raman spectroscopy[57] where the observed longitudinal optical

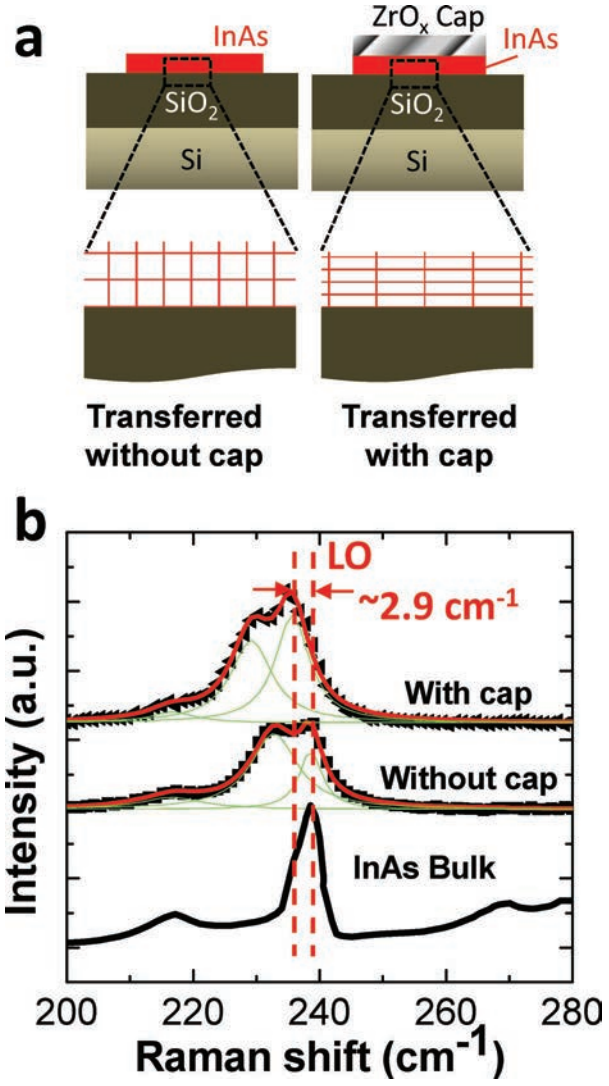

Figure 5. (a) Schematic of the method used for strain preservation. (b) The Raman spectra of InAs layers transferred with and without a ZrO_x cap. The Raman spectrum from bulk InAs[58] is also shown. Reproduced with permission.[57] Copyright 2011, American Institute of Physics.

(LO) phonon peak position at 239 cm^{-1} is the same as that of the InAs bulk substrates (Figure 5b).[58]

By introducing a cap layer with proper design prior to the ELT process, the strain in the material can be successfully preserved. Here, a ZrO_x layer (70 nm thick) is deposited as the cap on the patterned InAs surface prior to wet etching of the sacrificial layer.[57] After etching of the AlGaSb sacrificial layer, the ZrO_x capped InAs ribbons are transferred in a similar manner as previously described. Figure 5 shows the Raman spectra from both capped and non-capped transferred InAs layers on Si/SiO_2. Clearly, the InAs layers transferred with a ZrO_x cap show a Raman redshift of 2.9 ± 1.1 cm^{-1} compared to the InAs layers transferred without a cap (Figure 5b), which can be correlated to an in-plane strain of 0.8 ± 0.3%. One of the multi-faceted integration aspects offered by the XOI platform is illustrated in the strain engineering of the ultrathin III–V layers and is considered to be a key point in further optimizing and increasing the device performances of the enabled devices.

2.3. XOI Atomic Structure: Interfaces of Highly Dissimilar Materials

High-resolution transmission electron microscopy (TEM) was performed in order to characterize the atomic structure of InAs-on-insulator substrates (**Figure 6**).[7] Here, the thickness of InAs is ~13 nm. The single-crystalline, defect-free structure of InAs on an amorphous SiO_2 is clearly depicted. Notably, the SiO_2/InAs interface does not exhibit voids, although it should be noted that only a small cross-sectional area is analyzed by TEM. While providing tremendous opportunities for exploring novel devices, nanoscale XOI structures also present a number of materials challenges. A few examples of these challenges are highlighted schematically in **Figure 7**a. Specifically, an interface roughness of only a few angstroms can be detrimental to the carrier mobility, especially for XOI thicknesses down to a few unit cells (Figure 7b). Here, the surface-roughness limited mobility, μ_{SR} was calculated using an analytical model:

$$\mu_{SR} = \frac{e}{m^*}\left(\frac{\pi^4\hbar\Delta^2L^2}{2m^*t^6{k_f}^3}\int_0^{2k_f} Exp\left[\frac{-q^2L^2}{4}\right]\frac{q^2dq}{(1-(\frac{q}{2k_f})^2)^{0.5}}\right)^{-1} \quad (1)$$

for InAs XOI with a thickness of 4 nm.[59] Where e is the charge of the electron, m^* is the electron effective mass, Δ is the rms surface roughness, L is the autocorrelation length, t = 4nm is the InAs layer thickness, q is the electron wavevector, and $k_f = (2\pi n_S)^{0.5}$ with n_S being the sheet electron density. For this calculation, L = 2 nm (ref. [60]), and $n_S = 3.5 \times 10^{12}$ cm^{-2}, which roughly corresponds to a transistor in the ON-state, were used. Note that this calculation only presents a rough guidline for the expected role of surface roughness in the transport characteristics of ultrathin films. In the future, more detailed atomistic simulations are needed. The interfacial bonding configuration is also essential in determining the fixed and trapped charge densities at the interfaces which can degrade both the carrier mobility and the gate electrostatic control of the device. Finally, given the large Bohr radius of most high mobility III–V semiconductors (e.g., ~34 nm for InAs), control of the thickness down to a single atomic monolayer is critical in order to obtain a uniform material system with deterministic carrier effective mass and band structure. This effect is depicted in Figure 7c, where the InAs bandgap, calculated by using an infinite potential well model,[61] is plotted as a function of thickness, showing drastic size effects for sub-10-nm thick films. Furthermore, the precise positioning of the individual dopant atoms is critical,[62,63] especially for XOI layers with only a few atomic layers thickness. The issues discussed here present some of the basic materials challenges associated with nanoscale semiconductors, which require the control of the composition and structure down to individual atoms. In this regard, future works require the use of new characterization and processing techniques to better understand and control the nanoscale interfaces between highly dissimilar materials.

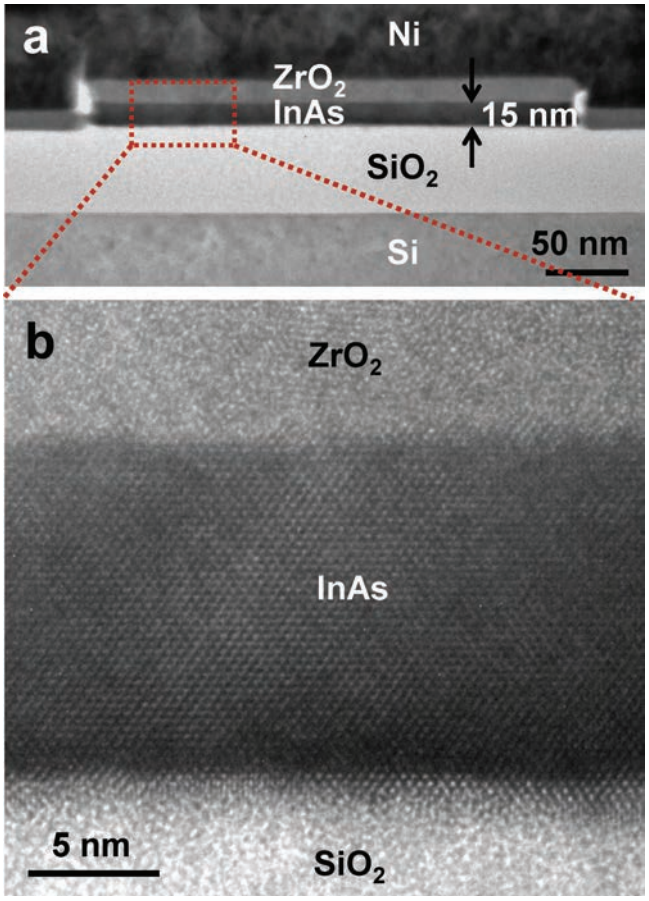

Figure 6. (a), (b) TEM images of an InAs nanoribbon on a Si/SiO_2 substrate. Here, InAs is coated with a ZrO_2/Ni cap which serves as the gate stack for the subsequently fabricated FETs. The interfaces between the crystalline InAs and amorphous SiO_2 and ZrO_2 layers are clearly depicted. Reproduced with permission.[7]

2.4. High Performance, Ultrathin Body XOI Transistors

III–V semiconductors offer the promise of low power transistors for energy efficient electronics due to their high electron mobility. Top-gated FETs on InAs XOI substrates were fabricated

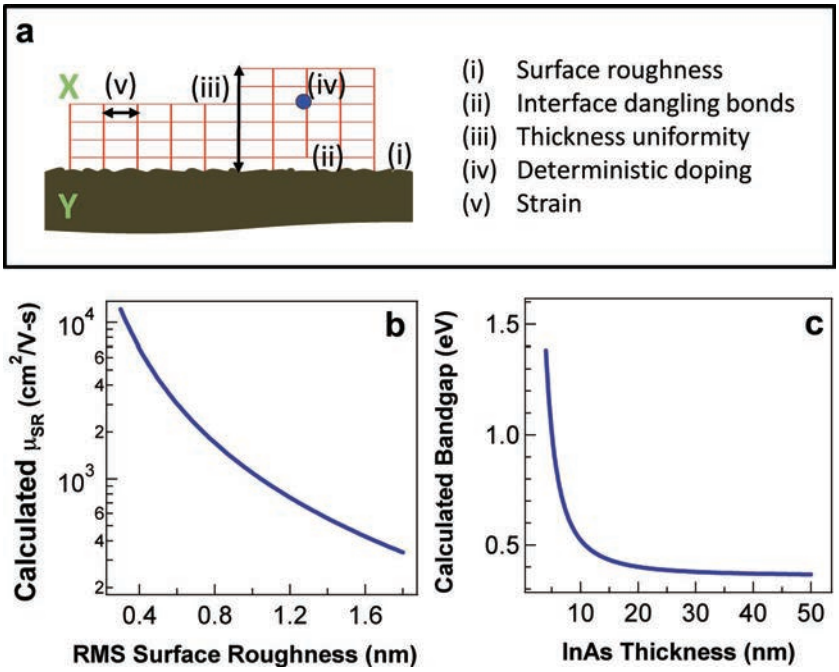

Figure 7. (a) A generic schematic of XoY. (b) Calculated surface-roughness limited mobility as a function of surface/interface roughness for a 4 nm thick InAs. (c) Calculated bandgap of InAs versus thickness.

by the deposition of lithographically patterned Ni source (S) and drain (D) contacts, a ZrO_2 gate dielectric layer (atomic layer deposition, around 8nm), and Ni gate (G) electrodes.[7] Transfer characteristics of a top-gated FET with a channel length of ~500 nm and InAs thickness of ~18 nm are shown in **Figure 8**a. The FETs display a respectable I_{ON}/I_{OFF} ratio of ~10^4, a subthreshold swing, SS ~ 150 mV/decade (lowest measured, ~107 mV/decade) and a peak transconductance, g_m of ~1.6 mS μm^{-1} at S/D voltage, V_{DS} of 0.5 V. The output characteristics of the same device show an ON current as high as 1.4 mA μm^{-1} at an operating voltage of $V_{DD} = V_{DS} = V_G = 1$ V (Figure 8b).[7] Despite the relatively long channel devices used here, both peak g_m and I_{ON} are among the highest reported for III–V devices. The results demonstrate the viability of the XOI concept for high performance MOSFETs. From the long channel devices (L ~ 2–10 μm), the peak field-effect mobility was found to be ~4000 cm^2 V^{-1}s^{-1} for InAs XOI with a thickness of ~13 nm (**Figure 9**). In comparison, the reported Hall mobilities for InAs quantum-well structures is ~13 000 cm^2 V^{-1}s^{-1}.[64] It should be noted that the Hall mobility is typically higher than the field-effect mobility by 2–4x due to a number of device and surface contributions to carrier transport that lower the mobility for a field-effect device. Further work requires optimizing the interface properties for reduced interfacial trap state densities, elucidating the dominant electron scattering mechanisms in XOI FETs, and exploring the channel length scaling limits of XOI FETs.

The thicknesses of the ultrathin layers have been demonstrated to critically affect both OFF currents and mobility of the fabricated FETs. The observed tendency is that the OFF currents decrease with decreasing InAs thicknesses (from 48 to 8 nm) due to an increased electrostatic gate coupling and the transition of the body to partially and fully depleted[7]. Quantum confinement also increases the bandgap and therefore reduces the leakage currents. Furthermore, the mobility is found to decrease as the system is reduced from three-dimensional to two-dimensional at small thicknesses although detailed experimental studies on the precise cause of this observation is on-going. These points stress the importance of the accurate control of the thickness of the active layers in the XOI device architecture.

Other device structures besides MOSFETs can also be readily explored using the XOI material system. For instance, III–V XOI is advantageous for tunneling field effect transistors (TFETs) due to the reduced leakage currents and better electrostatic control of the tunnel junction.[65] Additionally, the XOI platform offers the advantage of incorporating different III–V active layers with a low defect density on insulator (and not limited by the original III–V growth substrate) to enable heterojunction devices with band alignments optimized to achieve a low effective tunneling barrier. The device schematic of a proof-of-concept InAs XOI TFET is shown in **Figure 10**a. The device consists of a gated p+/n tunnel junction at the source contact which enables the modulation of the carrier injection into the channel. Here, InAs XOI (thickness of ~18 nm) was pattern doped by using a Zn surface doping technique[66] to form the *p*+ source contacts.[65] This post-growth, surface doping approach minimizes lattice damage to the InAs XOI compared to ion implantation, and enables a high electrically active dopant concentration of ~10^{19} cm^{-3}.

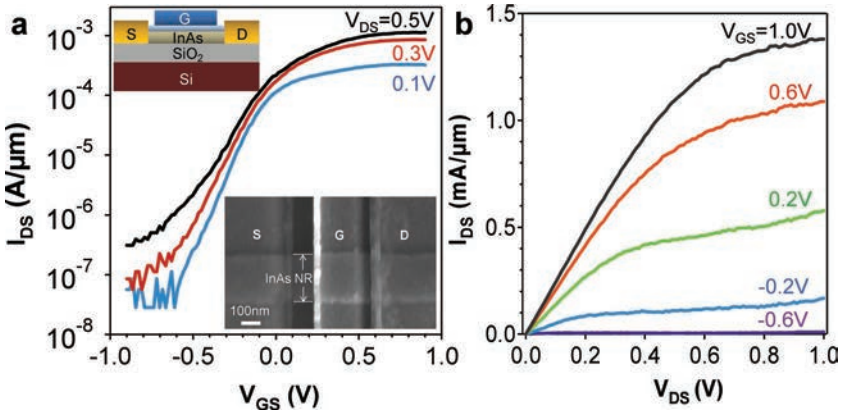

Figure 8. Ultrathin body InAs XOI FETs. (a) Transfer characteristics of a top-gated InAs XOI FET. InAs thickness is ~18nm, the channel length is ~500 nm, and the gate dielectric is ~8 nm thick ZrO_2. The inset shows the device schematic. (b) Output characteristics of the same device. Reproduced with permission.[7]

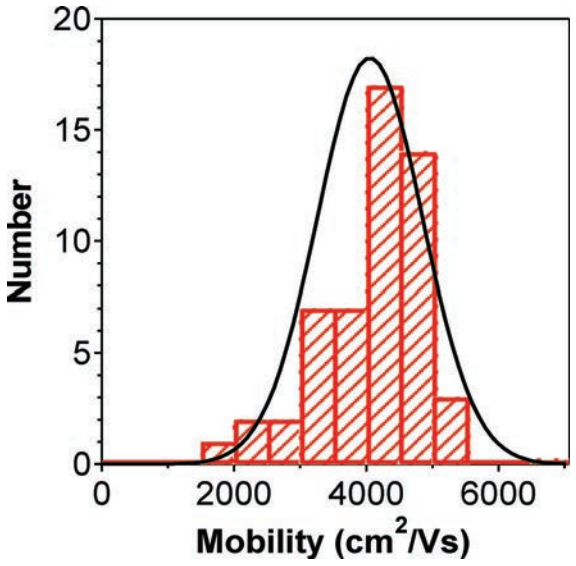

Figure 9. Histogram of the peak field-effect mobility for back-gated InAs XOI devices with $L = 2$–10 μm and InAs thickness of ~13 nm. Reproduced with permission.[7]

The diffusion length of Zn for the doping time and temperature used (~180 nm) is longer than the InAs NR thickness of ~18nm, enabling the entire depth of InAs to be doped.

The *I*–*V* characteristics at room temperature of a representative TFET device (channel length $L \sim 2.5$ μm) are shown in Figure 10b. The device exhibits sub-threshold swings (*SS*) of ~170 mV/dec with an *ON* current density of ~0.5 μA μm^{-1} at $V_{DS} = V_{GS} = 1$ V.[65] These figures of merit are respectable given that a non-ideal dopant, zinc, was used for the p^+ S formation and the TFET has a long channel length of ~2.5 μm. Surface trap states, and/or trap-assisted tunneling (TAT), are likely the reason for the *SS* exceeding 60 mV/decade. For negative V_{DS}, the device is forward biased and, under positive V_{GS}, negative differential resistance (NDR) behavior is observed, clearly confirming the inter-band tunneling mechanism of the device. As the vertical depletion width of <10 nm is significantly smaller than the lateral junction abruptness of ~180 nm achieved by zinc doping, vertical tunneling dominates the band-to-band current, with device performance thereby less sensitive to the lateral junction abruptness. The XOI TFET performance can be improved in the future by reducing the device dimensions, improving the surface properties, using a slower diffusing dopant to create a more abrupt lateral junction, or utilizing a heterojunction III–V materials stack. Nevertheless, the results demonstrate the versatilty of the XOI concept for exploring various material and device architectures on a Si substrate.

3. Large-Scale Nanowire-Array XoY

In the second example, large-scale assembly of NWs ('X') on plastic substrates ('Y') for use as the active back-plane of artificial electronic-skin (e-skin) is discussed. In recent years, integration of inorganic nanowires has been demonstrated on various rigid and flexible substrates,[1,41,67–70] which have led to an increasing exploration of their unique properties within many different applications. First of all, the electrical and optical properties of NWs can be tuned through the precise synthesis of composition, size and shape. Furthermore, they are compatible with large scale integration methods, such as contact printing, which has already been demonstrated as a viable route for obtaining high-throughput fabrication of NW based electronics and sensors. One of the key advantages of

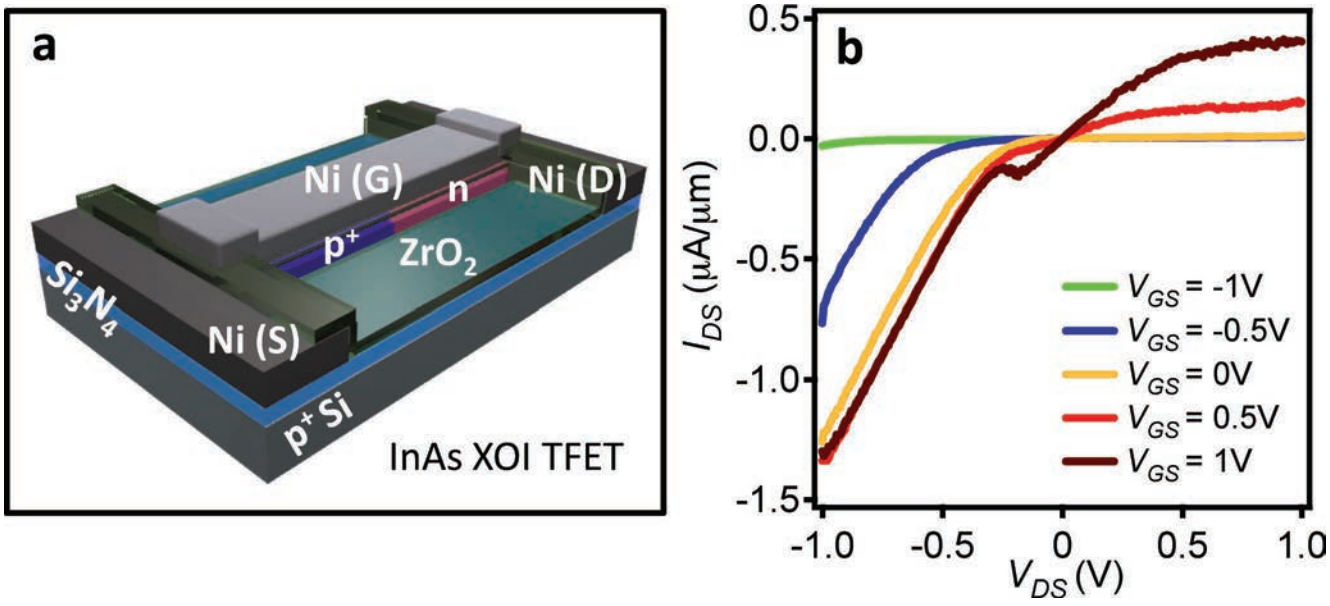

Figure 10. Ultrathin body InAs XOI TFETs. (a) Schematic of a proof-of-concept InAs XOI TFET. (b) Output characteristics of a representative InAs XOI TFET (channel length $L \sim 2.5$ μm and InAs thickness is ~18 nm). Note that the negative bias in this case corresponds to the forward bias condition. The observed NDR clearly depicts the tunneling operation of the device. Reproduced with permission.[65] Copyright 2011, American Institute of Physics.

the NW-based device technology is that single-crystalline NWs can be grown non-epitaxially on low cost amorphous substrates first, followed by their eventual transfer, for instance, by contact printing,[40] as parallel arrays on a desired device substrate using room-temperature processing. This makes the technology compatible with virtually all support substrates and readily enables for heterogeneous integration of NWs with different composition and functionality on substrates through a multi-step assembly process. A challenge however is that while processes such as contact printing enable large-scale, uniform assembly of NW-arrays on substrates, they lack the control in precise placement down to individual NWs at the nanometer scale. As such, single-NW (synthesized by the bottom-up approach) based devices often suffer from large stochastic device-to-device variation and non-uniformity over large areas. On the other hand, devices that utilize parallel NW-arrays, rather than individual NWs, as the active channel material, can be readily fabricated on large-scales with high device-to-device uniformity (**Figure 11**).[71] This platform presents perhaps the most practical device architecture for bottom-up NWs. For macro-electronics, this is particularly ideal since the objective is to cover a large spatial area with an array of devices and therefore, the device scales are often on the order of microns or more. For such applications, NW-array devices present clear technological advantages since (i) the processing is, in principle, highly scalable and compatible with various substrates, (ii) crystalline NWs exhibit excellent electrical and optical properties, mostly similar to their bulk counterparts, and (iii) their miniaturized dimensions make them mechanically flexible. These features combined with the recently developed NW printing processes have shifted the focus from fundamental studies of the properties to nano-manufacturing for practical applications. This presents the newly established field of "*translational nanotechnology*" that bridges the basic science of nanomaterials with applied engineering for their potential product development.

In the context of the above discussion, we here present an interesting application for inorganic NWs, namely artificial e-skin, focused towards multifunctional sensing of in principal any stimuli exerted on a skin-like material, by utilizing the 'XoY' platform.[1] E-skin is a broad concept and can be defined as a highly bendable, ultrathin material that can conformably cover any structure while providing real-time, two-dimensional mapping of an applied external stimuli. The stimuli could include pressure (e.g., touch), temperature, strain (e.g., crack formation), humidity and chemicals, and more. E-skin presents a new class of smart materials, which provides interfacing of a system to the external ambient with high fidelity. As an example system, we demonstrate a pressure-sensitive e-skin device that utilizes NW-arrays as the active matrix back-plane on an unprecedented scale of over 7 cm × 7 cm in area.[1]

3.1. Nanowire Printing Methodology

Transfer of NW-arrays from their growth to a receiver substrate is achieved by employing a contact printing technique, which utilizes shear force in order to assemble NWs in a highly ordered, well aligned manner. This can be performed by a simple print-and-slide technique, in which the growth substrate

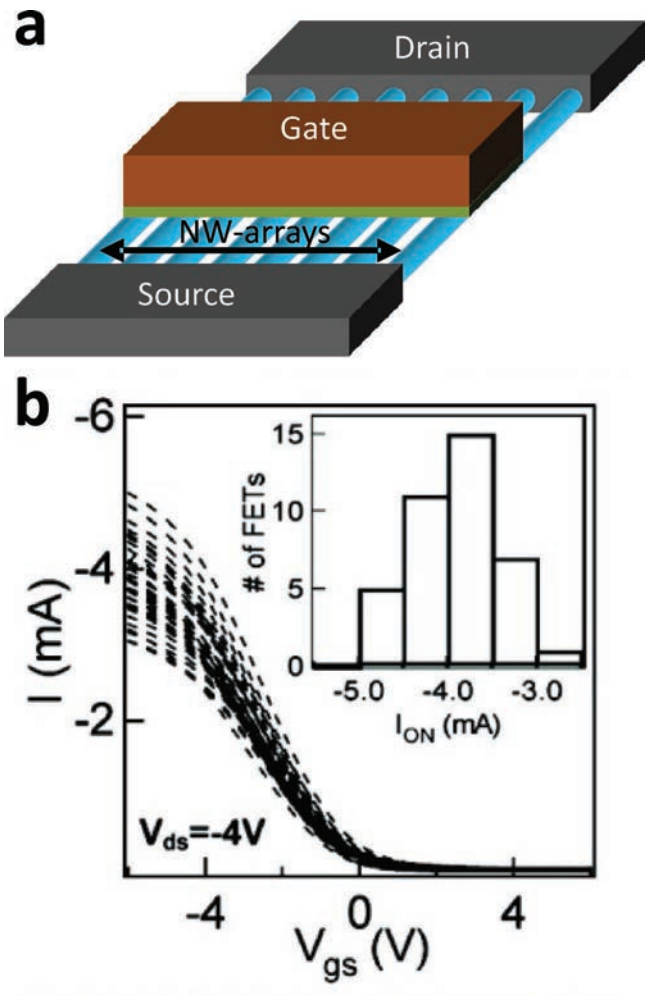

Figure 11. NW-array FETs. (a) Schematic of a top-gated NW-array FET. (b) Linear I_{DS}–V_{GS} curves for 40 Ge/Si NW-array FETs on the same chip with ~2 μm channel length, ~200 μm channel width, and 12 nm HfO_2 gate dielectric. The inset shows a histogram of the ON-current for the FETs with a with a 1-standard deviation variation of only 15%. Reproduced with permission.[71] Copyright 2007 American Chemical Society.

is placed in contact with the receiver substrate and subsequently slid at a constant velocity under an applied normal force.[40,44] During this process, NWs that were randomly (i.e., non-epitaxially) grown on the source substrate effectively get "combed" and aligned by the applied shear force and get transferred to the receiver substrate through surface chemical interactions. In this approach, the density of the printed NWs is controlled by the surface functionalization of the receiver substrate and NWs. Given the weak NW-NW surface interactions in part because of small surface contact area, stacking of NWs is not observed and the process is effectively self-limited to a maximum NW density equivalent to that of a monolayer. Patterned printing on selective regions can be achieved using two different approaches. In one approach, the receiver substrate is coated with a photoresist and patterned by standard lithography processes, followed by NW printing and lift-off of the resist.[40] In a second approach, patterned surface functionalization of the receiver substrate by

"sticky" (e.g., amine terminated) and "non-sticky" (e.g., fluoro carbon terminated) self-assembled monolayers is performed prior to the printing process.[42] NWs only transfer to the sticky regions. The NW printing concept is also compatible with roll based techniques, in which a roller is employed to print grown NWs from a roller to the receiver substrate elucidating the high-throughput capability of the technology. For the artificial e-skin device, integration is performed on a flexible polyimide substrate; however, the process has been demonstrated in the past to work on other substrates, including paper and glass, as well for different types of NWs.[43]

3.2. Artificial Electronic Skin

As an example of a large-scale NW-based electronic system, an artificial e-skin device, capable of touch mapping is demonstrated.[1] Here, Ge/Si core/shell NW-arrays were contact printed on polyimide substrates and used as the active channel material for the transistor back-plane. A pressure sensitive rubber (PSR) was then laminated on top to function as the sensing element. Each pixel consists of a single NW-array FET with the drain connected to the ground through the PSR. PSR consists of carbon black nanoparticles that are embedded in an insulating silicone rubber matrix. In a relaxed state, PSR is insulating, however, when pressed, the nanoparticle spacing is reduced such that current flows by tunneling between the particles, resulting in a drastic change of the conductance.

The e-skin devices were fabricated (**Figure 12**)[1] by spin-coating a polyimide layer (~24 μm in thickness) on a silicon handling wafer followed by electron-beam evaporation of SiO_x as a surface adhesive layer for the subsequent NW printing step. Next, NW-arrays were contact printed on photolithographically pre-patterned regions. Subsequently, source (S) and drain (D) Ni electrodes (~50 nm in thickness), Al_2O_3 gate dielectric (~50 nm in thickness by atomic layer deposition) and Al top gate electrodes (~100 nm in thickness) were fabricated by photolithography and lift-off processes. Parylene (~500 nm in thickness) was then vapor deposited as the insulating spacer layer. Patterned oxygen plasma etching of the parylene layer was performed to fabricate via-holes for electrical connection between the drain of each transistor and the PSR. PSR was then laminated on the top surface followed by the peel-off of the entire e-skin device from the handling wafer, resulting in the highly flexible integrated sensors and electronics.

The NW-array FETs are used as the active matrix circuitry to address individual pixels.[1] The gate (V_{GS}) and drain (V_{DS}) voltages of NW FETs are used for addressing the word (W) and bit (B) lines, respectively. **Figure 13**a displays a photograph of a fully fabricated 19 × 18 pixel-array e-skin device. The device is truly macroscale (7 cm × 7 cm in area)

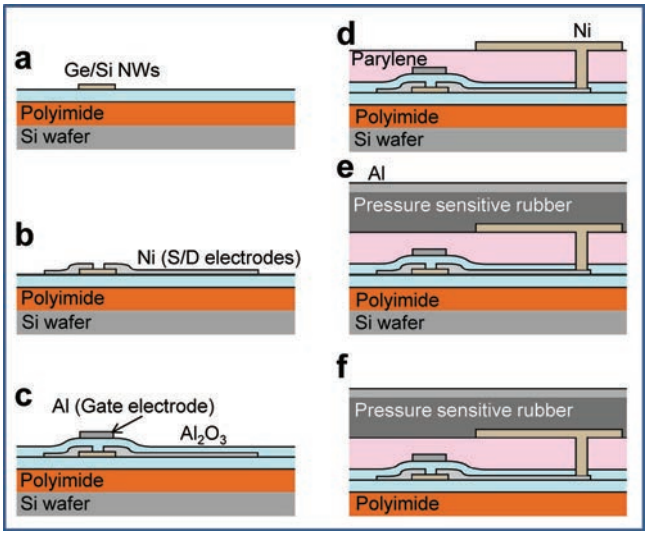

Figure 12. E-skin fabrication process flow. (a) Ge/Si NW-arrays were contact printed onto spun-on polyimide/evaporated SiO_2 on Si wafers. (b) Ni source-drain electrodes were patterned, followed by (c) Al_2O_3 (thickness, ~50 nm) gate dielectric deposition and Al gate electrode patterning. (d) Parylene-C was deposited as a spacer layer, and etched via-holes and deposited Ni pads were made to electrically contact the drain electrodes to the PSR. (e) A PSR with Al GND electrode was laminated on the top. (f) The device was peeled off-from the Si support wafer. Reproduced with permission.[1]

which presents the largest-scale demonstration of ordered NW-array electronics for a fully functional system to date. An optical image of a single pixel is shown in Figure 13b, highlighting the active and passive components. SEM images of a representative

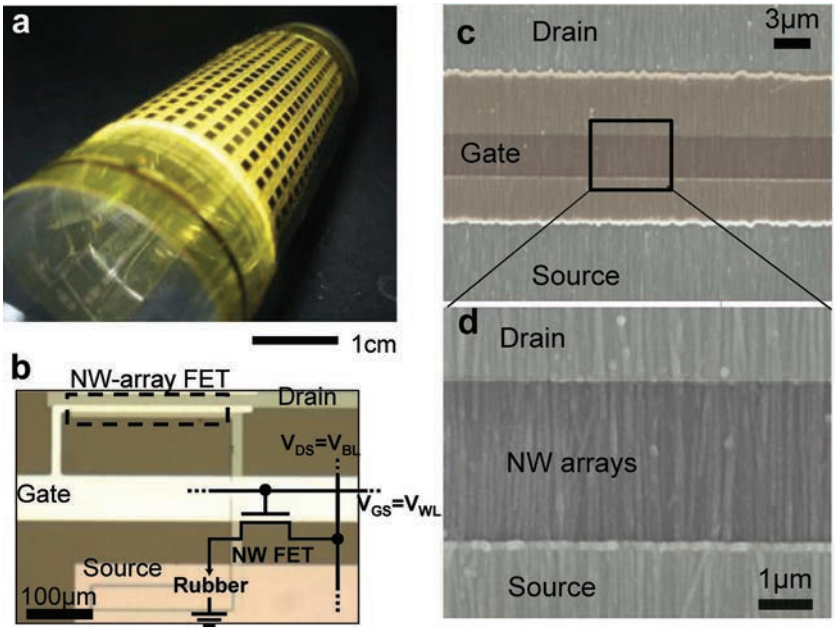

Figure 13. E-skin device with NW active matrix circuitry. (a) A photograph of a rolled 7cm × 7cm e-skin device. (b) An optical image of a pixel, consisting of a NW-array FET. (c), (d) SEM images of a representative Ge/Si NW-array FET with a NW density of ~5 μm^{-1}. Reproduced with permission.[1]

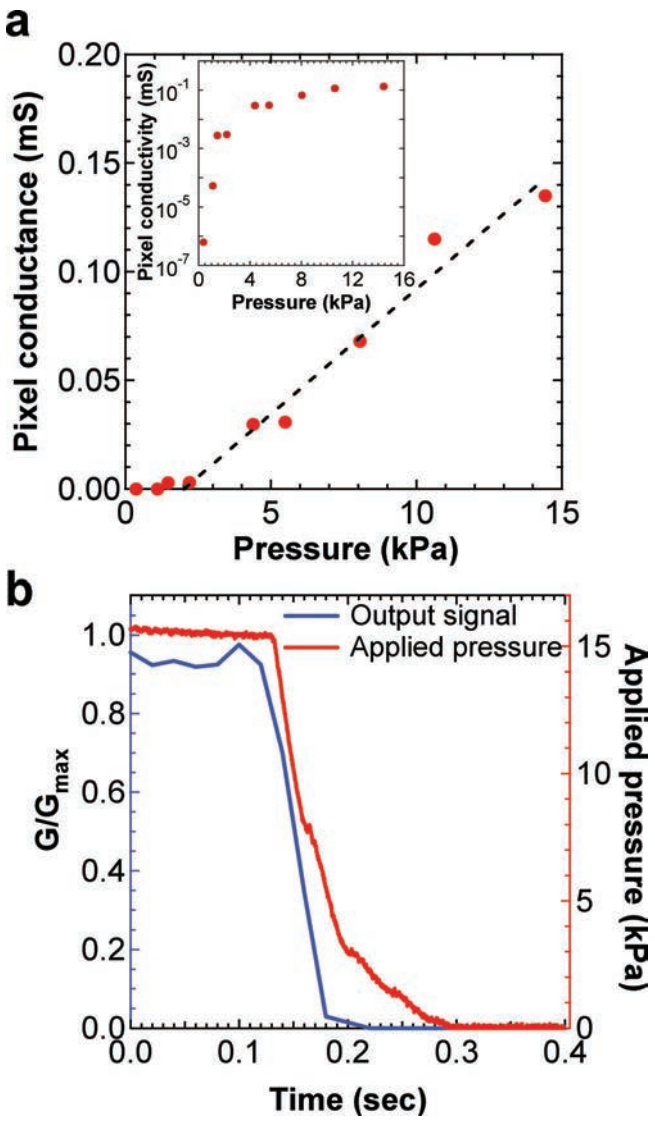

Figure 14. Pressure sensitivity and response time of the e-skin device. (a) Linear-scaled (inset: log-scale) output pixel conductance as a function of the applied pressure at $V_{GS} = V_{DS} = -3$ V. (b) Time resolved measurement of the normalized output signal of a pixel as the pressure is released, showing a response time of <0.1 s. Reproduced with permission.[1]

NW-array FET used for driving a pixel is shown in Figure 13c,d, clearly depicting the ordered NW assembly between the S/D contacts. The e-skin device exhibits high sensitivity to an applied normal pressure for $P = 0.1$–15 kPa (**Figure 14**a). In the linear operation regime ($P >$ ~2 kPa), the sensor sensitivity is $S = dG/dP = 11.5$ μS kPa^{-1}, where G is the ON-state conductance of a single pixel. Notably, the sensor exhibit a fast response and relaxation time of <~0.1 s (Figure 14b).

To demonstrate the functionality of the e-skin device (**Figure 15**a), a piece of polydimethylsiloxane (PDMS), molded as the letter 'C' and with an area of ~ 3 cm^2 was placed on top of the device and a normal pressure of ~15 kPa was applied.[1] The output pressure distribution is successfully mapped by monitoring the output conductance of each pixel by applying a word line voltage, $V_W = V_{GS} = 5$ V and bit line voltage, $V_B = V_{DS} = 0.5$V as depicted in Figure 15b. Notably, due to the use of inorganic NW-arrays as the active switching elements, the devices are operated at low voltages of <5 V and with a respectable device yield of ~84%. The low voltage operation presents an important advantage of using inorganic semiconductors as compared to their organic counterparts that often require operating voltages of >10 V. Further downscaling of the operating voltage and pixel resolution can be achieved by shrinking the device sizes, for example by using shorter channel length and thinner gate dielectric.

3.3. Mechanical Flexibility of Nanowire Based Electronics

Implementation of inorganic NW electronics on flexible substrates relies crucially on the ability to repeatedly bend the integrated structures without affecting the device performances reversibly or permanently. In this aspect, the mechanical flexibility and robustness of NW-array FETs on polyimide substrates with a parylene passivation layer were investigated. **Figure 16**a shows the normalized change in the conductance $\Delta G/G_o$, where $\Delta G = G - G_o$, G and G_o are the ON-state conductance for the bent and relaxed states, respectively as a function of curvature radius.[1] Here, the NWs are bent along their axial direction (Figure 16a inset). Clearly, only a small change in the conductance is observed as the devices are bent to a small bending radius down to 2.5 mm. Furthermore, the excellent mechanical robustness of the devices is demonstrated by measuring $\Delta G/G_o$ as a function of bending cycles (Figure 16b). Here, each bending cycle corresponds to a transition from the initial relaxed state (i.e., radius of curvature of infinity) to a bent state with a radius of curvature of ~10 mm. Minimal change in the output conductance of the FETs is observed, even after 2000 bending cycles. From finite-element method simulations, the strain along the length of the NWs is found to be only ~0.35% for a curvature radius of 2.5 mm for the explored device architecture. This is expected given that the Young's moduli for the metal, dielectric and NW layers are approximately two orders of magnitude higher than those of the parylene and polyimide surrounding layers. In addition, the thicknesses of all inorganic layers are <100 nm, resulting in most of the strain in the device being accommodated by the inactive organic layers. These findings highlight the superb mechanical flexibility of NW-based devices.

3.4. Performance Limits of Bendable NW-Array FETs

Moving forward, more complex NW-based systems are envisioned. In this regard, detailed characterization of NW-array FETs on flexible substrate is needed to understand their performance limits. Of particular importance for a number of circuit applications is the radio frequency (RF) response of the FETs. InAs NW-array FETs with ground-signal-ground configuration were fabricated on polyimide substrates for RF measurements (**Figure 17**a-c).[45] The flexible transistors display an impressive cut-off frequency of f_t ~ 1.08 GHz and a maximum frequency of oscillation f_{max} ~ 1.8 GHz at $V_{DS} = 3$ V(Figure 17d), clearly demonstrating that the NW-array electronics can operate in the ultrahigh frequency (UHF) regime, even with relatively

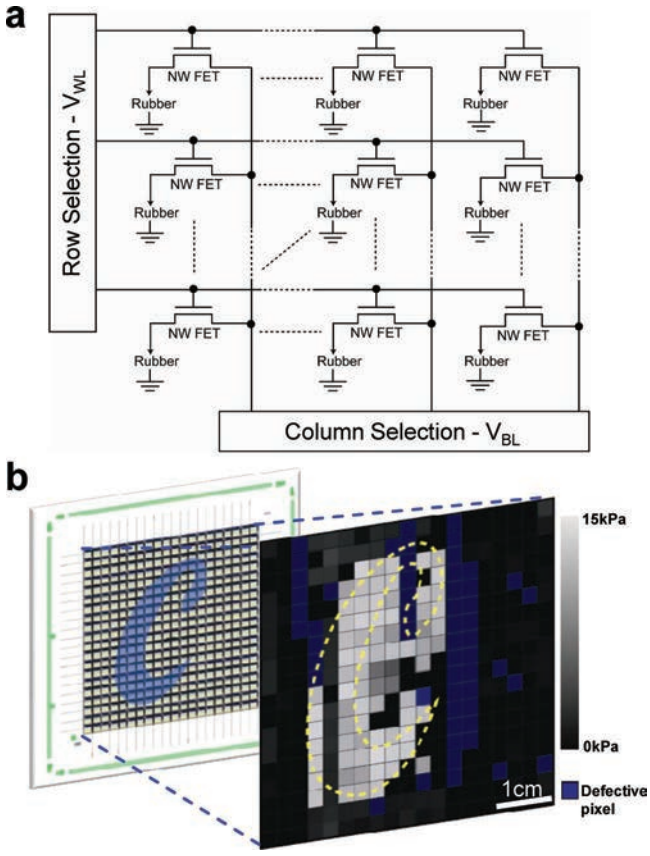

Figure 15. Fully integrated NW active matrix circuitry. (a) Circuit diagram of the e-skin device. Pressure distribution is mapped by scanning of row (V_{WL}) and column (V_{BL}) selection. (b) Two-dimensional pressure mapping of a letter "*C*", corresponding to the object placed on top of the device. Reproduced with permission.[1]

long channel lengths (L ~ 1.5 μm).[45] Notably, for NW RF applications, InAs is an attractive material system because (i) ohmic metal contacts can be readily obtained without chemical doping,[72] and (ii) the electron effective mobility is as high as ~5000 $cm^2\ V^{-1}\ s^{-1}$.[70] From the previously reported mobility and electron drift velocity of bulk InAs, an optimized cut-off frequency f_t > 10 GHz is projected, which may be achieved, for instance, by further enhancing the NW-array density and surface/interface quality.[45] In addition, the performance can be significantly improved by miniaturizing the device dimensions.

4. Conclusions and Outlook

In this Progress Report, recent developments in the integration of nanoscale inorganic semiconductors on various substrates for electronic and sensor applications are discussed. The integration methods rely on specific transfer techniques in which nanostructures of different size and shape are transferred from a growth to a device substrate in a manner, that allows for the free choice of both nanostructure (X) and substrate (Y). The transfer methods provide both the spatial control of the nanostructures in terms of position and orientation, which leads to well-aligned nanostructures in specified positions and over large areas.

In this work, we have focused on ultrathin layers and nanowires as the nanoscale elements for integration on both flexible and rigid substrates. In one approach, the epitaxial transfer of single crystalline, ultrathin III–V layers has been demonstrated as a promising method for fabrication of low-power and high-speed electronics on a conventional Si platform. As a proof-of-concept, a specific class of high performance n-type FETs based on ultrathin body InAs on Si has been fabricated with the potential of lowering the operating voltage (i.e., power) of CMOS circuits, which presents an important advance in the field. Moving forward, exploring the performance limits of InAs-on-insulator devices with short channels (i.e., sub-50 nm) is needed to benchmark their characteristics against those of the conventional Si MOSFETs. In addition, better understanding of the properties of highly dissimilar XoY interfaces, and the various size-effects on the band structure and carrier transport properties are needed. Finally, while InAs is an attractive material system for *n*-FETs, a comparable material system with a high hole mobility for *p*-FETs still needs to be developed to enable complementary III–V circuits on Si.

In a second approach, integration of inorganic NW-arrays, synthesized by the bottom-up technique, for use in flexible electronics is demonstrated. Here, we have focused on an artificial e-skin device based on printed NW-arrays as the switching elements of an active-matrix back-plane. The work presents the largest-scale integration of ordered nanoscale materials for a functional system, and paves the way for the establishment of the field of translational nanotechnology, where the emphasis is to bridge the fundamental nanoscience with applied engineering. It should be noted that the projects discussed in this Progress Report represent only a subset of the recent developments in the field, with the focus being on the directions

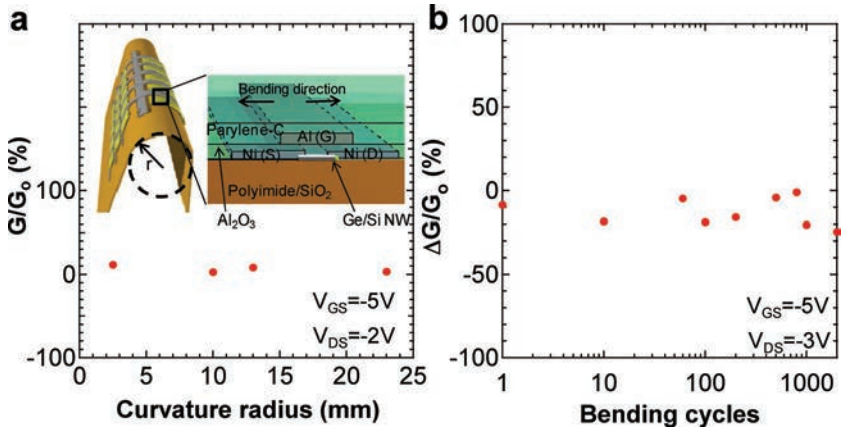

Figure 16. Mechanical reliability of mechanically flexible, NW-array FETs. (a) ON-state conductance change, $\Delta G/G_o$, of a NW-array transistor with bending up to 2.5 mm radii. The inset shows the schematic of the device. (b) $\Delta G/G_o$ as a function of bending cycle, showing minimal degradation even after 2000 cycles. Reproduced with permission.[1]

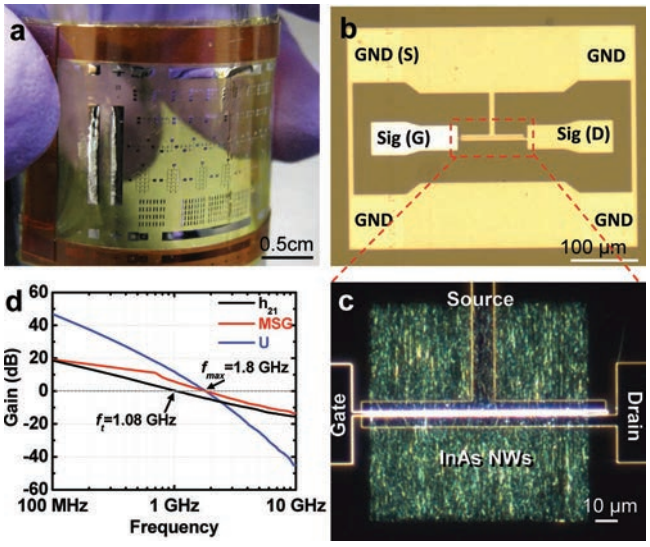

Figure 17. RF characterization of mechanically flexible, InAs NW-array FETs. (a) Optical image of the fabricated devices on a polyimide substrate. (b)-(c) Optical images of a single FET with the ground-signal-ground configuration. (d) Maximum stable gain (MSG), current gain (h21), and unilateral power gain (U) as a function of frequency extracted from measured S-parameters. Reproduced with permission.[45] Copyright 2010, American Chemical Society.

explored in our laboratory. The field has undoubtedly seen enormous progress over the past decade with numerous materials, structures, and device concepts being actively explored using the XoY architecture. As outlined in this report, many exciting opportunities and challenges lie ahead.

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