

Heterojunction Vertical Band-to-Band Tunneling Transistors for Steep Subthreshold Swing and High ON Current

Kartik Ganapathi, and Sayeef Salahuddin

Abstract—We propose a heterojunction vertical tunneling field-effect transistor and show using self-consistent ballistic quantum transport simulations that it can provide very steep subthreshold swings and high ON current, thereby improving the scalability of TFETs for high performance. The turn-on in the pocket region of the device is dictated by the modulation of heterojunction barrier height. The steepness of turn-on is increased because of simultaneous onset of tunneling in the pocket and the region underneath and also due to the contribution of vertical tunneling in the pocket to the current. These factors can be engineered by tuning heterojunction band offsets.

Index Terms—Ballistic quantum transport, band-to-band tunneling, heterojunction, steep subthreshold.

I. INTRODUCTION

THE INTEREST in band-to-band tunneling field-effect transistors (TFETs) has gained traction over the recent years with their demonstration in various material systems of the ability to provide subthreshold swings (SS) steeper than 60 mV/decade at room temperature—a fundamental limit in classical MOS devices—thereby providing a possible route to scaling down voltage and power [1]–[4]. However, the presence of tunneling resistance in the ON state of the device severely inhibits the scalability of TFETs for high performance. One of the proposed device structures to overcome this limitation involves having a heavily doped halo (pocket) region in the gate-to-source overlap region of a conventional p-i-n TFET geometry and hence introducing an additional component of tunneling current due to band overlap along the body thickness, amounting to an increased tunneling area [5]–[8]. From hereon, for brevity, we will refer to this device structure as vertical TFET (VTFET) indicating that the dominant tunneling current component is in the direction normal to the semiconductor–dielectric interface, while the regular p-i-n TFET structure will be referred to as lateral TFET (LTFET) denoting the fact that the tunneling is predominantly in the direction of transport. Recent electronic transport simulations of III–V VTFETs have not shown significant improvement in turn-on characteristics in comparison to LTFETs, although an

Manuscript received December 30, 2010; accepted January 30, 2011. Date of publication March 21, 2011; date of current version April 27, 2011. This work was supported in part by the FCRP Center on Functional Engineered and Nano Architectonics and in part by the National Science Foundation.

The authors are with the Department of Electrical Engineering and Computer Sciences, University of California Berkeley, CA 94720 USA (e-mail: kartik@eecs.berkeley.edu; sayeef@eecs.berkeley.edu).

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2011.2112753

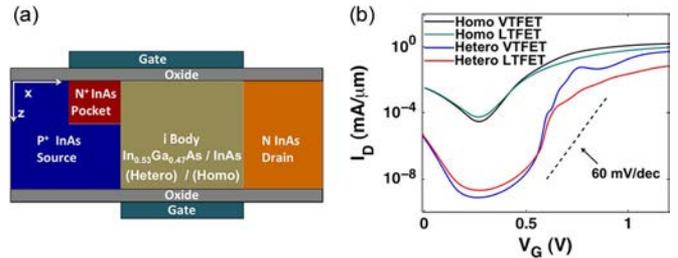


Fig. 1. (a) Schematic of the simulated homo- and hetero-VTFET devices. (b) I_D - V_G characteristics of homo- and hetero-VTFETs at $V_D = 0.4$ V. Similar characteristics are shown for the case of hetero-LTFET for comparison sake. The hetero-LTFET has top gate extending over the body alone. The steepest SS obtained in case of homo- and hetero-VTFETs are 62 mV/decade (from $V_G = 0.375$ to 0.4 V) and 16 mV/decade (from $V_G = 0.575$ to 0.6 V), respectively. The black and green curves in (b) are identical to blue and black curves in Fig. 2(a) in [7] respectively, except for a shift in OFF state voltage done for comparison purposes.

increased ON current is observed [7]. In this letter, we propose a VTFET with wide bandgap material in the channel region (hetero-VTFET from now on), in contrast to the heterojunction LTFET [9]–[12], and show using self-consistent ballistic quantum transport simulations with realistic multiband Hamiltonian that such a device can offer greatly improved OFF state and turn-on behavior while still providing high ON current owing to pocket geometry. We investigate the physics underlying the turn-on characteristics and the factors governing the steepness of SS. Our results provide insight into the directions for optimization of VTFET geometry thereby improving TFET scalability.

II. SIMULATION APPROACH

The structure of the simulated device is shown in Fig. 1(a). The doping concentrations in source, pocket, and drain are 5×10^{19} , 5×10^{19} , and 5×10^{18} cm^{-3} , respectively. The asymmetry in the doping concentrations of source and drain is motivated by the lower conduction band density of states in III–V materials and the need to inhibit ambipolar conduction. The channel is assumed to have an n-type doping of 1×10^{15} cm^{-3} to account for unintentional doping arising due to defects. The source, channel, and drain are 20 nm long each, while the pocket is 10 nm wide and 3.6 nm deep. We use a body thickness of 10 nm. A 1.2-nm-thick dielectric with $\kappa = 15.4$ is used as the gate insulator. The crystallographic direction for transport is (100), and the body is confined along (001) direction. For comparison between device structures, the workfunction difference between semiconductor and gate is adjusted so that the OFF

state occurs at the same gate voltage. The alloy composition of $\text{In}_x\text{Ga}_{1-x}\text{As}$ is chosen such that the band offsets of the channel with that of the source facilitate simultaneous onset of lateral and vertical tunneling in the device—details of which will be explained in a subsequent section.

We use a 4×4 $k \cdot p$ Kane's second-order Hamiltonian to describe the band structure of InAs and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ [13]. The spurious states in dispersion relations—an artifact arising due to confinement—are removed following the prescription in [14]. Spin-orbit coupling is neglected to reduce computation time. Also, we ignore the effect of strain in our heterostructures. The bandgaps of InAs and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ are thus estimated to be 0.5437 and 0.9130 eV, respectively. Band offsets are assumed to be in the same ratio as that of the corresponding bulk materials.

We perform 2-D ballistic transport simulations within the nonequilibrium Green's function (NEGF) formalism with the said multiband Hamiltonian description, thereby implicitly accounting for all tunneling paths. In all our simulations, both gates are maintained at identical electrostatic potential. The width of the device is assumed to be large. Hence, a periodic boundary condition is used, and the momentum modes are summed numerically in the calculation of charge densities and current. The electrostatic potential and the electron and hole concentrations are computed self-consistently by iteratively solving Poisson and NEGF equations.

III. RESULTS AND DISCUSSION

A. Transfer Characteristics

Fig. 1(b) shows the plot of drain current I_D as a function of gate voltage V_G for homogenous VTFET (homo-VTFET henceforth) and hetero-VTFET devices. Similar characteristics are shown for homo- and hetero- LTFETs on the same plot for reference purposes. A drain voltage V_D of 0.4 V is used throughout. Evident from the characteristics is the fact that hetero-VTFETs provide significant reduction in OFF state leakage as compared to their homogenous counterparts. They also provide much steeper SS (a minimum SS of 16 mV/decade versus 62 mV/decade in homo-VTFETs). Although a reduction in ON current, as expected, is observed due to staggered bands at the heterojunction, the pocket geometry, by virtue of boosting the current due to vertical tunneling, reduces this penalty in comparison to LTFETs.

B. OFF State

The OFF state behavior of a hetero-VTFET can be understood by examining the energy band diagram and energy resolved current $I(E) (= T(E) \times (f_1(E) - f_2(E)))$ where $T(E)$ is the transmission coefficient at a given energy E , and f_1 and f_2 are the Fermi-Dirac distributions corresponding to source and drain electrochemical potentials respectively, plotted in Fig. 2(a) and (b) respectively for homo- and hetero-VTFETs. The smaller OFF state leakage in hetero-VTFETs is due to two reasons: 1) larger barrier height due to band discontinuities; and 2) larger effective mass m^* in the channel ($0.046m_0$ at the bottom of conduction band in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ versus $0.032m_0$

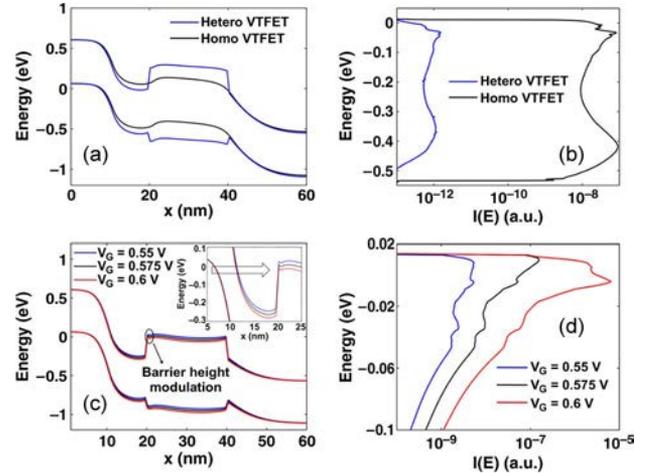


Fig. 2. (a) Energy band diagrams in homo- and hetero-VTFETs at $z = 0$ (semiconductor–top gate insulator interface) at $V_G = 0.25$ V which corresponds to OFF state. (b) Corresponding energy resolved current $I(E)$. (c) Energy band diagrams in hetero-VTFET at $z = 0$ for three gate voltages in the region of steep turn-on. Inset: pocket-channel interface region zoomed in. The arrow in the inset shows the energy window where majority of tunneling current flows. (d) $I(E)$ in hetero-VTFET for the same gate voltages as in (c).

in InAs, m_0 being the free electron mass) implying a smaller wavefunction penetration.

C. Turn-On Mechanism

We now turn to explain a fundamental difference in the turn-on mechanism of a VTFET in comparison to that of an LTFET. The potential profiles along the length of the device in hetero-VTFET near the semiconductor–top gate insulator interface are plotted in Fig. 2(c) for three different gate voltages in the region where the turn-on is the steepest. We note that this steep turn-on corresponds to the transition wherein the peak in $I(E)$, shown for corresponding gate voltages in Fig. 2(d), moves from below the barrier at the heterojunction to above it. It can be seen from the inset of Fig. 2(c) that the tunneling width in the energy region where most of the current flows remains virtually unchanged during this transition. This is in stark contrast to the case of LTFET turn-on where barrier *width* and not *height* is modulated. Two important clarifications are in order here: 1) the steep turn-on is *not* sensitive to the sharpness of the barrier at the heterojunction interface, and any broadening of this barrier introduced by a scattering mechanism will manifest only as a shift in the turn-on voltage. This is due to the fact that the $p^+ - n^+$ tunnel junction at the source–pocket interface is always turned on, by virtue of doping, as can be seen in Fig. 2(c); and 2) while the turn-on mechanism should be identical in homo-VTFET, the phenomenon is masked because of large lateral tunneling current akin to LTFET current that flows underneath the pocket as evidenced by the presence of tunneling states in a plot of logarithmic local density of states (LDOS) along the length of homo-VTFET, near the semiconductor-back gate insulator interface, shown in Fig. 3(b).

D. Factors Affecting Steepness

There are two other reasons for greater steepness in the turn-on of a hetero-VTFET: 1) the onset of lateral tunneling

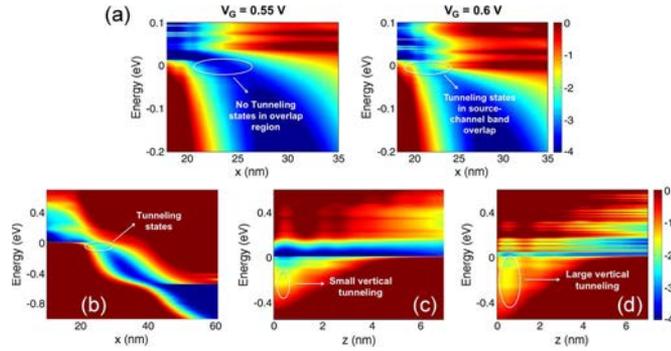


Fig. 3. (a) Plots of logarithmic LDOS in hetero-VTFET at $z = 10$ nm (semiconductor-back gate insulator interface) at $V_G = 0.55$ and 0.6 V. (b) LDOS plot in homo-VTFET at $z = 10$ nm at $V_G = 0.375$ V. (c) and (d) LDOS plots along body thickness at $x = 15$ nm (middle of pocket region) in homo ($V_G = 0.375$ V) and hetero ($V_G = 0.575$ V) VTFETs, respectively.

underneath the pocket together with tunneling in the pocket region. Fig. 3(a) shows logarithmic LDOS plots in hetero-VTFET near the back gate for $V_G = 0.55$ V and 0.6 V. We observe that, owing to the optimum choice of band discontinuities between source and channel materials, unlike homo-VTFET where the onset of lateral tunneling precedes turn-on in pocket region as explained before, in case of hetero-VTFET, it occurs simultaneously; and 2) the contribution of vertical tunneling component of current during steep turn-on. It must be observed that while vertical tunneling contributes to a larger ON state current in case of homo-VTFETs too, it does not lead to steeper swing as it sets in at large gate voltages wherein the device is already turned on. However, since turn-on voltage in hetero-VTFETs is larger owing to heterojunction band offsets, vertical tunneling does contribute to steepness of SS. The LDOS plots along the body thickness in the middle of pocket region of homo- and hetero-VTFETs during their steepest turn-on, shown in Fig. 3(c) and (d), respectively, indicate the presence of greater density of tunneling states in the latter.

E. Negative Transconductance

An interesting feature of the I_D - V_G characteristics of hetero-VTFET is a region of negative transconductance between $V_G = 0.775$ V and 0.85 V. Our simulations show that the negative transconductance arises due to resonance between tunneling states in the pocket region and states in the channel—the density of which is nonmonotonic near the bottom of conduction band, due to the difference in dispersion relations of InAs and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. The higher current at lower V_G is due to higher density of states in the channel coupling to tunneling states in the pocket that carry the majority of the current. The subsequent increase in I_D for large V_G is due to the appearance of increasing number of tunneling states in the pocket, many of which propagate through states far above the bottom of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ conduction band in the channel.

IV. CONCLUSION

Our simulations have shown that the turn-on in a hetero-VTFET is governed by the modulation of heterojunction barrier height as opposed to tunneling width modulation in case of LTFETs. We have also demonstrated that, by choosing the right

band offsets, the steepness of turn-on can be increased owing to the following: 1) simultaneous onset of tunneling in the pocket and the region underneath it; and 2) vertical tunneling contribution. The negative transconductance region that can occur in hetero-VTFET characteristics is explained to be due to resonant tunneling between states in the pocket and the channel. Although in this study we have restricted ourselves to nominal device structures so as to retain our emphasis on underlying physics, we note that enhanced performance can be obtained by optimizing the critical device parameters like heterojunction band offsets (tuned using Ga mole fraction), pocket width and depth, and doping profiles in source and pocket regions, thus fully leveraging the advantages of hetero-VTFETs.

ACKNOWLEDGMENT

The authors would like to thank the NSF Center for Computational Nanotechnology for the computing resources.

REFERENCES

- [1] W. Y. Choi, B.-G. Park, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.
- [2] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-gate strained-Ge heterostructures tunneling FET (TFET) with record high drive currents and <60 mV/dec subthreshold slope," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–3.
- [3] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196805, Nov. 2004.
- [4] S. Mookerjee, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu, and S. Datta, "Experimental demonstration of 100 nm channel length $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ -based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications," in *IEDM Tech. Dig.*, Dec. 2009, pp. 949–951.
- [5] P. Patel, K. Jeon, A. Bowonder, and C. Hu, "A low voltage steep turn-off tunnel transistor design," in *Proc. SISPAD*, 2009, pp. 23–26.
- [6] A. Bowonder, P. Patel, K. Jeon, J. Oh, P. Majhi, H.-H. Tseng, and C. Hu, "Low-voltage green transistor using ultra shallow junction and hetero-tunneling," in *Proc. Ext. Abstr. 8th IWJT*, 2008, pp. 93–96.
- [7] K. Ganapathi, Y. Yoon, and S. Salahuddin, "Analysis of InAs vertical and lateral band-to-band tunneling transistors: Leveraging vertical tunneling for improved performance," *Appl. Phys. Lett.*, vol. 97, no. 3, pp. 033504-1–033504-3, Jul. 2010.
- [8] S. Agarwal, G. Klimeck, and M. Luisier, "Leakage-reduction design concepts for low-power vertical tunneling field-effect transistors," *IEEE Electron Device Lett.*, vol. 31, no. 6, pp. 621–623, Jun. 2010.
- [9] E.-H. Toh, G. H. Wang, G. Samudra, and Y.-C. Yeo, "Device physics and design of germanium field-effect transistor with source and drain engineering for low power and high performance applications," *J. Appl. Phys.*, vol. 103, no. 10, p. 104504, May 2008.
- [10] A. S. Verhulst, W. G. Vanderberghe, K. Maex, S. De Gendt, M. M. Heyns, and G. Groeseneken, "Complementary silicon-based heterostructure tunnel-FETs with high tunnel rates," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1398–1401, Dec. 2008.
- [11] O. M. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt, and D. A. Antoniadis, "Design of tunneling field-effect transistors using strained-silicon/strained-germanium type-II staggered heterojunctions," *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 1074–1077, Sep. 2008.
- [12] K. Boucart, W. Riess, and A. M. Ionescu, "Lateral strain profile as key technology booster for all-silicon tunnel FETs," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 656–658, Jun. 2009.
- [13] D. Gershoni, C. H. Henry, and G. A. Baraff, "Calculating the optical properties of multidimensional heterostructures: Application to the modeling of quaternary quantum well lasers," *IEEE J. Quantum Electron.*, vol. 29, no. 9, pp. 2433–2450, Sep. 2008.
- [14] B. A. Foreman, "Elimination of spurious solutions from eight-band $k \cdot p$ theory," *Phys. Rev. B, Condens. Matter*, vol. 56, no. 20, pp. R12748–R12751, Nov. 1997.