Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness

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The effect of body thickness (5-13 nm) on the leakage currents of top-gated, InAs-on-insulator field-effect-transistors with a channel length of ~200 nm is explored. From a combination of experiments and simulation, it is found that the OFF-state currents are primarily dominated by Shockley Read Hall recombination/generation and trap-assisted tunneling. The OFF currents are shown to decrease with thickness reduction, highlighting the importance of the ultrathin body device configuration. The devices exhibit promising performances, with a peak extrinsic and intrinsic transconductances of ~1.7 and 2.3 mS/μm, respectively, at a low source/drain voltage of 0.5 V and a body thickness of ~13 nm. © *2011 American Institute of Physics*. [doi:10.1063/1.3636110]

High-mobility semiconductors have been actively explored in the recent years for use as the channel material of field-effect transistors (FETs) to enable low-power and high-speed electronics.[1–6] In this regard, the use of ultrathin layers of III-V semiconductors on conventional Si substrates has been recently explored, taking advantage of the excellent electrical properties of III-Vs along with the well-established processing technology of Si.[3,5] Two distinct approaches have been proposed; one utilizing the direct epitaxial growth of complex multilayers on Si[3,7] and the other involving the layer transfer of ultrathin films from a III-V source wafer onto a Si/SiO_2 handling substrate.[5,6] The latter structure is termed III-V-on-insulator or "XOI" (Refs. 5 and 8) in resemblance to the conventional Si-on-insulator (SOI) technology. To date, high mobility InAs XOI n-FETs have been experimentally reported with the effective electron mobility of $\mu_n = 1000$–$5000\ cm^2/Vs$ for a body thickness of $T_{InAs} = 7$-18 nm (Ref. 5). These initial results are highly promising, and set the need for an in-depth exploration of the performance limits of the enabled transistors, especially when scaled to short channel lengths, L_G. Here, we report on the detailed device characterization of top-gated XOI FETs with $L_G \sim 200$ nm as a function of T_{InAs} in order to better understand the operation of the devices through experiments and simulations. The gate delays of the devices are also extracted and benchmarked against other transistor technologies, shedding light on the potential of the XOI technology.

Ultrathin, fully relaxed InAs membranes of different thicknesses ($T_{InAs} = 5$ nm, 8 nm, and 13 nm) were transferred onto Si/SiO_2 substrates using an epitaxial layer transfer (ELT) technique reported previously.[5,9–11] Here, a thick SiO_2 layer (thickness, 1.2 μm) was used as the back-side insulator (i.e., body oxide) to reduce the parasitic capacitance of the Si substrate. Ni (thickness, ~40 nm) source (S) and drain (D) electrodes were fabricated using electron-beam lithography and annealed at 300 °C for 1 min in a N_2 ambient.[12] A 10 nm-thick ZrO_2 gate dielectric was subsequently deposited by atomic layer deposition at 130 °C, followed by a forming gas anneal at 170 °C for 30 min in order to improve the ZrO_2/InAs interface quality. Subsequently, Ni (thickness, ~40 nm) top-gate (G) electrodes, overlapping the S/D, were fabricated. A cross-sectional schematic and a top-view scanning electron microscopy (SEM) image of a top-gated InAs XOI FET are shown in Figs. 1(a) and 1(b), respectively. Here, the InAs channel is patterned into a nano-ribbon (NR) with a width of ~350 nm, the top-gate electrode overlaps the S/D electrodes, and the channel length (i.e., S/D spacing) is $L_G \sim 200$ nm. The cross-sectional transmission electron microscopy (TEM) image of the device is shown in Fig. 1(c), depicting an abrupt interface between the single-crystalline InAs ($T_{InAs} = 5$ nm) and the Si/SiO_2 substrate.

Transfer characteristics of InAs XOI n-FETs with $T_{InAs} = 5$ nm, 8 nm, and 13 nm are shown in Figs. 2(a)–2(c), respectively. A clear improvement in the subthreshold swing (SS) and OFF-state current (I_{OFF}) with body thickness miniaturization is evident. Specifically, the SS at $V_{DS} = 0.5$ V is monotonically improved from ~180 mV/dec for $T_{InAs} = 13$ nm FETs to ~115 mV/dec for $T_{InAs} = 5$ nm devices. Similarly, I_{OFF}, as defined by the minimum current value at $V_{DS} = 0.5$ V, is drastically decreased from ~ 1500 nA/μm for $T_{InAs} = 13$ nm to ~4 nA/μm for $T_{InAs} = 5$ nm. The reduction of SS with thickness scaling could be explained by the enhanced gate coupling efficiency, while the decreased I_{OFF} is attributed to the increased band gap due to quantum confinement. For instance, the calculated energy band gaps of InAs XOI from the k.p method are E_g ~0.54, 0.45, and 0.4 eV for $T_{InAs} = 5$, 8, and 13 nm, respectively.

The measured temperature dependency of I_{OFF} for the 8 nm XOI FET at a low field of $V_{DS} = 0.05$ V is shown in Fig. 2(d). An activation energy of $E_A = d(\ln I_{OFF})/d(1/kT)$

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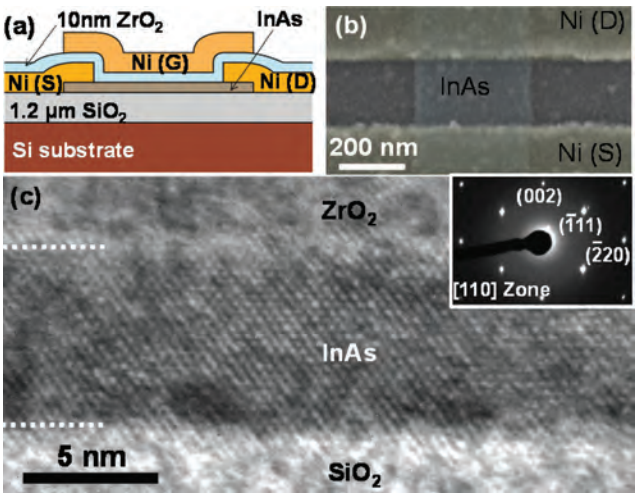

FIG. 1. (Color online) (a) Cross-sectional schematic of the top-gated InAs XOI FETs explored in this study. (b) SEM image of a fabricated device. (c) Cross-sectional TEM image of ~7 nm thick InAs membrane on a Si/SiO_2 substrate with a ZrO_2 gate dielectric. Inset shows the diffraction pattern corresponding to the InAs crystal.

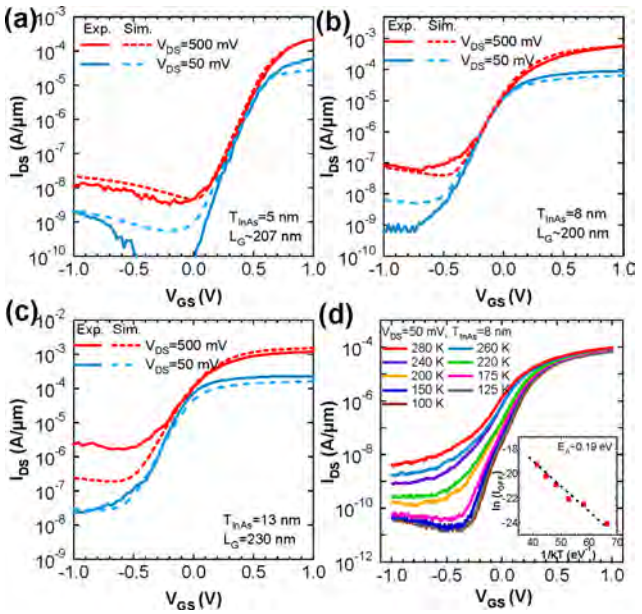

FIG. 2. (Color online) Experimental (solid lines) and simulated (dashed lines) transfer characteristics of InAs XOI FETs with (a) 5 nm, (b) 8 nm, and (c) 13 nm body thickness. (d) Temperature dependent measurements of an 8 nm thick InAs XOI FET at $V_{DS} = 50$ mV. Inset shows the Arrhenius plot of $\ln(I_{OFF})$ vs $1/kT$.

~0.19 eV was extracted, where k is the Boltzmann constant and T is the temperature. This activation energy is close to half of the band gap of 8 nm InAs ($E_g \sim 0.45$ eV), suggesting that the OFF current at low V_{DS} is dominated by mechanisms directly dependent on intrinsic carrier concentration, such as a combination of Shockley Read Hall (SRH) generation/recombination and trap assisted tunneling (TAT). At a high field of $V_{DS} = 500$ mV (data are not shown), an activation energy of $E_A \sim 0.15$ eV is extracted which is only slightly lower than that of the low-field measurements. This suggests band-to-band tunneling (BTBT) plays only a minor role as compared to SRH and TAT.

In order to better understand the effect of body thickness on the device characteristics, particularly the OFF current floor, 2D simulations coupling the Poisson's and drift-diffusion relations were conducted with TCAD Sentaurus 2010. The experimental OFF-state characteristics were fit by adjusting the low field minority carrier lifetime and including SRH, TAT, and BTBT models. The materials parameters, such as effective mass, band gap, and electron affinity values were obtained from k.p calculations for each T_{InAs}, and thickness dependent phonon mobilities previously calculated[5] were used. A body doping concentration of $N_D = 4 \times 10^{16} cm^{-3}$ was assumed. An interface trap density of $D_{it} = 3 \times 10^{12}$ states/cm^2eV uniformly distributed through the bandgap was used for all body thicknesses in order to fit the experimental SS. A nonlocal BTBT model was used, with A and B parameters extracted from our previous paper on InAs XOI tunnel-FETs[13] and scaled with tunneling mass and band gap. The Hurkx TAT model was used to simulate the subthreshold region as suggested by the temperature dependent measurements. In this model, TAT is accounted for by increasing the SRH recombination/generation rate in regions of high electric fields. A low-field minority carrier lifetime of $\tau = 1$ ps was used as a fitting parameter to match I_{OFF}. This lifetime is reasonable given that $\tau = 50$ ps has been reported for thicker ($T_{InAs} = 90$ nm) InAs epilayers,[14] with τ reducing as the thickness is decreased. The saturation velocity was used only as a fitting parameter to match the ON-state characteristics. A good fit with the experiments are obtained with the simple simulation used here (Figs. 2(a)–2(c)), once again suggesting that I_{OFF} is dominated by TAT and SRH with BTBT only making a minor contribution at high-fields. In the future, the simulations could be improved by a more rigorous treatment of all quantum effects.

Next, we focus on the ON-state characteristics of the XOI FETs. Figure 3(a) shows the transconductance, g_m as a function of the gate bias (V_{GS}) for different body thicknesses at $V_{DS} = 0.5$ V. Clearly, the peak g_m decreases as the body thickness is reduced with peak $g_m \sim 1.72$ and 0.65 mS/μm for $T_{InAs} = 13$ and 5 nm, respectively (Fig. 3(b)). The intrinsic transconductance, $g_{mi} = g_m/(1 - g_m R_S - g_d R_{SD})$ was also extracted by subtracting the contact resistance effects, where R_S is the source contact resistance, R_{SD} is the series resistance of S/D contacts (i.e., $R_{SD} = R_S + R_D = 2R_S$), and $g_d = dI_{DS}/dV_{DS}$ is the drain conductance. Here, $R_s = 85\ \Omega\ \mu$m, 230 $\Omega\ \mu$m, and 600 $\Omega\ \mu$m were used for $T_{InAs} = 13$, 8, and 5 nm, respectively, as measured from the transmission line method. Peak g_{mi} shows an improvement of ~1.4–2.5 × over peak g_m for the explored thickness range, with the thinner body devices

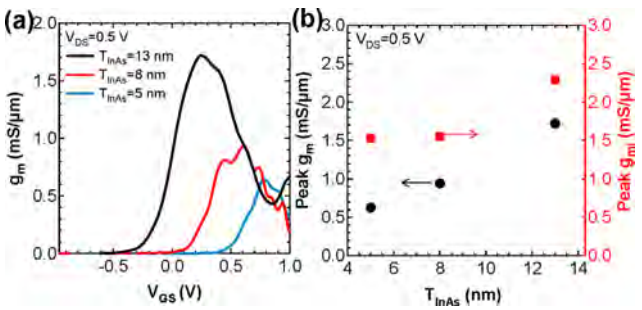

FIG. 3. (Color online) (a) Transconductance as a function of V_{GS} for different body thicknesses. (b) Peak g_m and g_{mi} as a function of thickness.

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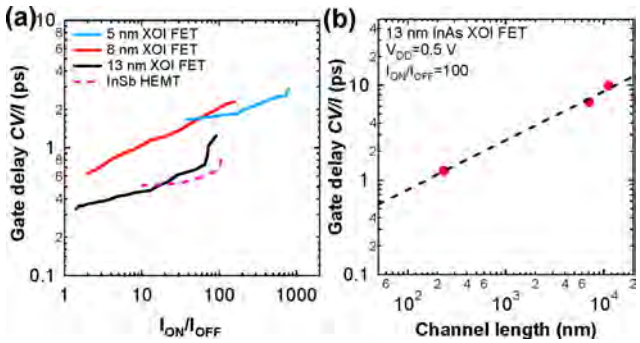

FIG. 4. (Color online) (a) Gate delay ($C_{ox}V_{DD}/I_{ON}$) as a function of I_{ON}/I_{OFF} for XOI FETs ($V_{DD}=0.5$ V) and InSb HEMT ($L_G=200$ nm, $V_{DD}=0.5$ V).[17] (b) Gate delay of 13 nm thick InAs XOI FETs at $V_{DD}=0.5$ V and $I_{ON}/I_{OFF}=100$ as a function of channel length.

showing a more dramatic enhancement, attributed to the higher contact resistance. Specifically, peak g_{mi} of ~2.3 and 1.5 mS/μm are observed for $T_{InAs}=13$ and 5 nm, respectively (Fig. 3(b)). The body thickness dependence of g_{mi} can be attributed to the previously reported mobility degradation for thin body InAs XOI FETs.[5] The reported g_{mi} values are among the highest reported values in literature for III-V FETs, despite $L_G \sim 200$ nm used in this work, and demonstrate the promise of the XOI technology for high performance FETs.

In order to assess the performance of InAs XOI FETs, gate delay[15,16] was estimated from $C_{ox}V_{DD}/I_{DS}$ at $V_{DD}=\Delta V_{GS}=V_{DS}=0.5$ V with an intrinsic gate oxide capacitance of $C_{ox} \sim 1.4$ μF/cm^2 (dielectric constant of ZrO_2 is ~16) and plotted as a function of I_{ON}/I_{OFF} in Fig. 4(a). The C_{ox} used here is extracted from the parallel plate capacitance of ZrO_2 without considering the quantum capacitance (C_Q) of InAs membranes. While this is acceptable for present thicknesses, heavily scaled devices should use the series combination of C_{ox} and C_Q for this metric. As a comparison, the gate delays for a InSb[17] high electron mobility transistor (HEMT) with the same channel length ($L_G=200$ nm) and $V_{DD}=0.5$ V from literature is also shown. InAs XOI FETs with $T_{InAs}=13$ nm show a gate delay of ~0.4 to 1 ps at I_{ON}/I_{OFF} ratio of ~10 to 100. These values are comparable to the buried channel 20 nm-thick InSb HEMTs on III-V substrates. As expected, the thinner body XOI FETs exhibit a higher gate delay due to the lower g_m (and thereby, lower I_{ON}), but they deliver higher I_{ON}/I_{OFF}. The results show the interplay between I_{ON}/I_{OFF} and gate delay and suggest that the optimal body thickness need to be wisely selected for a given application. To predict the performance limits of 13 nm InAs XOI FETs, the experimentally extracted gate delays at $I_{ON}/I_{OFF}=100$ and $V_{DD}=0.5$ V are plotted for different channel lengths as shown in Fig. 4(b). Based on this plot, the gate delay is projected to be ~0.5 ps when the device is scaled down to 50 nm. This projected gate delay is comparable to the state-of-the-art carbon nanotube *p*-FETs, which are known for their ultrahigh carrier mobility, for the same L_G, V_{DD}, and I_{ON}/I_{OFF} (Refs. 15 and 18).

The results here are particularly promising given that the ultrathin XOI FETs are surface devices with the channel in intimate contact with the gate stack. This device configuration is highly attractive for future scaled transistors as they are expected to exhibit better short channel effects as compared to HEMTs and other buried channel devices. In the future, more in-depth theoretical models that incorporate improved tunneling treatments are needed to further guide the experimental efforts. In parallel, scaling of the channel lengths of the experimental devices down to the sub-50 nm regime is needed, along with exploring sub-5 nm thick body thicknesses.

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