Tunnel Field Effect Transistor With Raised Germanium Source

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***Abstract*—The performance of a tunnel field effect transistor (TFET) with a raised germanium (Ge) source region is investigated via 2-D device simulation with a tunneling model calibrated to experimental data. The comparison of various Ge-source TFET designs shows that a fully elevated Ge-source design provides for the steepest subthreshold swing and, therefore, the largest ON-state drive current for low-voltage operation. Mixed-mode (dc and ac) simulations are used to assess the energy-delay performance. In comparison with a MOSFET, an optimized Ge-source TFET is projected to provide for a lower energy per operation for throughput in the frequency range of up to ∼1 GHz for sub-0.5-V operation.**

***Index Terms*—Band-to-band tunneling (BTBT), germanium (Ge) source, raised source, tunnel field effect transistor (TFET).**

I. Introduction

TUNNEL field-effect transistors (TFETs) are of interest as an alternative transistor design for very low voltage operation. Based on carrier injection via band-to-band tunneling (BTBT), TFETs can achieve subthreshold swing (S) less than 60 mV/dec at room temperature, which allows for a more aggressive reduction of the threshold voltage (V_T) and, hence, the supply voltage (V_{DD}) for a given performance target [1]. Recent experimental demonstrations of Si TFETs [2] and Ge-source TFETs [3] have shown sub-60-mV/dec switching behavior. The Ge-source design achieves much higher ON-state drive current (I_{ON}) because of the smaller band gap of the Ge versus Si.

The conventional TFET is designed for lateral (parallel to the semiconductor/gate-dielectric interface) tunneling in which the BTBT occurs across the source-channel junction [4]. Although it can achieve a steep subthreshold swing, this design has fundamental limitations. Since the carrier injection occurs over a very small area, I_{ON} is inherently small. Moreover, the drain bias can modulate the tunnel barrier width, resulting in a nonlinear output characteristic [5].

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The planar Ge-source TFET presented in [3] is designed for vertical (perpendicular to the semiconductor/gate-dielectric interface) tunneling in which the BTBT occurs within the source region. At small gate biases, however, the lateral tunneling occurs first, resulting in a small "kink" in the transfer characteristic which effectively degrades the S [3]. This paper presents an improved Ge-source TFET design in which this lateral tunneling is suppressed to achieve steeper switching behavior and higher I_{ON} for low-voltage $(V_{DD} < 0.5\ V)$ operation. The performance of this new TFET design is compared against that of other Ge-source TFET designs via 2-D device simulation. For a 30-nm gate length (L_G), an optimized Ge-source TFET is projected to provide for reduced energy per operation, as compared to a MOSFET, for throughput in the frequency range of up to ∼1 GHz for sub-0.5-V operation.

II. Device Structures and Simulation

Fig. 1(a) shows the planar Ge-source TFET design reported in [3], which is fabricated by recessing the Si in the source region before selectively growing 15 nm of *in situ*-doped p-type Ge. Fig. 1(b) shows the partially elevated Ge-source design, which can be fabricated by recessing the Si in the source region and then overgrowing the *in situ*-doped Ge (by 10 nm) for a total Ge thickness (T_{Ge}) of 25 nm. Fig. 1(c) shows the fully elevated Ge-source design, which can be fabricated by selectively growing a thin Si vertical offset layer before growing the *in situ*-doped Ge in the source region.

For each of the TFET designs, the Ge source is heavily doped p-type $(N_{Ge} = 10^{19}\ cm^{-3})$, and the Si drain is heavily doped n-type $(10^{19}\ cm^{-3})$. The Si channel region is moderately doped p-type $(10^{18}\ cm^{-3})$ and is 100-nm thick to minimize the OFF-state leakage current [6]. The underlying buried oxide (SiO_2) layer is 200-nm thick. L_G is 30 nm, and the gate dielectric equivalent SiO_2 thickness (EOT) is 1 nm. The gate material is metallic, with a work function of 4.0 eV. For the planar source design, the gate-sidewall spacers (L_{SP}) comprise silicon nitride and are 8-nm wide; for the elevated source designs, they comprise silicon dioxide and are 1-nm wide. For the planar and partially elevated source designs, the gate-to-source overlap (L_{OV}) is 5 nm. For the fully elevated source design, the Si vertical offset layer (T_{OFFSET}) is 5-nm thick and doped p-type $(10^{18}\ cm^{-3})$. A fixed charge $(\sim 10^{11}\ q/cm^2)$ at each dielectric/Ge interface is assumed [7].

The device simulations were performed with Sentaurus Device [8] using a nonlocal BTBT model that dynamically

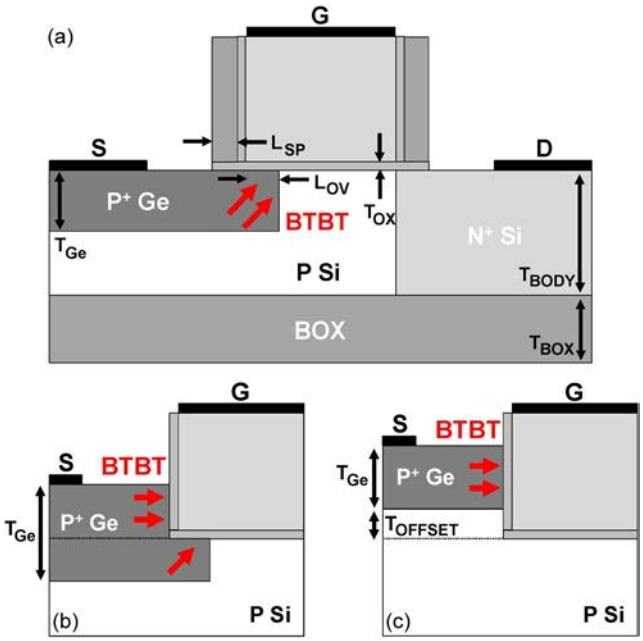

Fig. 1. Schematic cross section of the (a) planar, (b) partially elevated, and (c) fully elevated Ge-source TFETs, with (b) and (c) only showing the schematics near the source region. Dominant directions of electron tunneling are indicated by the arrows.

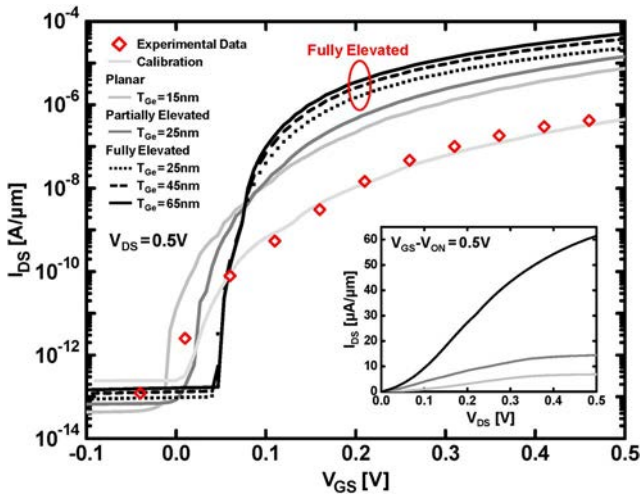

Fig. 2. Simulated transfer characteristics for planar, partially elevated, and fully elevated Ge-source TFETs. Experimental data from [3] and the corresponding simulated curve using the calibrated model are shown for reference. Inset: simulated output characteristics for planar ($T_{Ge} = 15$ nm), partially elevated ($T_{Ge} = 25$ nm), and fully elevated ($T_{Ge} = 65$ nm) Ge-source TFETs. V_{ON} is defined as the gate voltage at the onset of BTBT, which is extracted by determining the gate voltage at which the transconductance increases by more than an order of magnitude.

determines the tunneling paths according to the gradient of the energy band and is applicable to arbitrary tunneling barriers with a nonuniform electric field and abrupt or graded heterojunctions. The Fermi statistics is assumed, and the drift-diffusion carrier transport and Shockley-Read-Hall recombination models were used. The tunneling model was first calibrated to experimental data [3] for a (nonoptimized) planar Ge-source TFET, as shown in Fig. 2. Since the BTBT occurs primarily within the Ge-source region, the modification of the parameters for the Si was found to have little effect on the device performance. The fitted A and B coefficients ($A = 1.46 \times 10^{17}$ cm$^{-3} \cdot$ s^{-1} and $B = 3.59 \times 10^{6}$ V $\cdot$ cm^{-1}) of the tunneling model were then used to simulate the dc and ac characteristics for the various Ge-source TFET designs.

III. DC Characteristics

The dominant tunneling mode (lateral versus vertical) within a TFET is strongly dependent on its geometry. At high gate voltages, the vertical tunneling is dominant as indicated by the arrows in Fig. 1 if the source is nondegenerately doped and adequately thick ($N_{Ge} = 10^{19}$ cm^{-3} and $T_{Ge} = 15$ nm) and if there is significant gate-to-source overlap [4]. With a thin gate-sidewall dielectric, the vertical tunneling can be induced within the elevated Ge in the partially elevated and fully elevated source structures, resulting in increased I_{ON} (see Fig. 2). At low gate voltages, the lateral tunneling can occur from the lower corner of the Ge source to the Si channel if the drain voltage induces a significant potential drop across the channel-source junction. This is the case for the planar and partially elevated source structures; the device first turns on with the lateral tunneling and then transitions to the predominantly vertical tunneling so that the average S is degraded. For the fully elevated source structure, the lateral tunneling is suppressed because the potential drop across the source-channel junction is relatively small. This is because the drain voltage is dropped laterally within the Ge source rather than across the source-channel junction, thus electrostatically coupling with V_{GS} to maximize the BTBT within the source. A vertical offset ($T_{OFFSET} > 0$ nm) is necessary to achieve this effect.

IV. Energy-Delay Performance

It can be seen from Fig. 2 that the fully elevated Ge-source TFET design offers the highest I_{ON}/I_{OFF} ratio and that I_{ON} increases with Ge thickness. However, increasing T_{Ge} increases the total gate capacitance (C_{GG}) which compensates the effect of increasing I_{ON} with regard to the switching speed. (This tradeoff is favorable when the device drives a significant interconnect capacitance.) Fig. 3 shows the $C_{GG}-V_{GS}$ curves obtained from the ac simulations. In the OFF state, the total gate capacitance is dominated by the gate-to-(p^+) source capacitance (C_{GS}) due to the accumulation of holes at the gate dielectric interface in the source and channel regions. In the ON state, the total gate capacitance is dominated by the gate-to-(n^+) drain capacitance (C_{GD}) due to the inversion layer of the electrons at the gate dielectric interface in the channel region [9].

Using the dc and ac simulation results, the energy-delay performance of each TFET structure is evaluated using the methodology described in [1]. The fully elevated Ge-source design is projected to achieve the best delay because of its higher I_{ON} [see Fig. 4(a)], saturating for $T_{Ge} > 45$ nm. The best energy-versus-delay (1/frequency) performance is achieved with $T_{Ge} = 25$ nm [see Fig. 4(b)]. The curves for the 22-nm L_G MOSFET [10] are also shown in Fig. 4 for comparison. The TFET is not favorable for operation at high frequencies (> 1 GHz) because it cannot achieve very high I_{ON}. At lower frequencies, however, the fully elevated Ge-source

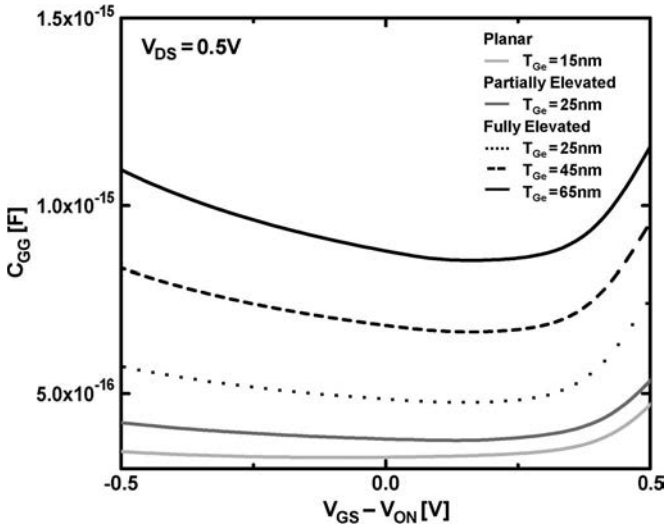

Fig. 3. Simulated gate capacitance versus gate voltage (C_{GG}–V_{GS}) characteristics for planar, partially elevated, and fully elevated Ge-source TFETs. C_{GG} is dominated by C_{GS} in the OFF state and by C_{GD} in the ON state. V_{ON} is defined as the gate voltage at the onset of BTBT.

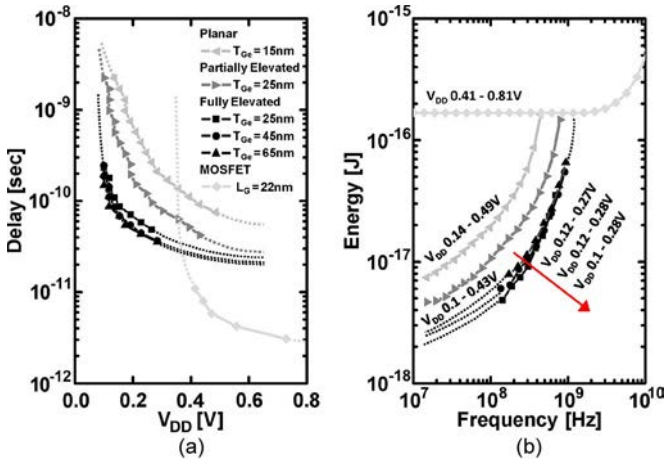

Fig. 4. Simulated (a) minimum-energy delay versus V_{DD} and (b) energy/cycle versus frequency of the TFETs versus MOSFET for a 30-stage FO1 inverter chain (activity factor = 0.01). Projections are indicated by the dotted lines.

TFET can achieve better energy efficiency than the MOSFET. This is because the TFET can operate at a substantially lower V_{DD} (corresponding to the subthreshold regime of operation of the MOSFET) with a steeper swing. A reasonable performance ($>$ 100 MHz) is projected for the fully elevated Ge-source TFET design, for V_{DD} down to 0.1 V. It should be noted that the fully elevated Ge-source TFETs can be scaled down to 10 nm in gate length without the OFF-state leakage degradation associated with conventional TFETs [11], due to the longer effective channel length provided by the Si vertical offset layer [see Fig. 1(c)].

V. Conclusion

A fully elevated Ge-source TFET design provides for an improved energy-delay performance, in comparison to planar or partially elevated Ge-source TFET designs. Based on 2-D device simulation using a tunneling model calibrated to experimental data, an optimized Ge-source TFET is projected to provide for energy efficiency superior to that of the MOSFET for operating voltages below 0.5 V. Thus, the fully elevated Ge-source TFET is a promising device for ultralow-power applications. It should be noted that complementary approaches, e.g., employing "pocket" doping for achieving a high I_{ON} in TFETs [12], [13], may allow the energy efficiency benefit of TFET technology to be extended to frequencies above 1 GHz. Moreover, the interconnect power savings due to low V_{DD} operation are not considered in this letter.

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