

Nonvolatile Hybrid CMOS-MRAM Circuits Using Three-Terminal Spin Orbit Torque Switches for Normally-Off Computing

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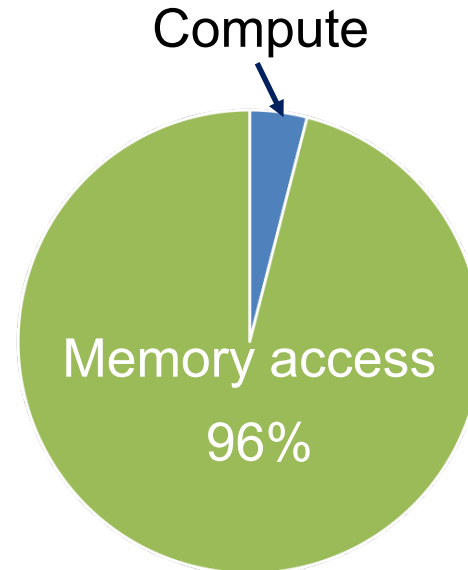
⁴Applied Materials



SRAM leakage and memory wall are motivation for normally-off computing

SRAM idle leakage
> 20% of total power¹⁻²

Memory wall for big data



Computing time for
genome sequencing³

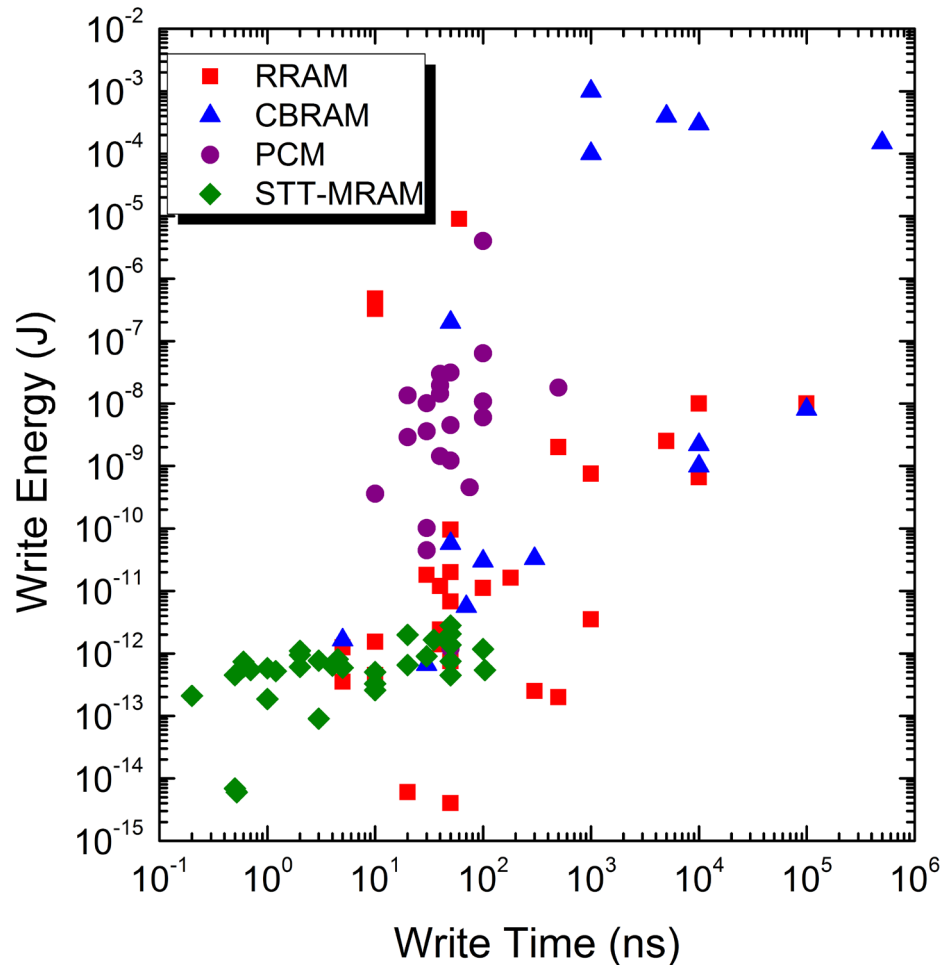
¹K. Zhang, et al. Solid-State Circuits, IEEE Journal of 40, 895-901 (2005).

²F. Tachibana, O. et al. IEEE Journal of Solid-State Circuits 49, 118-26 (2014).

³M.M.S. Aly, et al. IEEE Computer (2015)



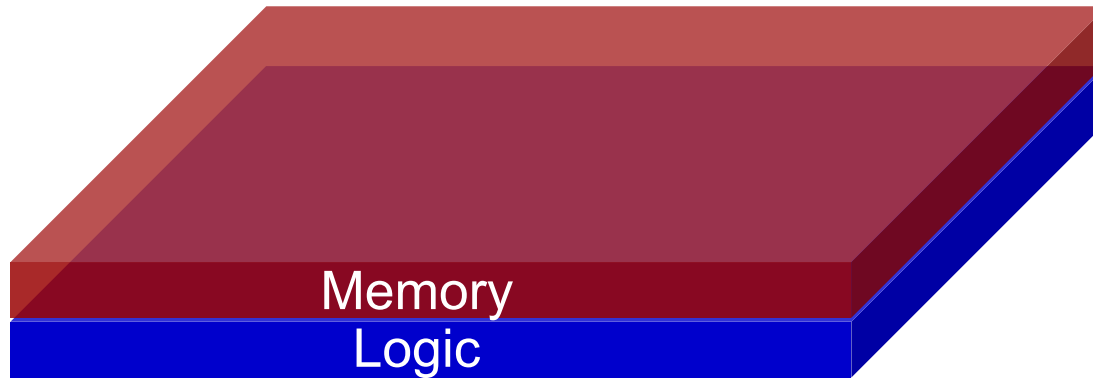
MRAM provides low voltage and high endurance nonvolatile memory



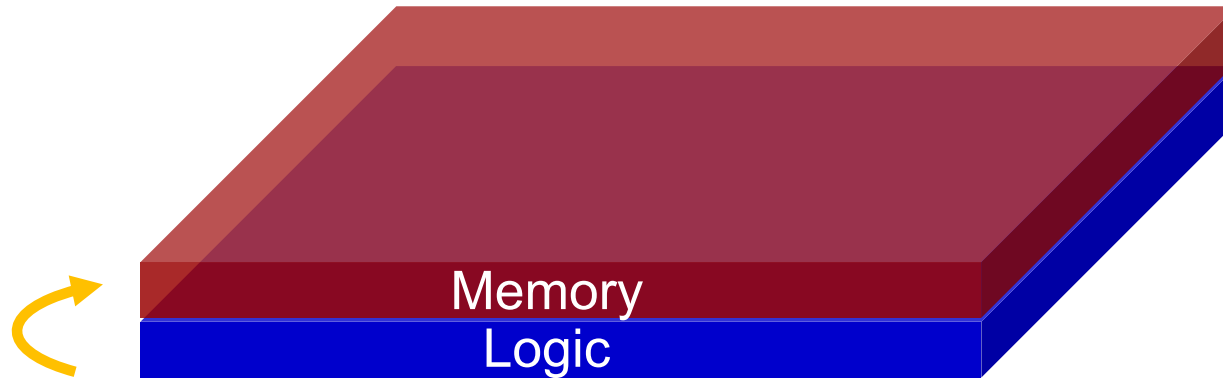
Endurance > 10^{15} cycles

H.-S. P. Wong, et al., "Stanford Memory Trends," <https://nano.stanford.edu/stanford-memory-trends>, 2016

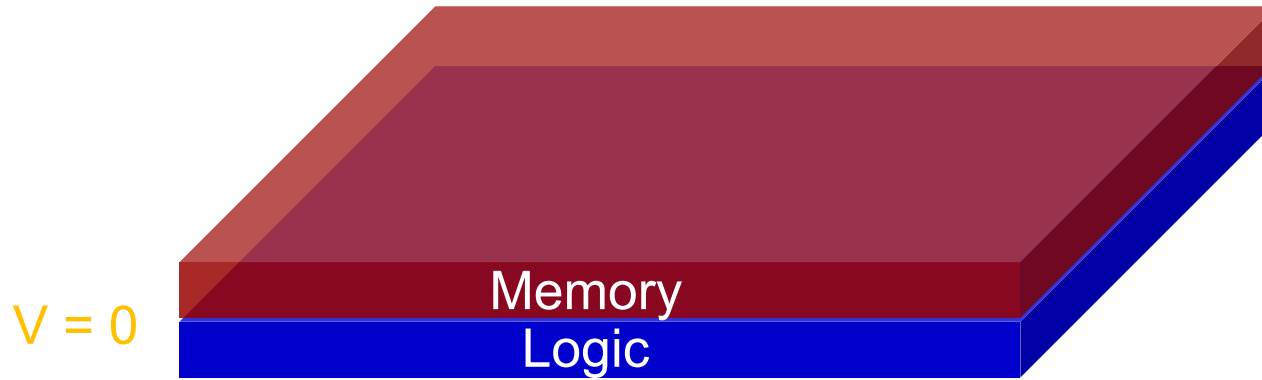
Goal: nonvolatile *circuits*



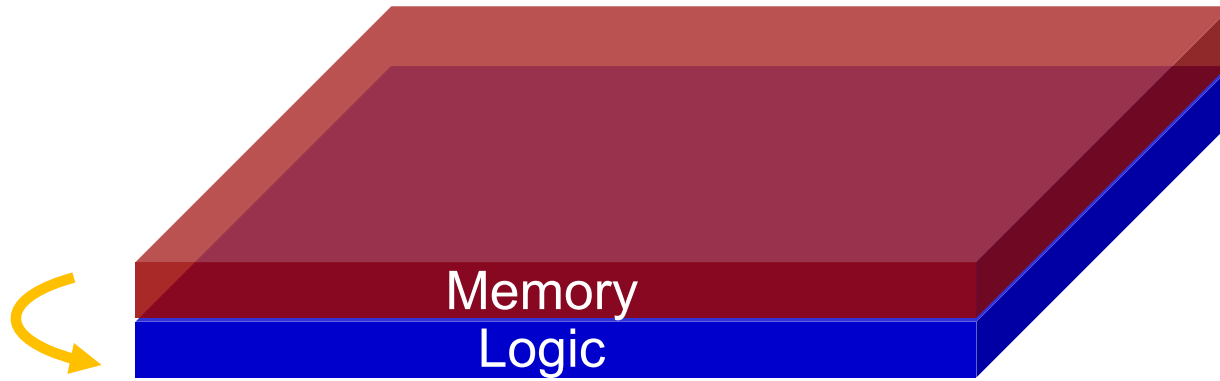
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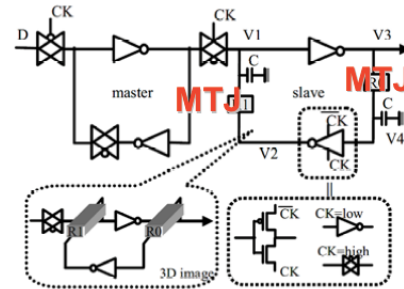
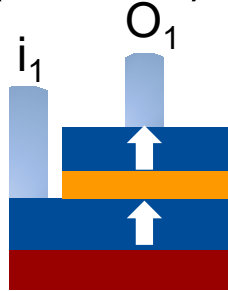


Prior art: 2-terminal MTJs

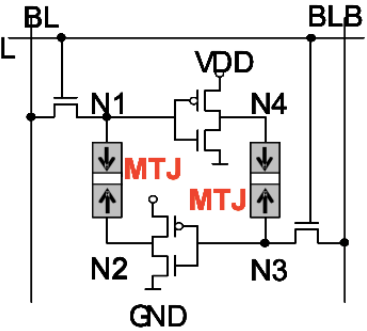
This work: 3-terminal or 4-terminal MTJs

H. Yoda et al. (Toshiba) IEDM 2012:

2-terminal
spin switch



Nonvolatile Flip flop
> 2GHz



Nonvolatile SRAM
> 2GHz

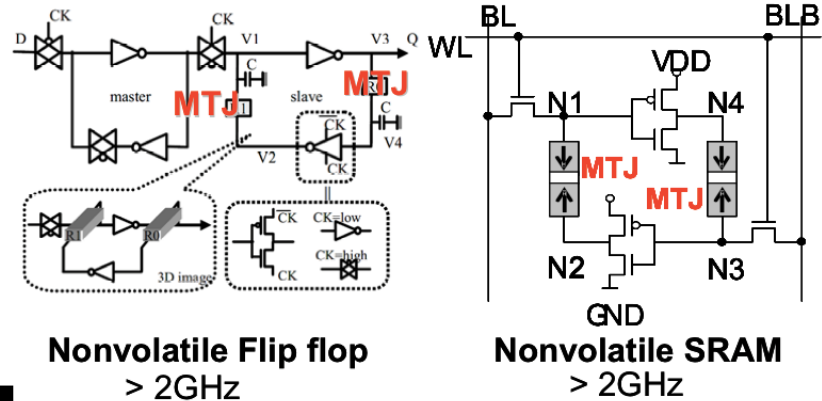
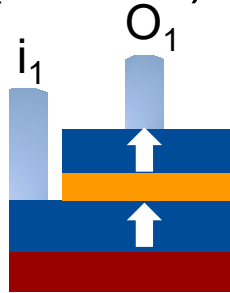


Prior art: 2-terminal MTJs

This work: 3-terminal or 4-terminal MTJs

H. Yoda et al. (Toshiba) IEDM 2012:

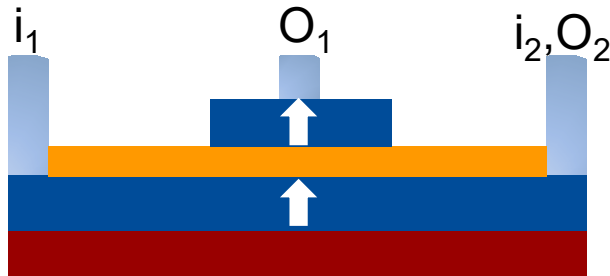
2-terminal spin switch



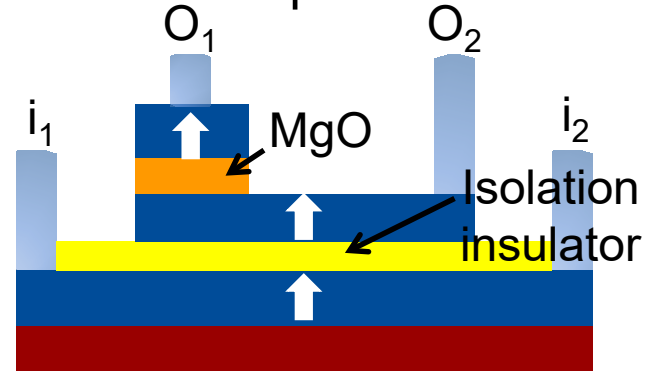
Nonvolatile Flip flop
> 2GHz

Nonvolatile SRAM
> 2GHz

3-terminal spin switch*



4-terminal spin switch**



- Separated read/write paths
- Avoids unnecessary current through the MTJs to enhance endurance
- Normal circuit operation is no longer dependent on MTJ variability

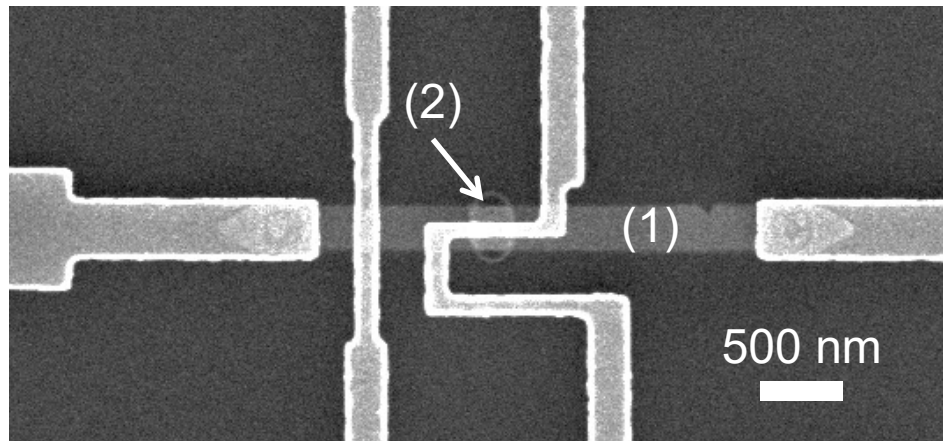
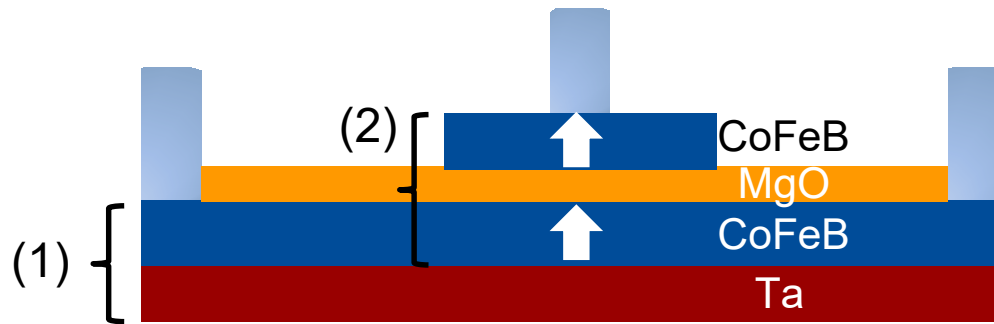
*Currivan-Incorvia et al. Nature Comm. 7, 10275 (2016)

**D.M. Bromberg et al. IEDM (2014)

3-terminal spin switches

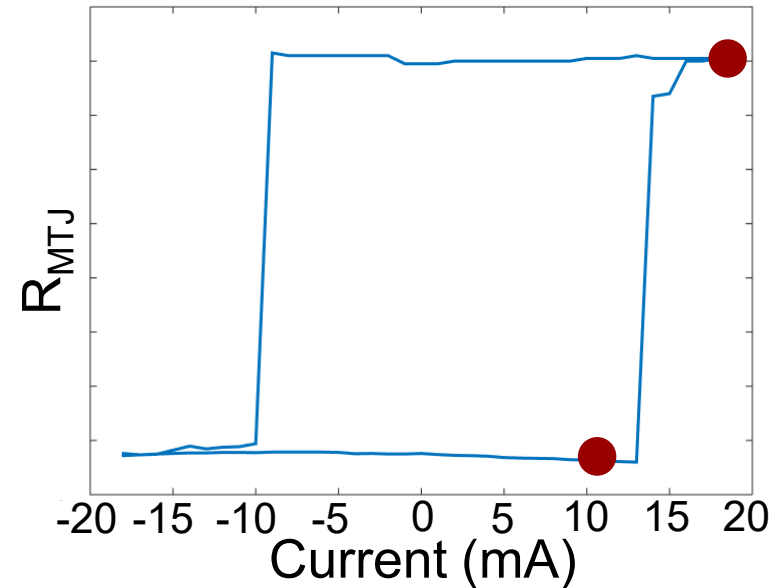
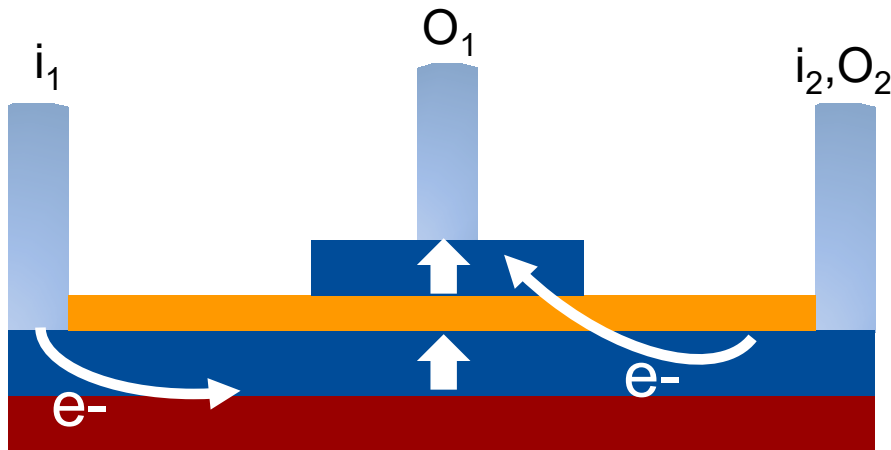
(1) Input magnetic wire

(2) Output magnetic tunnel junction (MTJ)



Device operation includes a write step and a read step

- To write: apply electrical current between i_1 and i_2
 - Magnetic wire switches via spin Hall effect (SHE)¹⁻²
- To read: apply current through MTJ between O_1 and O_2

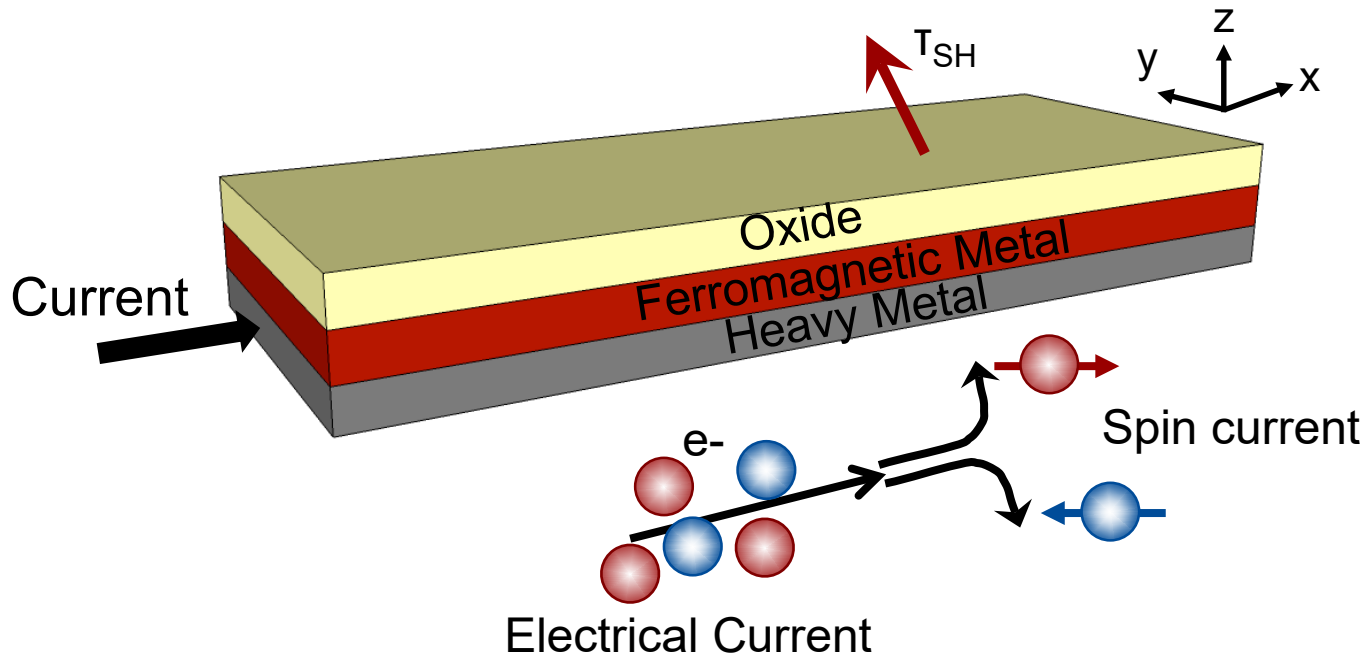


¹L. Liu et al. Science 336, 555-8 (2012)

²S. Emori et al. Nature Materials 12, 611 (2013)



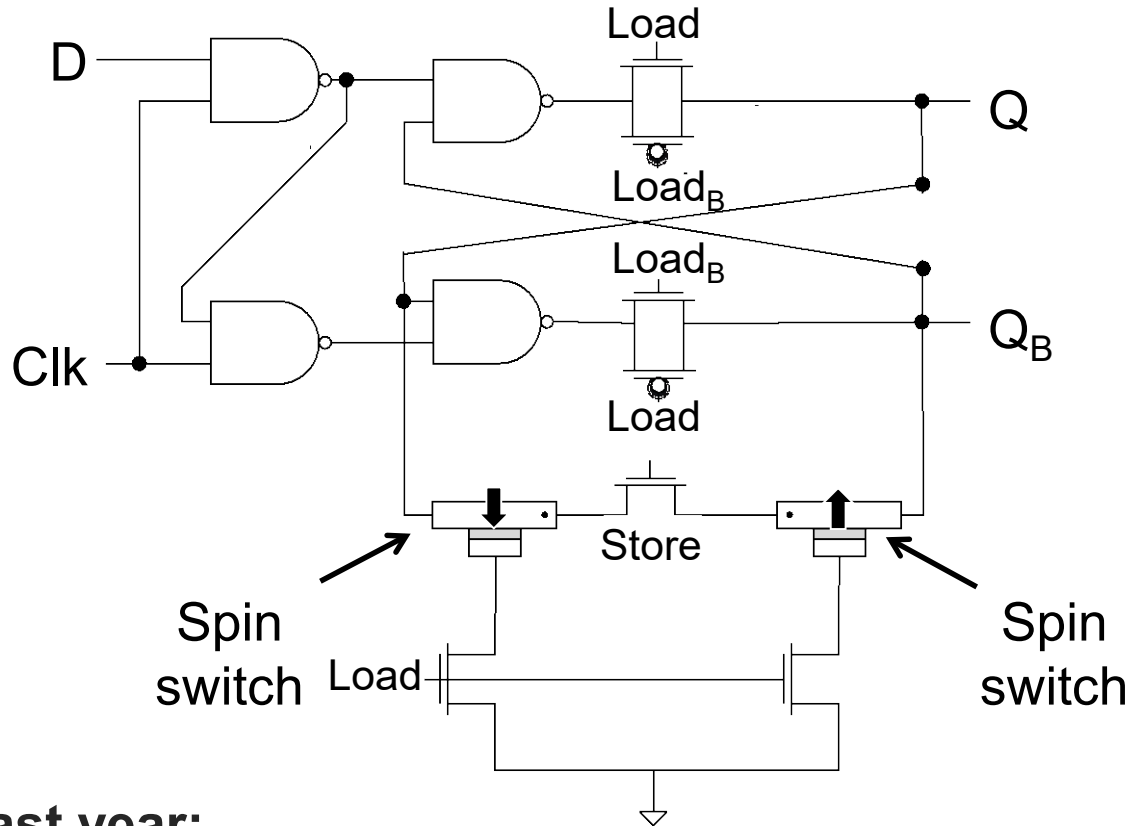
Magnetization switched by current via spin Hall effect



- Can utilize thicker heavy metal, keeping ferromagnet thin
- Domain wall-assisted switching
- $J_c \sim 0.1-1 \times 10^7$ A/cm² depending on edge pinning

Latch as demo of nonvolatile hybrid circuit

- CMOS circuit with 2 spin switches of opposite magnetization



- Last year:

- ❑ Designed circuit in SPICE
- ❑ Designed tapeout with 130 nm CMOS, $V_{dd} = 1.8$ V
- ❑ Grew and fabricated spin switch devices with 7% TMR

Improved spin switches

- Worked with Applied Materials to grow high-quality MTJ stack

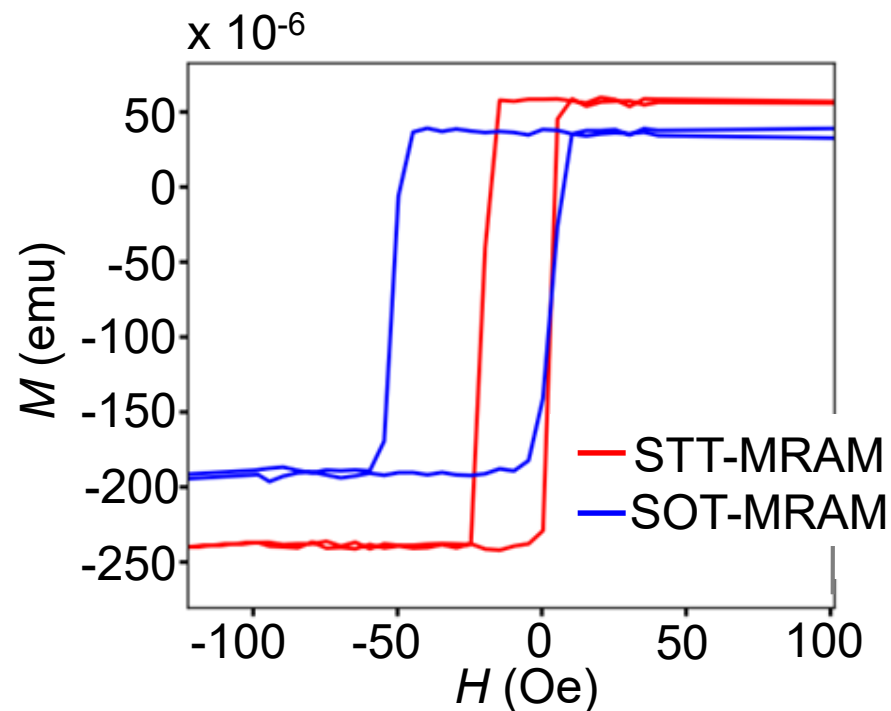
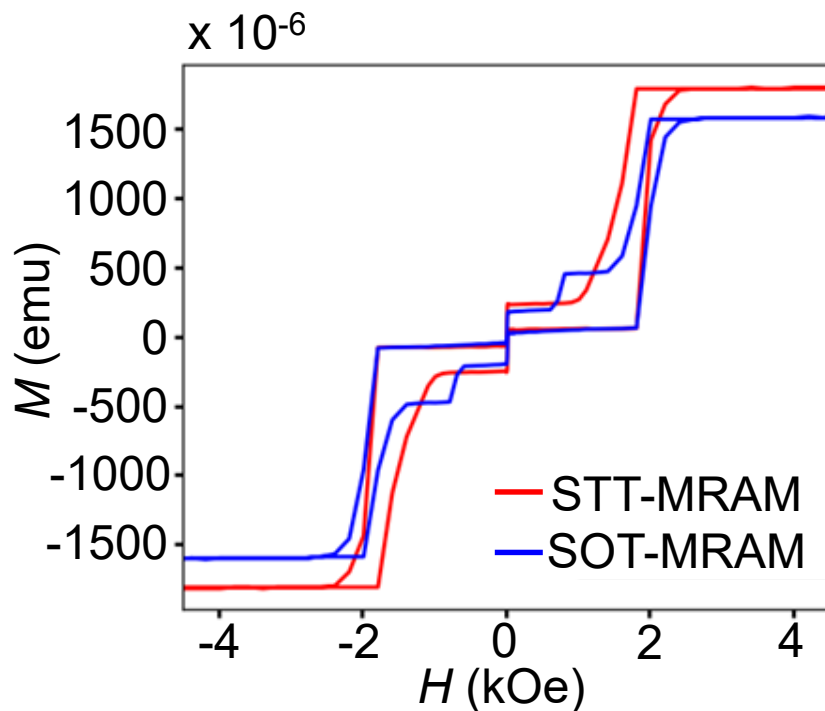
Layer	Thickness (Å)
Ru	30
Ta	10
[Co/Pt]	69
Ru	9
[Co/Pt]	50
CoFeB	19
MgO	RA 35
CoFeB	12
Ta	100
Thermal oxide	1k

- Requirements:
 - Perpendicular magnetic anisotropy
 - Free layer on bottom
 - Thick bottom Ta for spin Hall switching



Improved spin switches

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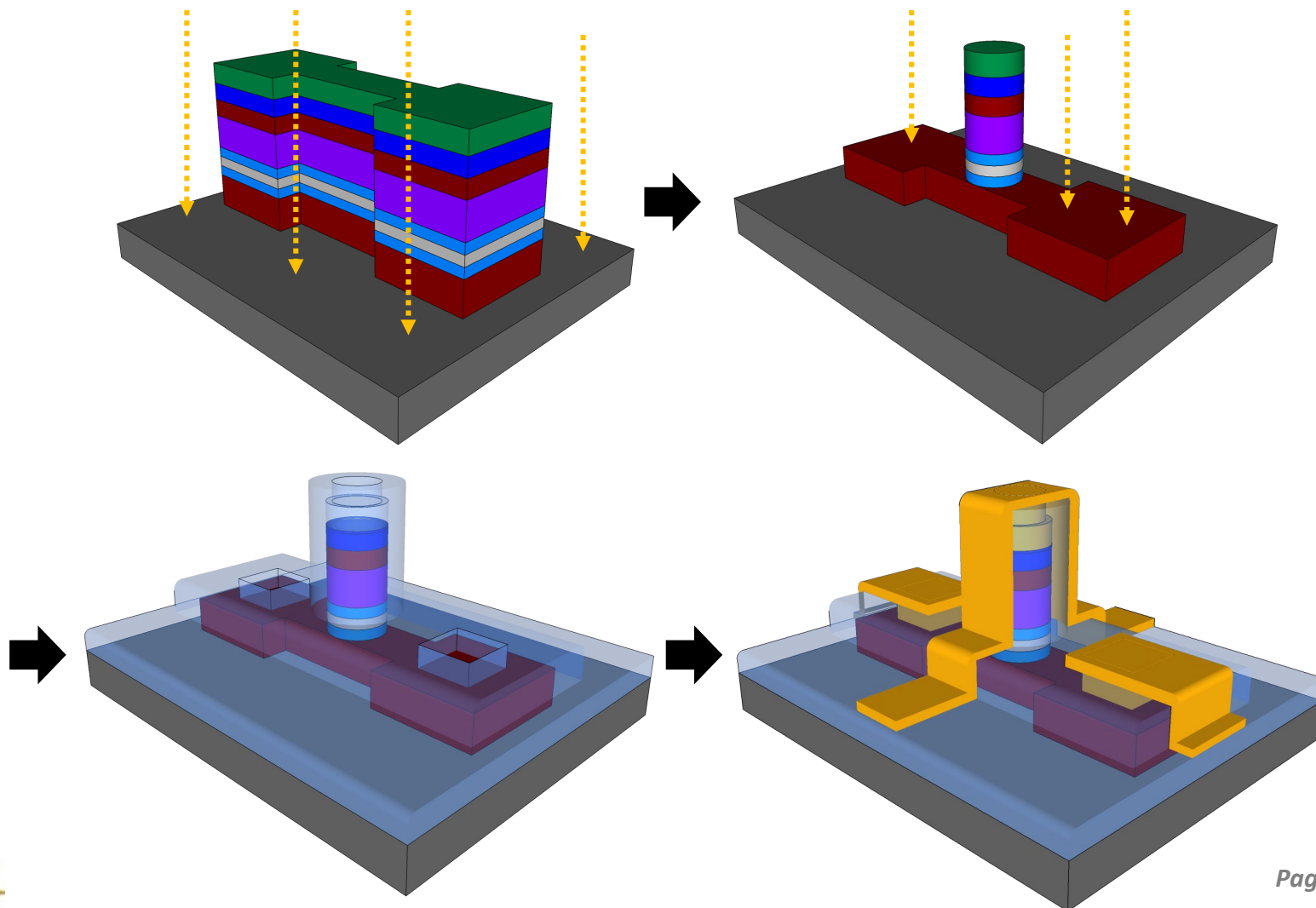


- Still have separation between free and fixed layers switching
- SOT stack has an extra fixed layer switch and a more asymmetric loop



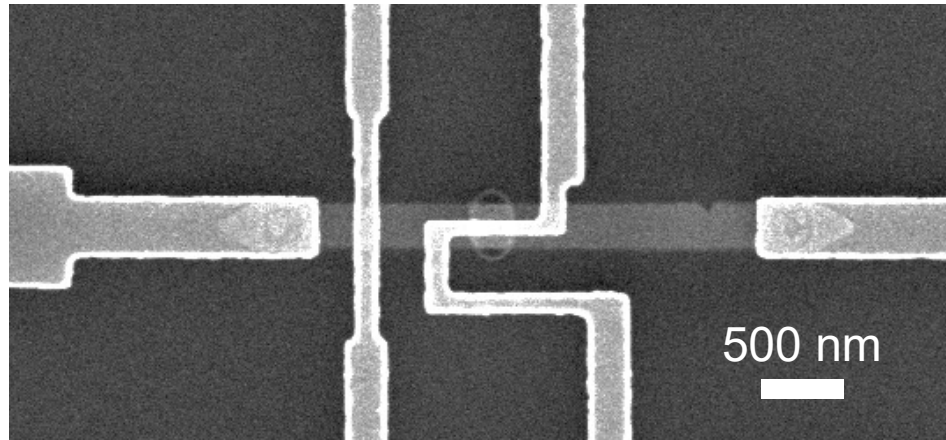
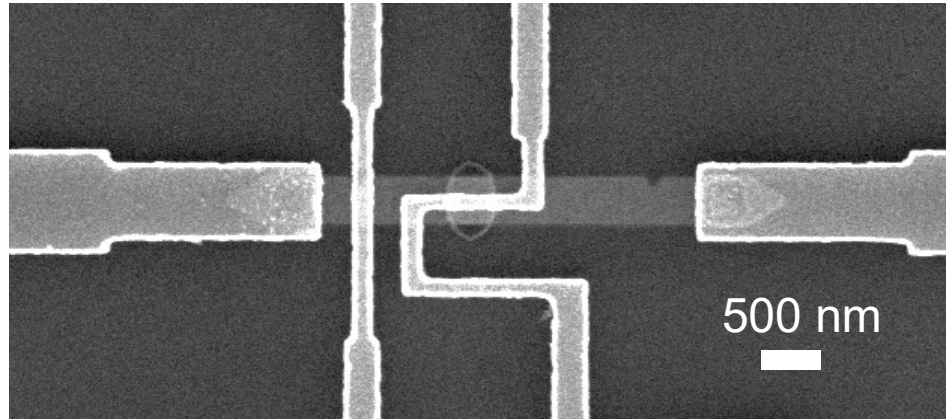
Device Fabrication

- *Pattern using e-beam lithography*
- *Etch using non-reactive ion milling*

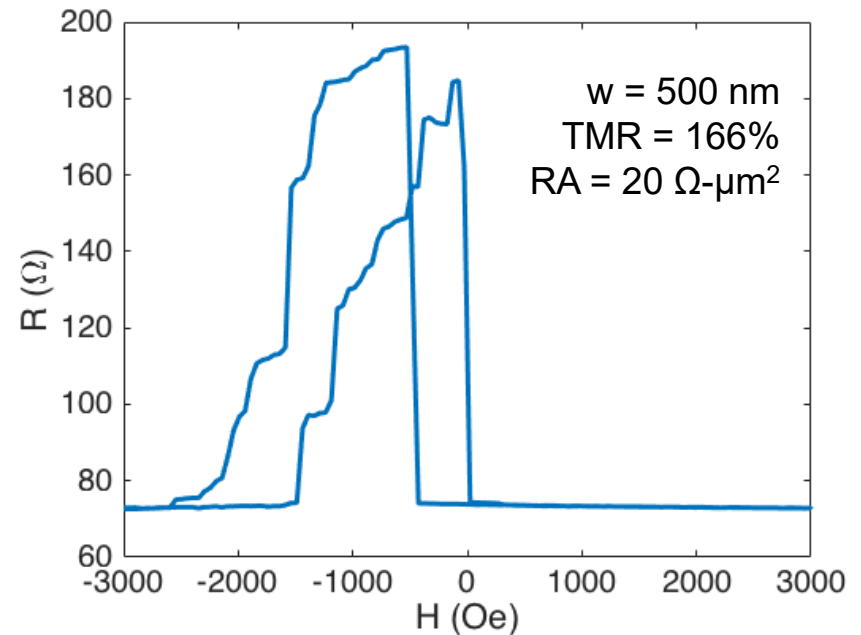
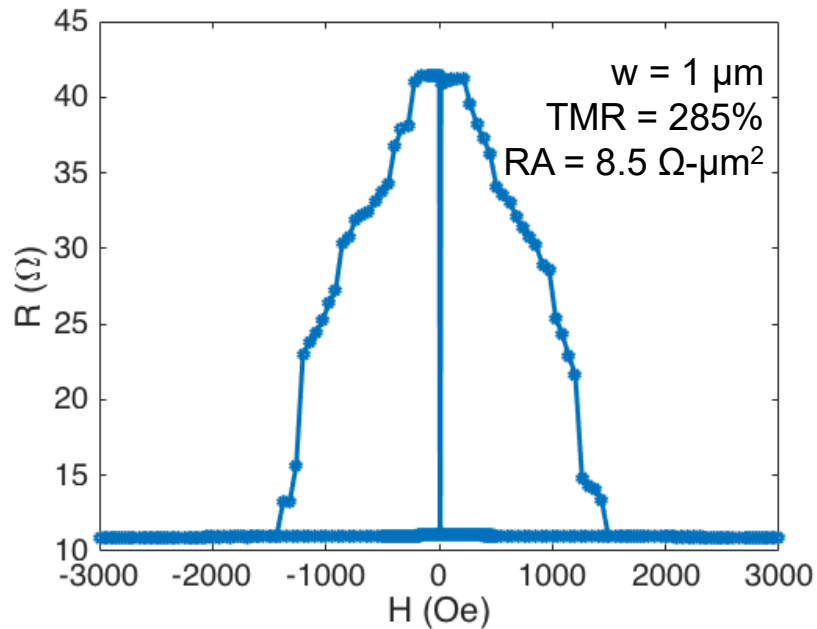


Device Fabrication

- 1 μm – 200 nm wide devices

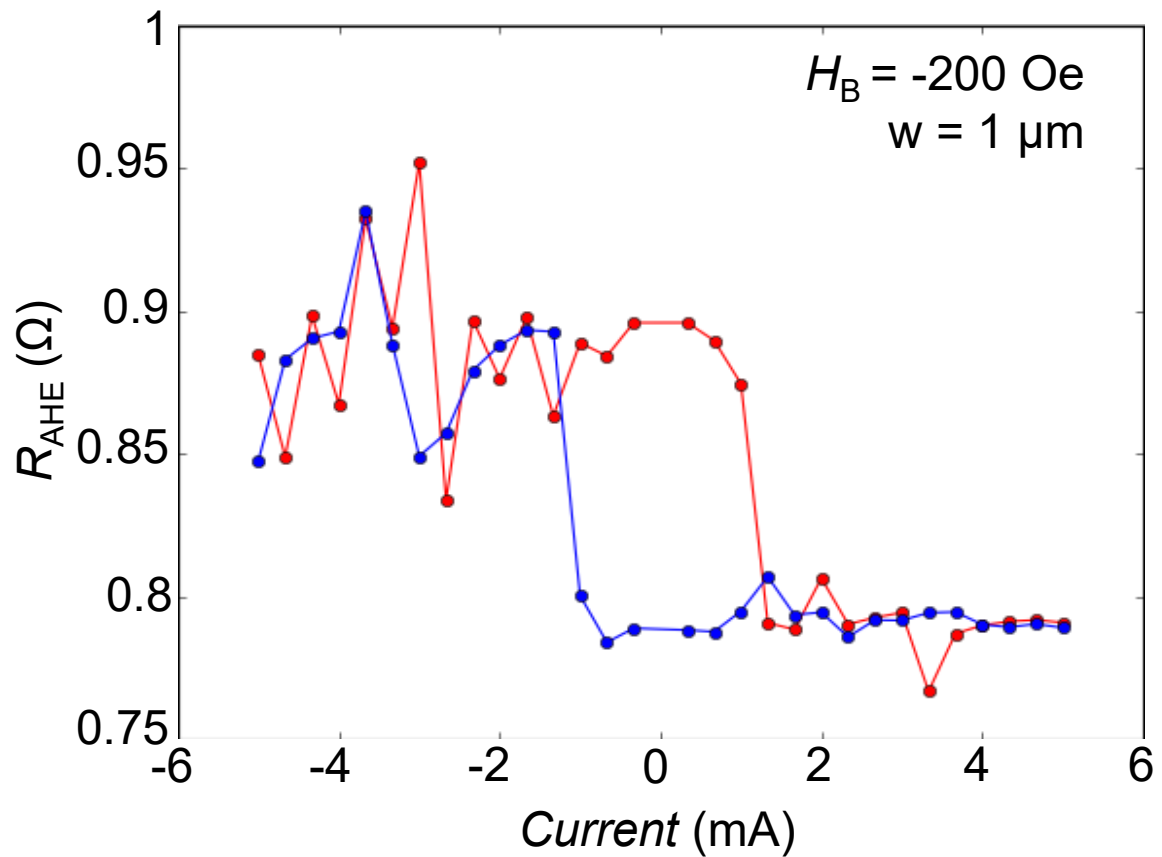


Field Testing



- **TMR 166% - 200%**
- **See scaling-induced effects on TMR and RA, but still have good switching separation**
- **Building setup with improved ESD control for testing smaller devices**

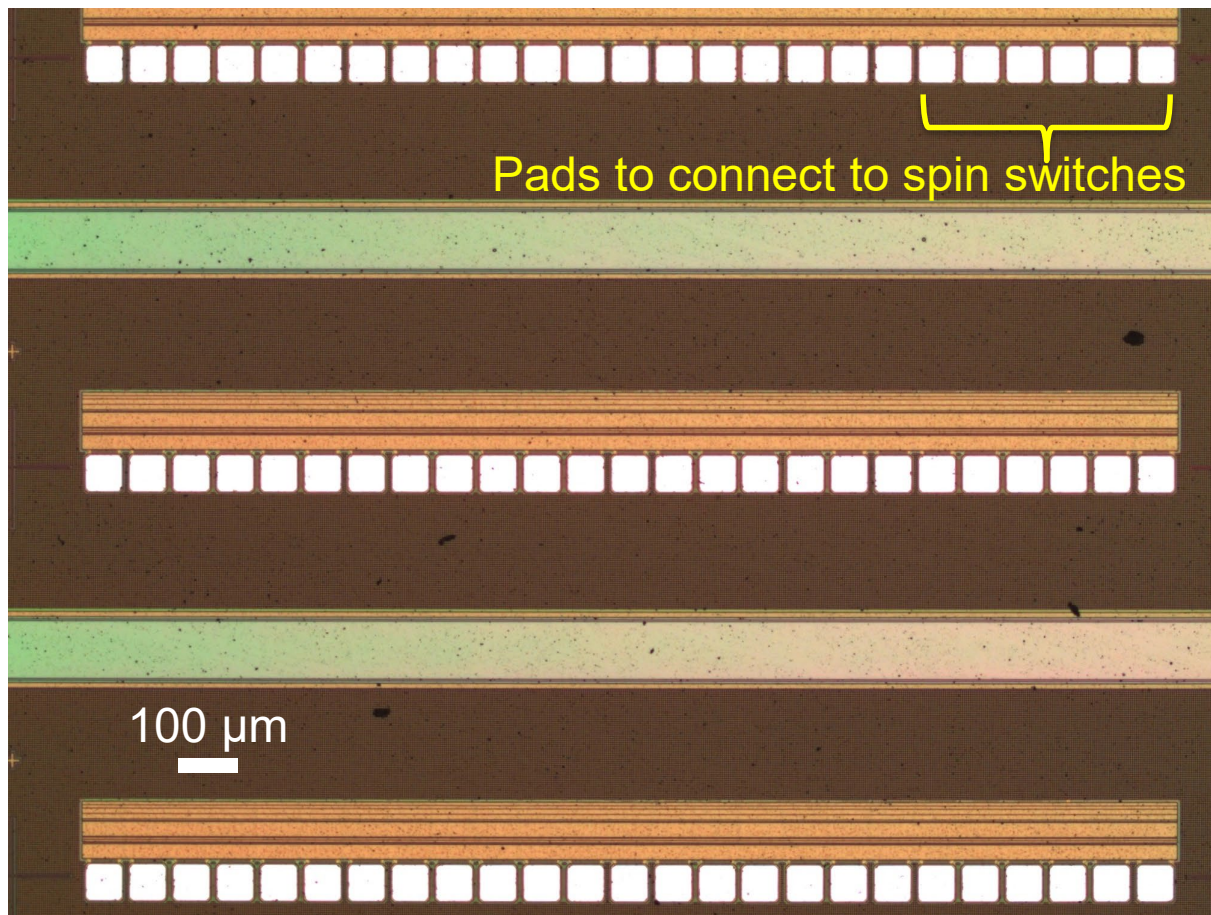
Current Testing



- Spin Hall switching with $J_c \sim 1.04 \times 10^7 \text{ A/cm}^2$
- Tapeout simulation shows we expect $I = 325 \mu\text{A}$
 - Requires $w_{\text{max}} = 280 \text{ nm}$



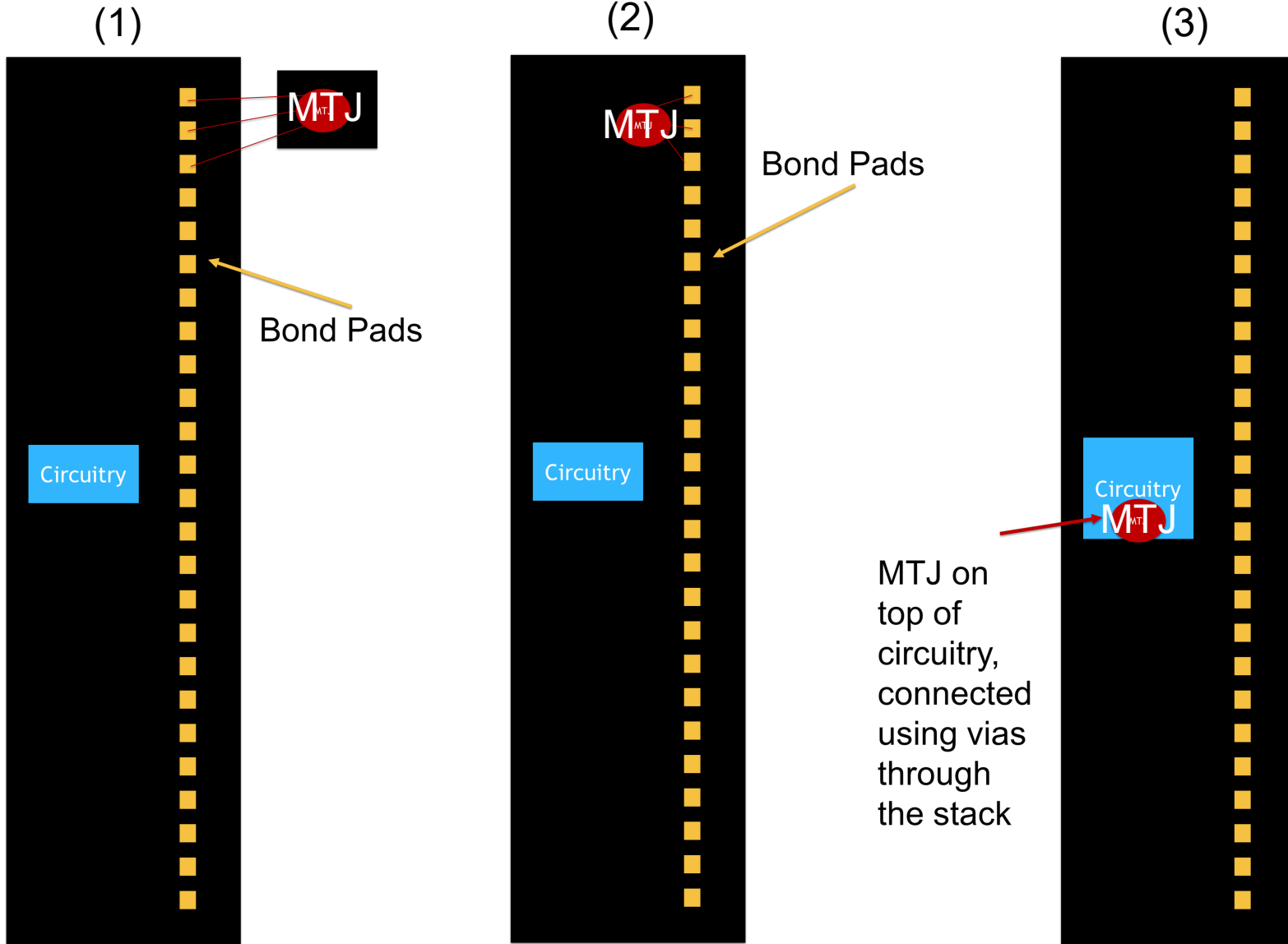
Tapeout testing in progress



- **Currently being wire bonded**



Circuit testing plan



Conclusions

- **Hybrid CMOS-magnetic latch can exploit nonvolatility at a circuit level with separate read and write paths**
- **3-terminal and 4-terminal spin switches promising due to their separated read and write paths and utilization of spin Hall switching**
- **Improved spin switches from 7% TMR to 160-200% TMR, scaled down to 200 nm wide, showing switching currents that are compatible with tapeout**
- **130 nm tapeout completed of CMOS circuit, testing in progress**
- **Next steps are full circuit integration**



