5th Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop

October, 19-20, 2017
University of California, Berkeley
Sutardja Dai Hall, Banatao Auditorium
Berkeley, CA, USA

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ORGANIZING COMMITTEE

Eli Yablonovitch, University of California, Berkeley (co-chair)
Jeffrey Bokor, University of California, Berkeley (co-chair)
Paolo Gargini, IRDS
Ru Huang, Peking University
Giuseppe Iannaccone University of Pisa
Adrian Ionescu, École Polytechnique Fédérale de Lausanne (EPFL)
Subhasish Mitra, Stanford
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5th Berkeley Symposium on Energy Efficient Electronic &
Steep Transistors Workshop

THURSDAY, OCTOBER 19, 2017

8:30 am **REGISTRATON & BREAKFAST**

9:15 am ***Welcome Remarks***

Eli Yablonovitch & Jeffrey Bokor (University of California, Berkeley, USA)

9:30 am ***Systems Benefits of Lower Operating Voltage***
Chairs: Jeffrey Bokor, Eli Yablonovitch, University of California, Berkeley, USA

9:30 am **Paolo Gargini** (IRDS, USA) *invited*
"Roadmap Evolution: From NTRS to ITRS, from ITRS 2.0 to IRDS"

9:50 am Questions & Discussion

9:55 am **Adrian Ionescu** (Ecole Polytechnique Fédérale Lausanne, Switzerland) *invited*
"Sub-unity Body Factor: The Next CMOS and Beyond CMOS Technology Booster for Enhanced Energy Efficiency?"

10:15 am Questions & Discussion

10:20 am **Subhasish Mitra** (Stanford University, USA) *invited*
"N3XT 3D Nanosystems for Energy-Efficient Abundant-Data Computing"

10:40 am Questions & Discussion

10:45 am **Takahiro Hanyu** (Tohoku University, Japan) *invited*
"Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing for IoT Applications"

11:05 am Questions & Discussion

11:10 am **BREAK**

11:25 am ***Analog and Digital Accelerators for Deep Learning***
Chair: Eli Yablonovitch, University of California, Berkeley

11:25 am **Amir Khosrowshahi** (Intel Corporation, USA) *invited keynote*
Keynote Presentation: "Building a Platform for AI"

12:00 am Questions & Discussion

12:05 am **Engin Ipek** (University of Rochester, USA) and Mahdi Nazm Bojnordi (University of Utah, USA) *invited*
"Memristive Boltzmann Machine: A Hardware Accelerator for Combinatorial Optimization and Deep Learning"

12:25 pm Questions & Discussion

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12:30 pm **LUNCH**

1:30 pm ***Steep Tunnel Transistors for Reduced Operating Voltage***
Chair: Lars-Erik Wernersson, Lund University

1:30 pm **Alan Seabaugh** (University of Notre Dame, USA) *invited*
"Advance of Steep Transistors"

1:50 pm Questions & Discussion

1:55 pm **Shinichi Takagi**, Daehwan Ahn, Takahiro Gotow, Koichi Nishi, Taeeon Bae, Takumi Katoh, Ryo Matsumura, Ryotaro Takaguchi, Kimihiko Kato and Mitsuru Takenaka (University of Tokyo, Japan) *invited*
"III-V/Ge-based Tunneling MOSFET"

2:15 pm Questions & Discussion

2:20 pm **Ru Huang**, Qianqian Huang, Yang Zhao, Cheng Chen, Rundong Jia, Lingyi Guo and Yangyuan Wang (Peking University, China) *invited*
"Steep Switch with Hybrid Operation Mechanism for Performance Improvement"

2:40 pm Questions & Discussion

2:45 pm **Peter Asbeck** and Jie Ming (University of California, San Diego, USA)
"Modeling the Influence of Dielectric Interface Traps on I-V Characteristics of TFETs"

3:00 pm Questions & Discussion

3:05 pm **BREAK**

3:20 pm ***Strategies for Neuromorphic Computing***
Chair: Jeffrey Bokor, University of California, Berkeley

3:20 pm **Yichen Shen**, Nicholas C. Harris, Dirk Englund and Marin Soljacic (Massachusetts Institute of Technology, USA) *invited*
"Deep Learning with Coherent Nanophotonic Circuits"

3:40 pm Questions & Discussion

3:45 pm **Shunsuke Fukami**, William Borders, Aleksandr Kurenkov, Chaoliang Zhang, Samik Duttagupta and Hideo Ohno (Tohoku University, Japan) *invited*
"Use of Analog Spintronics Device in Performing Neuro-morphic Computing Functions"

4:05 pm Questions & Discussion

4:10 pm **Sapan Agarwal**, Alexander Hsia, Robin Jacobs-Gedrim, David R. Hughart, Steven J. Plimpton, Conrad D. James and Matthew Marinella (Sandia National Laboratories, USA) *invited*
"Designing an Analog Crossbar-based Neuromorphic Accelerator"

4:30 pm Questions & Discussion

4:35 pm **Masanao Yamaoka** (Hitachi Ltd., Japan) *invited*
"An Ising Computing to Solve Combinatorial Optimization Problems"

4:55 pm Questions & Discussion

5:00 pm **BREAK**

5:10 pm ***Panel Discussion on Deep Learning and Neural Networks***

Moderator: Jan Rabaey, University of California, Berkeley

Panelists: Amir Khosrowshahi, Engin Ipek, Masanao Yamaoka, Yichen Shen, Shunsuke Fukami, Sapan Agarwal

5:50 pm **WALK TO POSTER SESSION**

6:00 pm ***Poster Session & Reception***

POSTER LIST

Authors	Title
Jasper Bizindavyi, Anne S. Verhulst, Quentin Smets, Devin Verreck, Nadine Collaert, Anda Mocuta, Bart Sorée and Guido Groeseneken	*Calibration of the high-doping induced ballistic band-tails tunneling current with In0.53Ga0.47As Esaki diodes*
Sarthak Gupta, Kaushal Nigam, Sunil Pandey, Dheeraj Sharma and Pravin Kondekar	*Performance Improvement of Heterojunction Double Gate Drain Overlapped TFET using Gaussian Doping*
Dheeraj Sharma, Bhagwan Ram Raad and Sukeshni Tirkey	*Channel Engineered Tunnel FET for Reduced Ambipolar Nature*
Jon Gorchon, Charles-Henri Lambert, Yang Yang, Akshay Pattabi, Sayeef Salahuddin and Jeffrey Bokor	*Single shot ultrafast all optical magnetization switching of ferromagnetic Co/Pt multilayers*
Stefan Glass, Christian Schulte-Braucks, Lidia Kibkalo, Uwe Breuer, Jean-Michel Hartmann, Dan Buca, Siegfried Mantl and Qing-Tai Zhao	*Examination of a new SiGe/Si heterostructure TFET concept based on vertical tunneling*
Rebecca Durr, Danny Haberer, Yea-Lee Lee, Alin Miksi Kalayjian, Raymond Blackwell, Tomas Marangoni, Steven Louie and Felix Fischer	*Graphene Nanoribbon Band Gap Engineering Through Orbitally Matched Dopant Atoms.*
Zhifu Liu, Peter Girouard, Pice Chen, Young Kyu Jeong, Seng-Tiong Ho and Bruce W. Wessels	*50 GHz Electro-optic Modulators with BaTiO3 Epitaxial Thin Film Platform for Short Distance Optical Communications*
Francesco Settino, Sebastiano Strangio, Marco Lanuzza, Felice Crupi, Pierpaolo Palestri and David Esseni	*Simulations and comparisons of basic analog and digital circuit blocks employing Tunnel FETs and conventional FinFETs*
Yasmine Elogail, Joerg Schulze and Inga Fischer	*Fabrication and Simulation of Vertical Ge-based P-Channel Planar-Doped Barrier FETs with 40 nm Channel Length*
Shaloo Rakheja and Kexin Li	*Graphene-Based Plasma Wave Interconnects for On-Chip Communication in the Terahertz Band*
Jun Huang, Pengyu Long, Michael Povolotskyi, Gerhard Klimeck and Mark Rodwell	*Sb- and Al- Free Ultra-High-Current Tunnel FET Designs*
Hongjuan Wang, Xiangwei Jiang, Genquan Han, Yue Hao, Shushen Li and David Esseni	*Revisiting Piezoelectric FETs with Sub-Thermal Swing*
Pin-Chun Shen and Jing Kong	*Chemical Vapor Deposition of High-Quality Monolayer Transition Metal Disulfides*
Sajjad Moazeni, Amir Atabaki, Fabio Pavanello, Hayk Gevorgyan, Jelena Notaros, Luca Alloatti, Mark Wade, Chen Sun, Seth Kruger, Huaiyu Meng, Kenaish Al Qubaisi, Imbert Wang, Bohan Zhang, Anatol Khilo, Christopher Baicco, Milos Popovic, Rajeev Ram and Vladimir Stojanovic	*Integration of Polysilicon-based Photonics in a 12-inch Wafer 65nm Bulk CMOS Process*

POSTER LIST (CONT.)

Authors	Title
Bivas Saha, Benjamin Osoba, Tsu Jae King Liu and Junqiao Wu	*Materials Engineering of Micro-relay Contact Surfaces for milli -Volt Switching*
Sri Krishna Vadlamani and Eli Yablonovitch	*On the broadening of energy levels in a quantum dot-based tunnel transistor*
Nishtha Sharma, Andrew Marshall, Jonathan Bird and Peter Dowben	*Verilog-A based Compact Modeling of the Magneto-electric FET Device*
Nishtha Sharma, Andrew Marshall, Jonathan Bird and Peter Dowben	*Novel Ring Oscillator Design Using ME-MTJ Based Devices*
William Vandenberghe	*Two-dimensional Topological Insulator Transistors as Energy Efficient Switches Robust against Material and Device Imperfections*
Ting Cao, Fangzhou Zhao, Yea-Lee Lee and Steven G. Louie	*Graphene Nanoribbons for Transistor Applications*
Taeeon Bae, Ryota Suzuki, Ryosho Nakane, Mitsuru Takenaka and Shinichi Takagi	*Effects of Ge-source impurity concentration on electrical characteristics of Ge/Si hetero-junction tunneling FETs*
Jean Anne Incorvia, Elyse Barre, Suk Hyun Kim, Connor McClellan, Eric Pop, H.-S. Philip Wong and Tony Heinz	*Near-room temperature electrical control of spin and valley Hall effect in monolayer WSe2 transistors for spintronic applications*
Sean Hooten and Eli Yablonovitch	*Metallodielectric Antenna for Spontaneous Emission Enhancement*
Sergio Almeida, David Zubia, Aldo Vidaña and Mariana Martinez	*Conductance Modulation in 2D Materials by NEMS for Lower-Power Applications*
Amal El-Ghazaly, Daisy O'Mahoney, Charles-Henri Lambert, Jon Gorchon, P. Nigel Brown, Akshay Pattabi, H.S. Philip Wong and Jeffrey Bokor	*Ultrafast Magnetic Memory Bits Using All-Optical Magnetic Switching*
Nicolas Andrade, Seth Fortuna, Kevin Han, Sean Hooten, Eli Yablonovitch and Ming Wu	*Efficient and Broadband Single-Mode Waveguide Coupling of Electrically Injected Optical Antenna Based nanoLED*
Brayan Navarrete, Mark Stone and Sakhrat Khizroev	*Properties of Magnetic Tunneling Junction Devices with Characteristic Sizes in Sub-5-nm Range*
Samuel Xavier-De-Souza, Eduardo Neves, Alex Furtunato, Luiz Silveira, Kyriakos Georgiou and Kerstin Eder	*The Benefits of Low Operating Voltage Devices to the Energy Efficiency of Parallel Systems*
Peida Zhao, Matin Amani, Der-Hsien Lien, Geun Ho Ahn, Daisuke Kiriya, James P. Mastandrea, Joel W. Ager, Eli Yablonovitch, Daryl C. Chrzan and Ali Javey	*Measuring the Edge Recombination Velocity of Monolayer Semiconductors*
Mirza M. Elahi, K. M. Masum Habib and Avik W. Ghosh	*Gate tunable transport-gap to beat the Boltzmann limit: a Graphene Klein Tunnel Field Effect Transistor*
Zhixin Alice Ye, Hei Kam and Tsu-Jae King Liu	*Negative Stiffness Structures for Energy Efficient MEM Switches*
Matin Amani, Der-Hsien Lien, Daisuke Kiriya, Geun Ho Ahn, Peida Zhao, Joel Ager, Eli Yablonovitch and Ali Javey	*High Photoluminescence Quantum Yield in Transition Metal Dichalcogenides Enabled by Superacid Treatment*
Sreetosh Goswami and T. Venkatesan	*Resistive Memory Devices using Metal-Coordinated Azo-aromatics*

FRIDAY, OCTOBER 20, 2017

8:45 am **BREAKFAST**

9:30 am ***Negative Capacitance Transistors***
Chair: Sayeef Salahuddin, University of California, Berkeley

9:30 am — **Masaharu Kobayashi** (University of Tokyo, Japan) *invited*
"Technology Breakthrough by Ferroelectric HfO2 for Ultralow Power Logic and Memory"

9:50 am — Questions & Discussion

9:55 am — **Zoran Krivokapic**, Ahmedullah Aziz, Da Song, Uzma Rana, Rohit Galatage and Srinivasa Banna (GlobalFoundries, USA) *invited*
"NCFET: Opportunities & Challenges for Advanced Technology Nodes"

10:15 am — Questions & Discussion

10:20 am **BREAK**

10:30 am ***Ultrafast Magnetic Switching***
Chair: Eli Yablonovitch, University of California, Berkeley

10:30 am — **Jeffrey Bokor** (University of California, Berkeley, USA) *invited*
"Prospects for Ultrafast MRAM with <10 psec Write Latency"

10:50 am — Questions & Discussion

10:55 am — **Lucian Prejbeanu**, Andrey Timopheev, Ricardo Sousa, Gilles Gaudin and Bernard Dieny (SPINTEC, CEA Grenoble, France) *invited*
"Ultrafast MRAM Strategies for Cache Applications and Beyond"

11:15 am — Questions & Discussion

11:20 am ***Adaptive Neural Networks***
Chair: Eli Yablonovitch, University of California, Berkeley

11:20 am — **Gert Cauwenberghs** (University of California, San Diego, USA) *invited*
"Energy Efficiency in Adaptive Neural Circuits"

11:40 am — Questions & Discussion

11:45 am **LUNCH**

12:45 pm ***New Mechanisms for Energy Efficient Computing***
Chair: Nerissa Draeger, Lam Research

12:45pm — **Farnaz Niroui**, Jatin Patil, Timothy Swager, Jeffrey Lang and Vladimir Bulovic (Massachusetts Institute of Technology, USA)
"Towards Low-Stiction Nanoelectromechanical Switches Using Self-Assembled Molecules"

1:00pm — Questions & Discussion

1:05 pm **Vladimir Stojanovic,**[1] Sajjad Moazeni,[1] Amir Atabaki,[2] Fabio Pavanello,[3] Hayk Gevorgyan,[4] Jelena Notaros,[2] Luca Alloatti,[2] Mark Wade,[5] Chen Sun,[5] Seth Kruger,[6] Huaiyu Meng,[2] Kenaish Al Qubaisi,[4] Imbert Wang,[4] Bohan Zhang,[4] Anatol Khilo,[4] Christopher Baicco,[6] Milos Popovic,[4] and Rajeev Ram[2] ([1]University of California, Berkeley, USA, [2]Massachusetts Institute of Technology, USA, [3]Ghent University-IMEC, Belgium, [4]Boston University, USA, [5]Ayar Labs, Inc., USA, [6]SUNY Polytechnic Institute, USA)
"Integration of Polysilicon-based Photonics in a 12-inch Wafer 65nm Bulk CMOS Pro cess"

1:20 pm Questions & Discussion

1:25 pm **Seth Fortuna**, Christopher Heidelberger, Nicolas Andrade, Kevin Han, Eugene Fitzgerald, Eli Yablonovitch and Ming Wu (University of California, Berkeley and Massachusetts Insitute of Technology, USA)
"Large Spontaneous Emission Rate Enhancement in a Nanoscale III-V LED Coupled to an Optical Antenna"

1:40 pm Questions & Discussion

1:45 pm **BREAK**

1:55 pm ***Defects and Energy Level Characteristics of Tunnel Transistors***
Chair: Alan Seabaugh, University of Notre Dame

1:55 pm **Jesus del Alamo**, Xin Zhao, Lu Wenjie and Vardi Alon (Massachusetts Institute of Technology, USA) *invited*
"Towards Sub-10 nm Diameter InGaAs Vertical Nanowire MOSFETs and TFETs"

2:15 pm Questions & Discussion

2:20 pm **Lars-Erik Wernersson** (Lund University, Sweden) *invited*
"III-V Nanowire TFETs: Performance, Statistics, and Band Edge Sharpness"

2:40 pm Questions & Discussion

2:45 pm **Anne Verhulst**,[1] Devin Verreck,[1] William G. Vandenberghe,[2] Quentin Smets,[1] Mazharuddin Mohammed,[1,3] Jasper Bizindavyi,[1,3] Marc M. Heyns,[1,3] Bart Soree,[1,3,4] Nadine Collaert,[1] and Anda Mocuta[1] ([1]IMEC, Leuven, Belgium, [2]Univ. of Texas at Dallas, USA, [3]KU Leuven, Belgium, [4]UAntwerp, Belgium) *invited*
"Inherent Transmission Probability Limit Between Valence-band and Conduction-band States and Calibration of Tunnel-FET Parasitics"

3:05 pm Questions & Discussion

3:10 pm **Felix Fischer** (University of California, Berkeley, USA)
"Graphene Nanoribbon Band Gap Engineering Through Orbitally Matched Dopant Atoms"

3:25 pm Questions & Discussion

3:30 pm **Sheikh Ahmed**, Yaohua Tan, Daniel Truesdell and Avik Ghosh (University of Virginia, USA)
"Auger Effect Limited Performance in Tunnel Field Effect Transistors"

3:45 pm Questions & Discussion

3:50 pm ***Closing Remarks***

Eli Yablonovitch & Jeffrey Bokor (University of California, Berkeley, USA)

Keynote Speaker

Amir Khosrowshahi is VP and CTO of the AI Products Group at Intel. He was co-founder and CTO of Nervana, a startup developing processors and solutions for deep learning, acquired by Intel last year. Amir has a research background in neuroscience, machine learning, and distributed computing. He started his career in finance and was a derivatives trader at Goldman, Sachs. He has a AB and AM from Harvard and PhD from Berkeley.

Invited Speakers

Sapan Agarwal is a Senior Member of Technical Staff at Sandia National Laboratories in Livermore, CA. He completed his PhD in Electrical Engineering in 2012 at UC Berkeley in the Center for Energy Efficient Electronics with Professor Eli Yablonovitch. He received the B.S. degree with highest honors in electrical engineering from the University of Illinois, Urbana Champaign, in 2007. He is a member of the IEEE International Roadmap for Devices and Systems (formerly ITRS). His research interests include brain inspired computing, neural networks, adaptive machine learning, resistive memory, low power electronics, semiconductor devices and optoelectronic devices.

Jeffrey Bokor is the Paul R. Gray Distinguished Professor of Engineering in the department of Electrical Engineering and Computer Sciences (EECS) at UC Berkeley, with a joint appointment as Senior Scientist in the Materials Science Division at Lawrence Berkeley National Laboratory. He also serves as Chair of the Electrical Engineering Division in the EECS Department. He received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology in 1975, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1976 and 1980, respectively. He joined the Berkeley faculty in 1993. His current research activities include nanomagnetics/spintronics, graphene electronics, nanophotonics, and nanoelectromechanical systems. He is a fellow of IEEE, APS, and OSA.

Gert Cauwenberghs is Professor of Bioengineering and Co-Director of the Institute for Neural Computation at UC San Diego, La Jolla CA. His research focuses on micropower integrated biomedical circuits, neuron-silicon and brain-machine interfaces, neuromorphic engineering, and adaptive intelligent systems. He is a Fellow of the Institute of Electrical and Electronic Engineers (IEEE) and the American Institute for Medical and Biological Engineering (AIMBE). He served IEEE in a variety of roles including as Distinguished Lecturer of the IEEE Circuits and Systems Society, as General Chair of the IEEE Biomedical Circuits and Systems Conference (BioCAS 2011, San Diego), as Program Chair of the IEEE Engineering in Medicine and Biology Conference (EMBC 2012, San Diego), and as Editor-in-Chief of the IEEE Transactions on Biomedical Circuits and Systems.

Jesús A. del Alamo is Director of the Microsystems Technology Laboratories, Donner Professor, and Professor of Electrical Engineering at Massachusetts Institute of Technology. He holds a PhD degree from Stanford University. His research interests focus on the physics, technology, modeling and reliability of new III-V and III-N field-effect transistors for future logic, communications and power switching applications. He was awarded the 2012 Intel Outstanding Researcher Award in Emerging Research Devices and the Semiconductor Research Corporation 2012 Technical Excellence Award. He is a Fellow of IEEE and APS and a member of the Royal Spanish Academy of Engineering.

Shunsuke Fukami received Ph. D. degree (Doctor of Engineering) from Nagoya University in 2012. He joined NEC Corp (2005). He moved to Tohoku University as an Assistant Professor (2011) and then as an Associate Professor (2015). He is working on spintronics devices and its application to integrated circuits.

In 2012 **Dr. Paolo Gargini** returned to the world of research (e.g., IRDS, IEUVI, ICCI, Stanford University, UC Berkeley etc.). During his 34 years at Intel Dr. Gargini was Director of Technology Strategy in Santa Clara, California. He was also responsible for worldwide outside research activities. Dr. Gargini did research at Stanford University and Fairchild R&D from 1970 to 1977. He then developed technologies at Intel and in 1985 he headed the first submicron team. In 1995, Dr. Gargini was elevated to Intel Fellow. He was the Chairman of I300I, NRI and a member of Sematech Board. From 1998 to 2015, he was the Chairman of the ITRS and then Chairman of IRDS since 2016. He is the Chairman of IEUVI. Dr. Gargini was inducted in the VLSI Research Hall of Fame in 2009. Dr. Gargini became an International Fellow of JSAP in 2014.

Takahiro Hanyu received the B.E., M.E. and D.E. degrees in Electronic Engineering from Tohoku University, Sendai, Japan, in 1984, 1986 and 1989, respectively. He is currently a Professor and Vice Director in the Research Institute of Electrical Communication, Tohoku University. His general research interests include nonvolatile logic circuits and their applications to ultra-low-power and/or highly dependable VLSI processors, and post-binary computing and its application to brain-inspired VLSI systems. He received the Sakai Memorial Award from the Information Processing Society of Japan in 2000, the Judge's Special Award at the 9th LSI Design of the Year from the Semiconductor Industry News of Japan in 2002, Technology by MEXT, Japan in 2015. Dr. Hanyu is a Senior Member of the IEEE.

Adrian M. Ionescu is Full Professor at the Swiss Federal Institute of Technology, Lausanne, Switzerland. He received the B.S./M.S. and Ph.D. degrees from the Polytechnic Institute of Bucharest, Romania and the National Polytechnic Institute of Grenoble, France, in 1989 and 1997, respectively. He is the 2013 recipient of the IBM Faculty Award in Engineering. He served the IEDM and VLSI conference technical committees and was the Technical Program Committee (Co) Chair of ESSDERC in 2006 and 2013. He is director of the Laboratory of Micro/Nanoelectronic Devices (NANOLAB). He is appointed as national representative of Switzerland for the European Nanoelectronics Initiative Advisory Council (ENIAC) and member of the Scientific Committee of CATRENE. Dr. Ionescu is the European Chapter Chair of the ITRS Emerging Research Devices Working Group.

Masaharu Kobayashi (M'09) received the B.S. and M.S. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 2004 and 2006, and the Ph.D. degree in electronics engineering from Stanford University, Stanford, CA, in 2010. He joined the IBM T.J. Watson Research Center, Yorktown Heights, NY, in 2010, where he worked on advanced CMOS technologies such as FinFET, nanowire FET, SiGe channel and III-V channel. He was also engaged in launching 14nm SOI FinFET and RMG technology development. Since 2014, he has been an Associate Professor in Institute of Industrial Science, University of Tokyo, Tokyo, Japan, where he has been working on ultralow power transistor and memory technology. Dr. Kobayashi is a member of IEEE and JSAP.

Subhasish Mitra is Professor of Electrical Engineering and of Computer Science at Stanford University, where he directs the Stanford Robust Systems Group and co-leads the Computation focus area of the Stanford SystemX Alliance. He is also a faculty member of the Stanford Neurosciences Institute. Prof. Mitra holds the Carnot Chair of Excellence in Nanosystems at CEA-LETI in Grenoble, France. Before joining the Stanford faculty, he was a Principal Engineer at Intel Corporation. Prof. Mitra's research interests range broadly across robust computing, nanosystems, VLSI design, validation, test and electronic design automation, and neurosciences. Prof. Mitra's honors include the Semiconductor Research Corporation's Technical Excellence Award, the Intel Achievement Award , and many others.

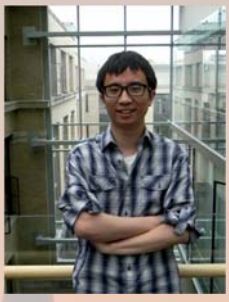
Ru Huang is currently a professor and the Dean of School of EECS, Peking University. She is an elected academician of Chinese Academy of Science and IEEE Fellow. Her research interests include low-power devices, nano-scaled CMOS devices, emerging memory technology, new devices for neuromorphic computing, and device variability/reliability. She has authored or coauthored five books，more than 250 papers, and gave nearly 40 invited talks at international conferences. She is the holder of more than 200 granted patents. Prof. Huang is an editor of IEEE T-ED. She is the Chair of IEEE EDS SRC Region 10 and elected BoG member.

Engin Ipek is an Associate Professor of Electrical & Computer Engineering at the University of Rochester. His research interests are in energy-efficient architectures, high-performance memory systems, and the application of emerging technologies to computer systems. Prof. Ipek received his BS (2003), MS (2007), and Ph.D. (2008) degrees from Cornell University, all in Electrical and Computer Engineering. Prior to joining the University of Rochester, he was a researcher in the computer architecture group at Microsoft Research (2007-2009). His work has been recognized by the 2014 IEEE Computer Society TCCA Young Computer Architect Award, an HPCA 2016 distinguished paper award, three IEEE Micro Top Picks awards, and many others.

Zoran Krivokapic is a senior member of technical staff at GLOBALFOUNDRIES ,a leading full-service semiconductor design, development, fabrication and innovation company with locations across the globe.

Lucian Prejbeanu holds a Physics degree from Babes Bolyai University in Cluj (Romania), a PhD in Physics from Louis Pasteur University in Strasbourg where he pioneered the work on magnetic nanostructures. He joined SPINTEC research laboratory in Grenoble, where he pioneered scientific work on thermally assisted MRAM, tackling the key long-standing problem of bits stable enough for long-term storage. From this, Crocus Technology was founded in 2006 to develop and commercialize thermally assisted MRAM technology. Lucian joined Crocus Technology as R&D manager. Lucian returns to Spintec as deputy director and became executive director as of January 1st, 2016, working on advanced STT-MRAM strategies, hybrid CMOS-MRAM circuits and magnetic sensors.

Alan Seabaugh (S'78–M'79–SM'92–F'03) received the Ph.D. degree in electrical engineering from the University of Virginia, Charlottesville, VA, in 1985. He worked at the National Bureau of Standards, Texas Instruments, and Raytheon before joining the University of Notre Dame as Professor of Electrical Engineering. He is the Director of the SRC/DARPA STARnet Center for Low Energy Systems Technology.



Yichen Shen is currently a post-doc associate in Prof. Marin Soljacic's group at MIT. Research interests covers theoretical and experimental Nanophotonics, deep Learning and optical computing. His research interests covers theoretical and experimental Nanophotonics, Deep Learning and Optical Computing.

Shinichi Takagi received the B.S., M.S. and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1982, 1984 and 1987, respectively. He joined the Toshiba Research and Development Center, Kawasaki, Japan, in 1987, where he has been engaged in the research on the device physics of Si MOSFETs. From 1993 to 1995, he was a Visiting Scholar at Stanford University. In October 2003, he moved to the University of Tokyo, where he is currently working as a professor in the department of Electrical Engineering and Information Systems, School of Engineering.

Anne S. Verhulst received the master degree in electrical engineering from KU Leuven, Leuven, Belgium and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 2004. She joined imec, Leuven, Belgium, in 2005. Her research interests include modeling and calibration of ideal and parasitic performance of tunnel field -effect transistors.

Lars-Erik Wernersson received the M.S degree the Ph.D. degree in Solid State Physics at Lund University in 1993 and 1998, respectively. Since 2005 he is Professor in Nanoelectronics at Lund University, following a position at University of Notre Dame 2002/2003. His main research topics include nanowire- and tunneling- based nanoelectronic devices and circuits for low-power electronics and wireless communication. He has authored/co-authored more than 200 scientific papers. He has been awarded two individual career grants and he served as Editor for IEEE Transaction on Nanotechnology. He is coordinator for the H2020 project INSIGHT.

Masanao Yamaoka received the B.E., M.E., and ph. D degrees in Electronics and Communication Engineering from Kyoto University, Kyoto, Japan, in 1996, 1998, and 2007 respectively. In 1998, he joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, where he engaged in the research and development of low-power embedded SRAM and CMOS circuits. Since 2012, he has been engaging in the research of new-paradigm computing using CMOS circuits.

Thank You for Attending

The 5th Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop

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