Characterization of Low-Voltage Micro-Electro-Mechanical Relay Integrated Circuits

Angelica Perlas[1], Zhixin Alice Ye[2], and Tsu-Jae King Liu, Ph.D.[2]
[1]Ventura College
[2]University of California, Berkeley, Department of Electrical Engineering and Computer Science

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Abstract— With the emergence of the Internet of Things, the search for more energy-efficient semiconductor devices has begun. Micro-electro-mechanical (MEM) switches, or relays, have been proposed as alternatives to complementary metal-oxide-semiconductor (CMOS) transistors for ultra-low-power digital logic applications, such as in very-large-scale integrated circuits. This is because the relay mechanism imposes no subthreshold leakage, a switching behavior that CMOS transistors cannot achieve due to the 60 mV/decade minimum subthreshold swing at room temperature. Previous research has successfully demonstrated that a single-relay-based inverter circuit actuates reliably with a sub-100 mV switching voltage[1]. We aim to demonstrate the reliable low-voltage operation of relay-based integrated circuits. To do this, we characterized different pass-gate logic circuits operating in body bias mode, which enables lower switching voltage. A 2-to-1 multiplexer, or mux, and an OR gate are investigated. The demonstration of MEM switches integrated in low-voltage digital circuits will enable scientists and engineers to design more energy-efficient computer chips.

INTRODUCTION

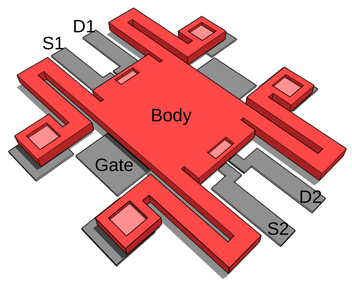
OBJECTIVE

Demonstrate and characterize different pass-gate logic circuits: 2-to-1 mux and OR gate operating in body bias mode on a CLICKR7 chip

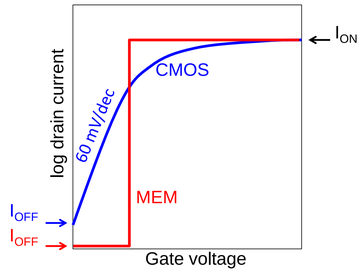
MEM SWITCHES

- Ideal switching behavior due to its zero OFF-state leakage current
- Not limited by the 60 mV/decade minimum subthreshold swing at 300K, allowing a more abrupt switching than CMOS transistors
- Low-cost fabrication

MEM relay diagram

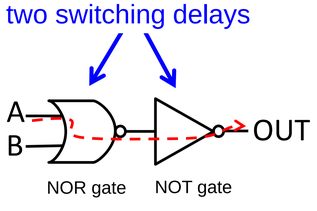


CMOS vs. MEMS

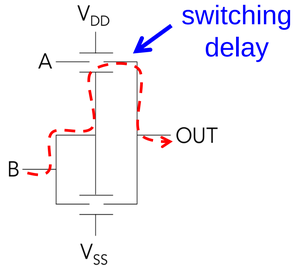


MEM SWITCHES IN PASS-GATE LOGIC CIRCUITS

- Switching delay is minimized
- Reduced number of devices in a circuit since complementary logic is not required



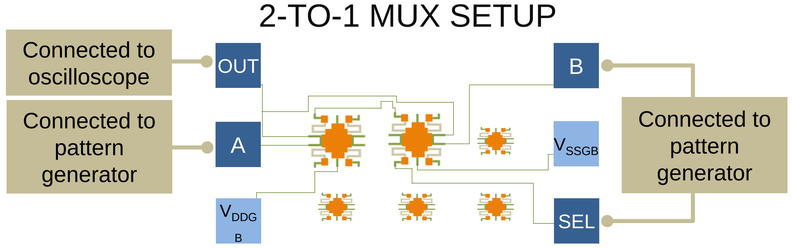
OR gate logic with CMOS Transistors



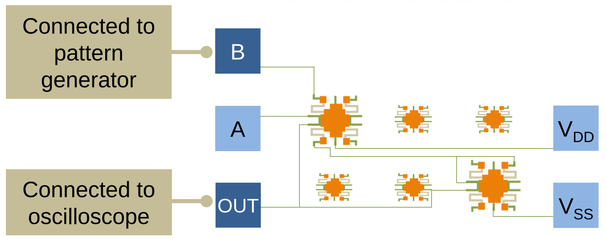
OR gate logic with MEM Switches

METHODS

2-TO-1 MUX SETUP



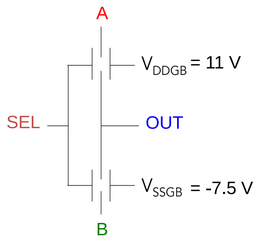
OR GATE SETUP



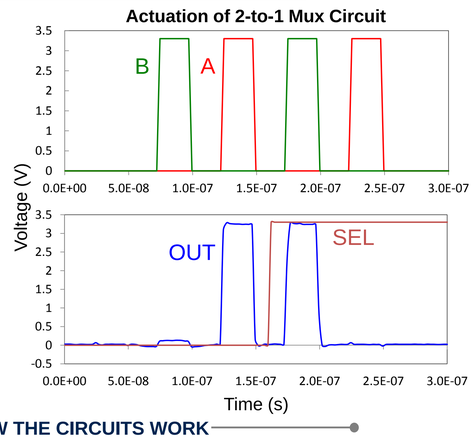
EXPERIMENTAL PROCEDURE

1. Perform oxide breakdown process on each device.
2. Determine the appropriate body bias voltage to actuate each device.
3. Test the whole circuit, adjusting the appropriate body bias voltage for each device.

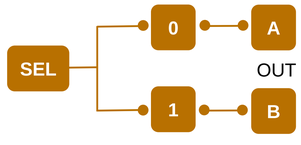
DATA ANALYSIS



2-to-1 mux circuit diagram



HOW THE CIRCUITS WORK



2-to-1 Mux Logic

A	B	A+B
0	0	0
1	0	1
0	1	1
1	1	1

OR Gate Logic

RESULTS

- 2-to-1 mux circuit actuated with 3.3 V input voltage on new-released CLICKR7 chip
- Low-voltage operation for 2-to-1 mux was not achieved due to equipment limitations
- OR gate does not actuate due to these possible reasons:

CONTACT RESISTANCE
- Oxide breakdown process applies too much voltage on the drain (set to 0 V)
- The electrodes degrade due to joule heating

OVERDRIVE VOLTAGE
- The set of chips tested are sensitive to applied gate-body voltage, causing pull-in mode operation at high overdrive gate voltage

CONCLUSION

Relay-based 2-to-1 mux circuit was successfully demonstrated and improvements on the experiment setup will help in achieving low-voltage operation of pass-gate MEM relay logic.

Future Plans

- Implement a buffer to the system to achieve low-voltage operation
- Develop an oxide breakdown process that can minimize device failure
- Investigate the effects of ambient environment to the reliability of the devices on the CLICKR7 chip

REFERENCES

[1] C. Qian, A. Peschot, B. Osoba, Z. A. Ye and T. J. K. Liu, "Sub-100 mV Computing With Electro-Mechanical Relays," in *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 1323-1329, March 2017.

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CONTACT INFORMATION
acperlas1@gmail.com
(805) 394-9752

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