Towards Sub-10 nm Diameter InGaAs Vertical nanowire MOSFETs and TFETs

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5th Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop

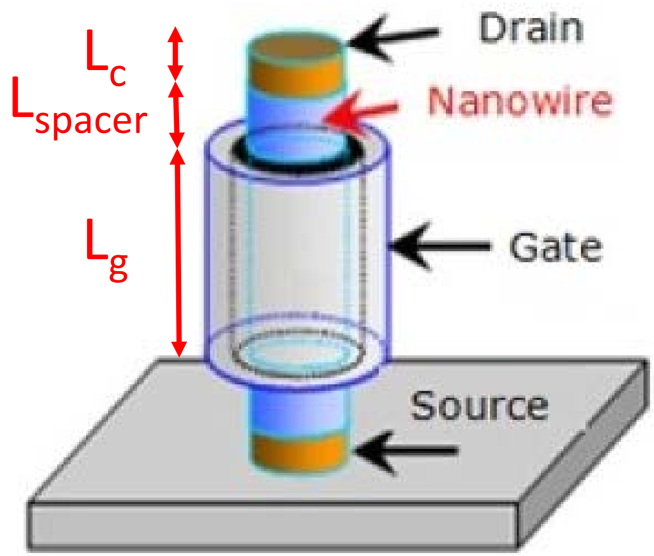
Berkeley, CA, October 19-20, 2017

Acknowledgements:

- Students and collaborators: D. Antoniadis, E. Fitzgerald, E. Yablonovitch
- Sponsors: DTRA, KIST, Lam Research, Samsung, SRC
- Labs at MIT: MTL, EBL

Vertical Nanowire MOSFETs: the ultimate scalable transistor

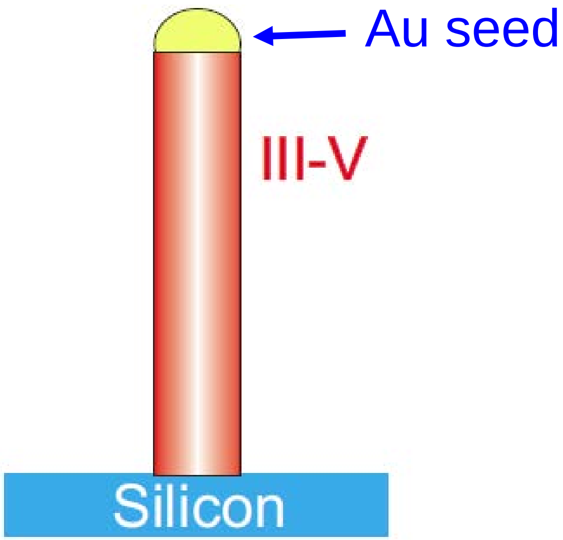
Vertical nanowire MOSFET: ultimate scalable transistor



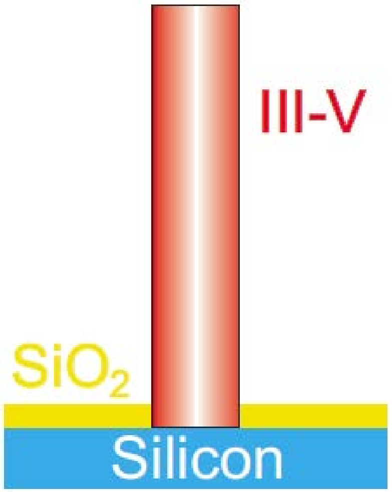
Vertical NW MOSFET:

→ uncouples footprint scaling from L_g, L_{spacer}, and L_c scaling

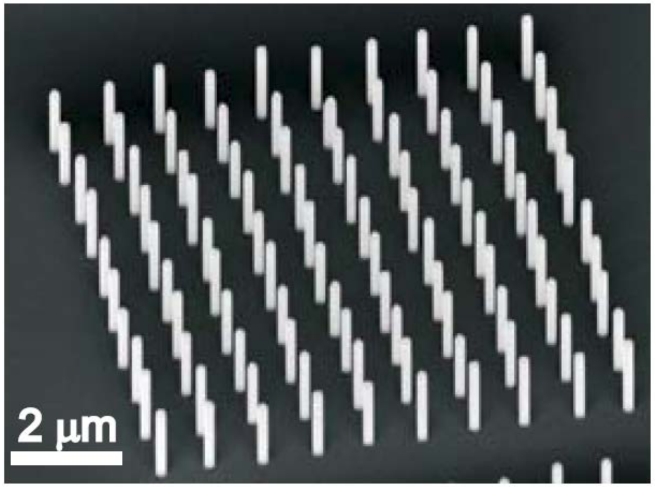
InGaAs Vertical Nanowires on Si by direct growth



Vapor-Solid-Liquid (VLS) Technique

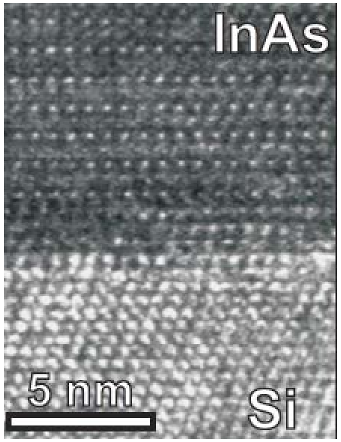


Selective-Area Epitaxy (SAE)



InAs NWs on Si by SAE

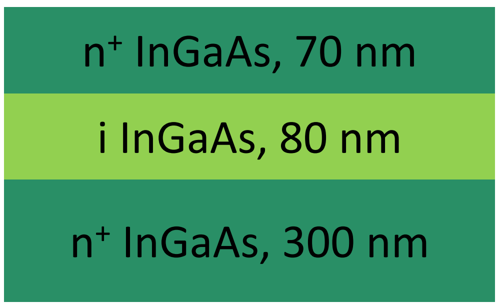
Riel, MRS Bull 2014



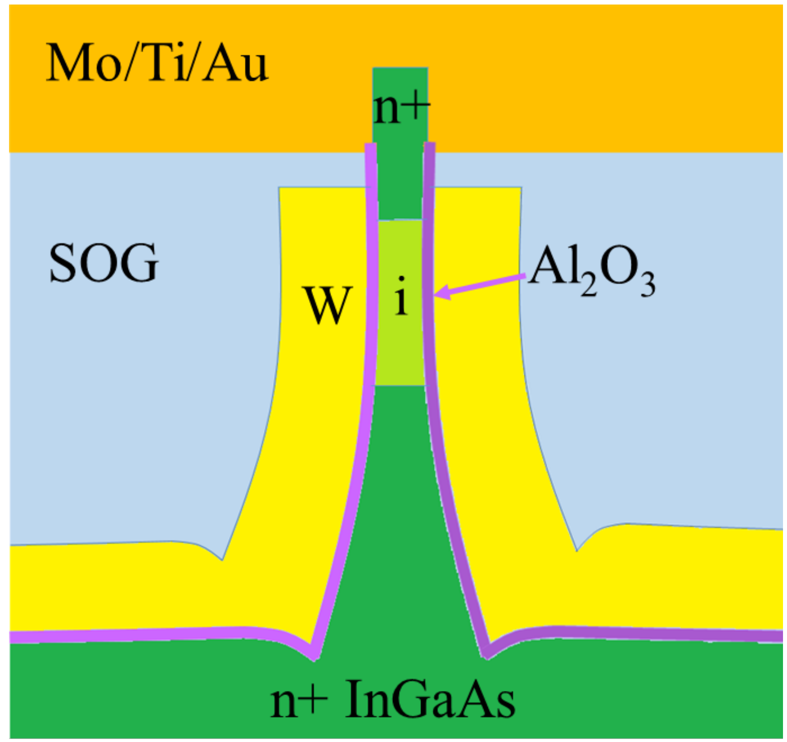
Riel, IEDM 2012

InGaAs VNW-MOSFETs by top-down approach @ MIT

Starting heterostructure:



n^+: 6×10^{19} cm^{-3} Si doping



Top-down approach: flexible and manufacturable

InGaAs Vertical Nanowires @ MIT

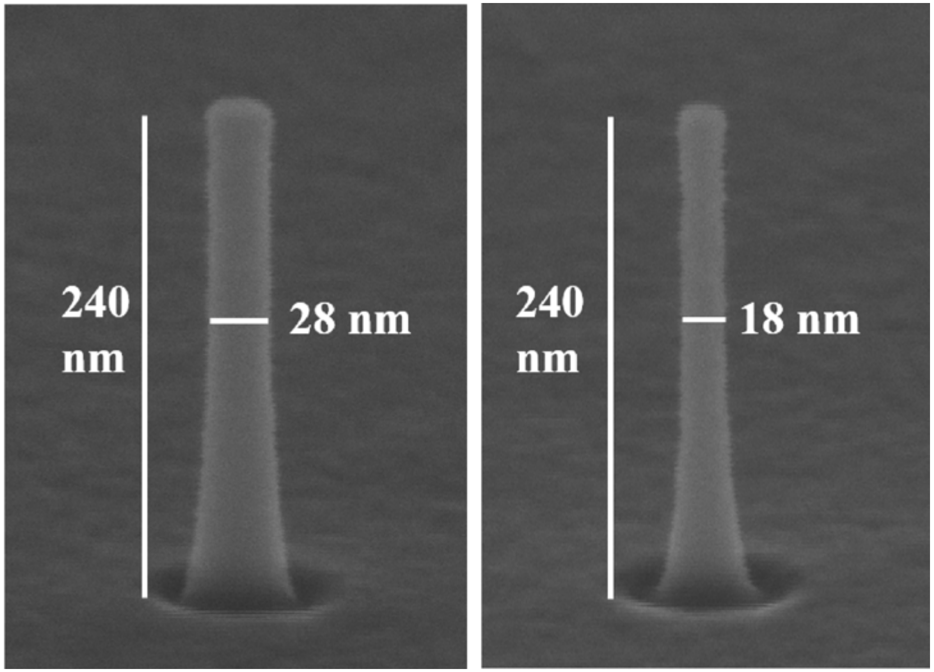
Key enabling technologies:

- RIE = $BCl_3/SiCl_4/Ar$ chemistry
- Digital Etch (DE) =

self-limiting O_2 plasma oxidation + H_2SO_4 or HCl oxide removal

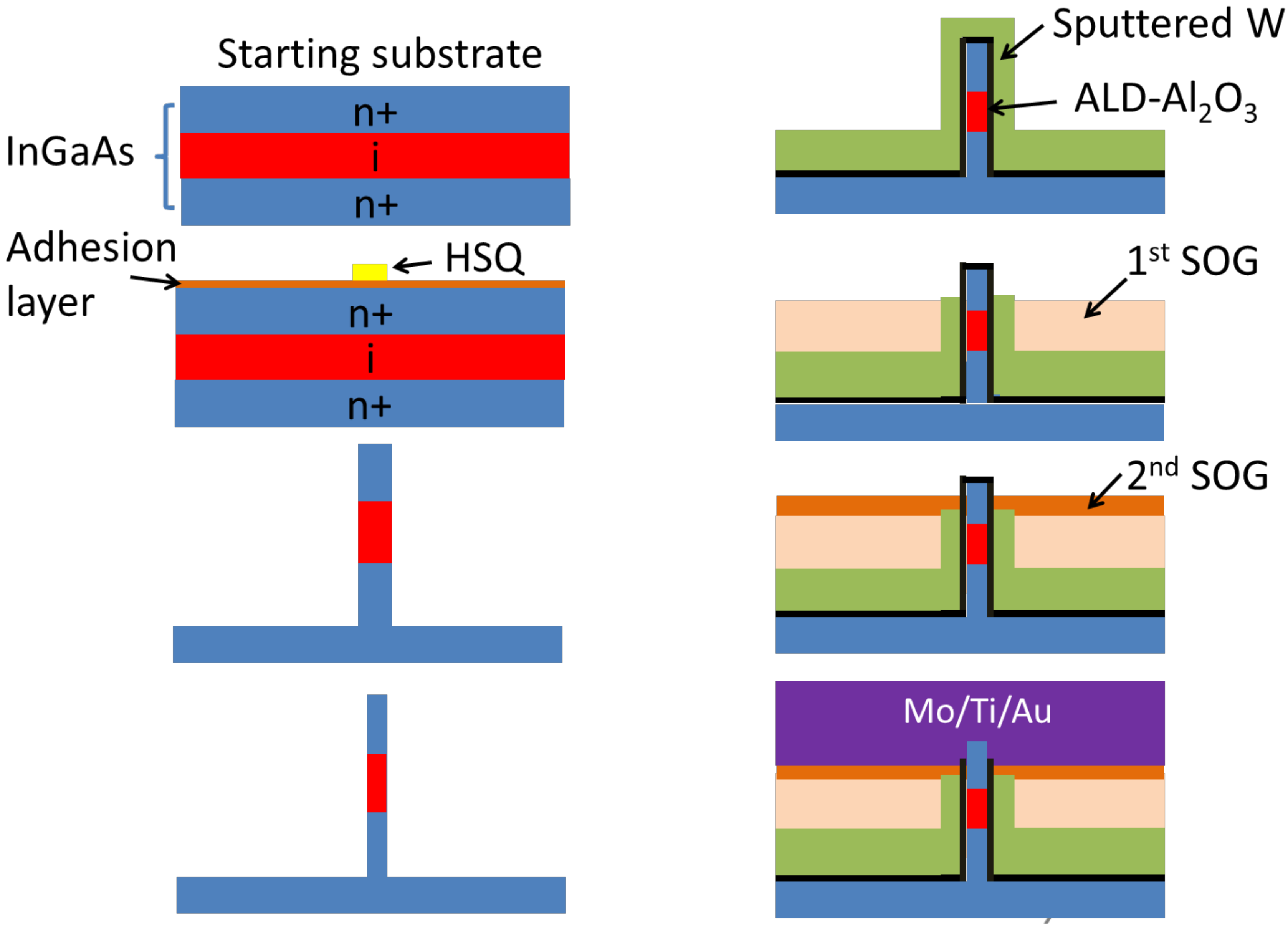
- Radial etch rate=1 nm/cycle
- Sub-20 nm NW diameter
- Aspect ratio > 10
- Smooth sidewalls

RIE + 5 cycles DE

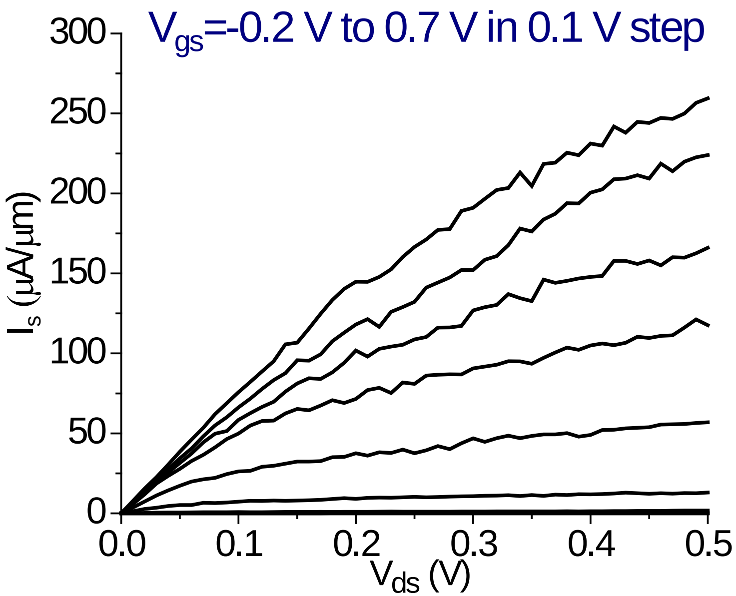


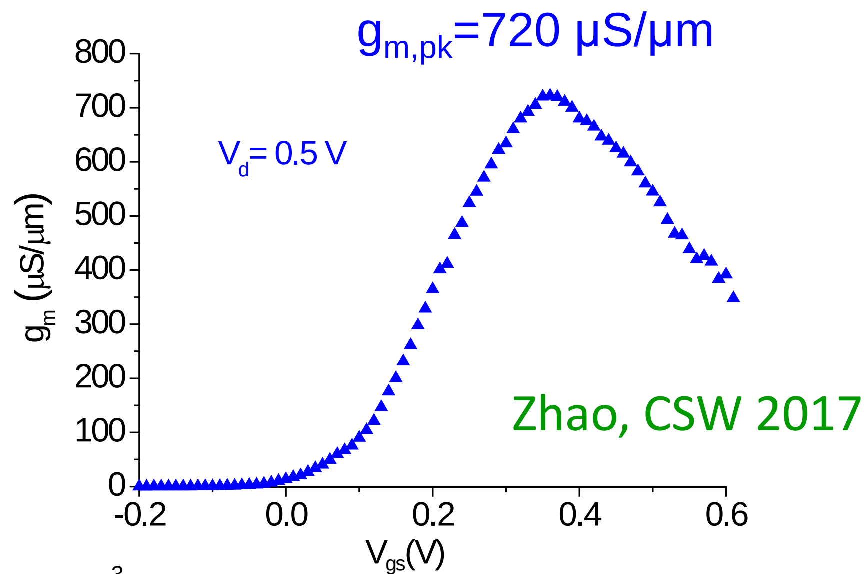
Zhao, IEDM 2013
Zhao, EDL 2014
Zhao, IEDM 2014

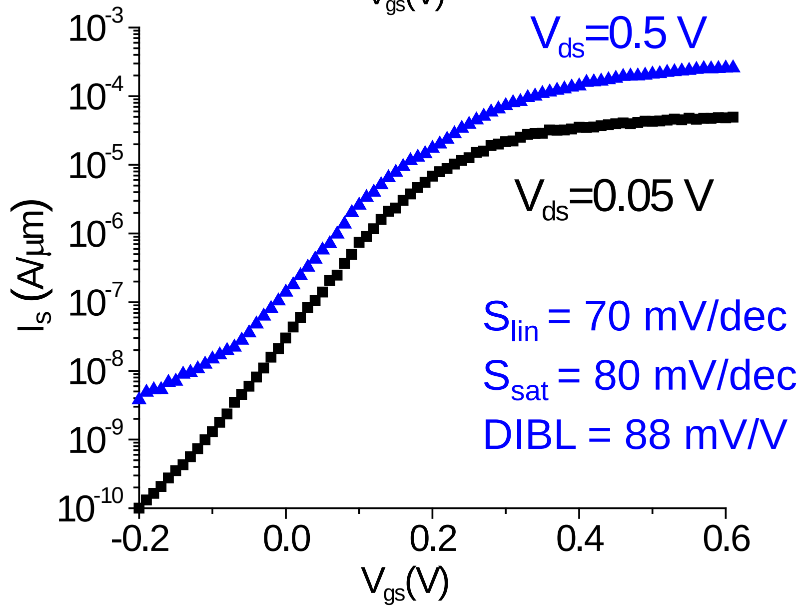
III-V VNW MOSFET/TFET process flow



NW-MOSFET I-V characteristics: D=40 nm





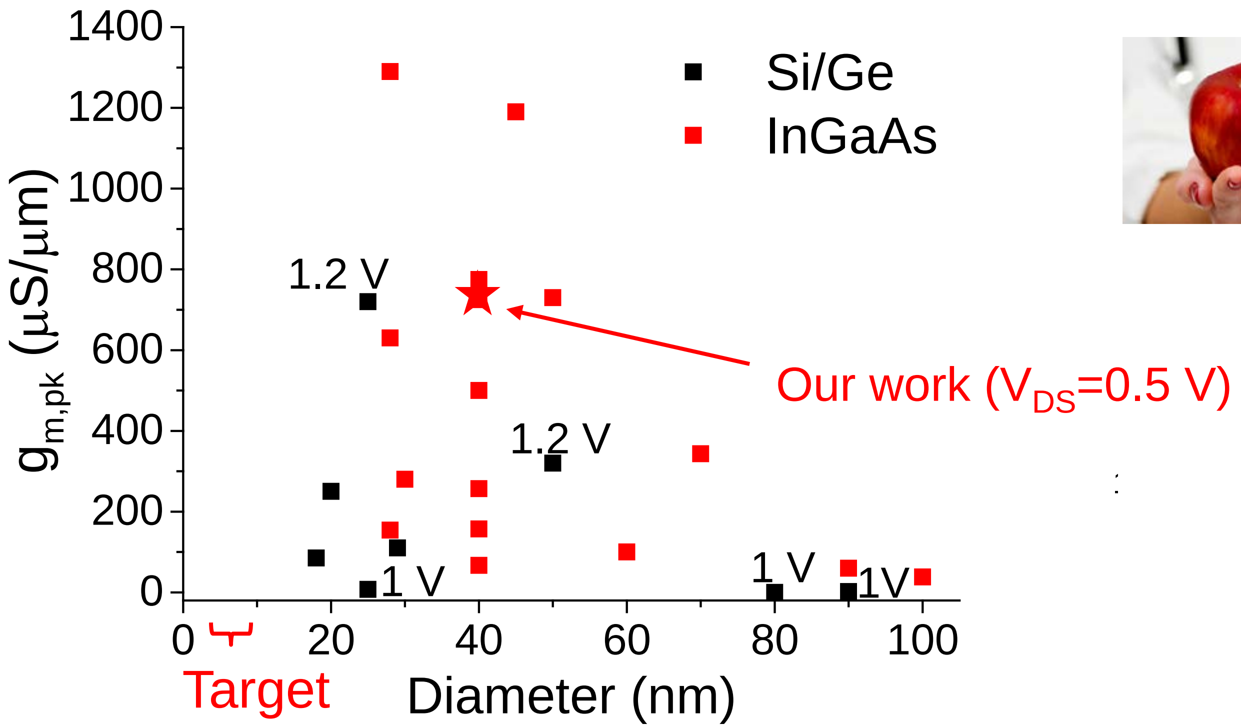


Single nanowire MOSFET:

- L_{ch}= 80 nm
- 3 nm Al_2O_3 (EOT = 1.5 nm)

Benchmark with Si/Ge VNW MOSFETs

Peak g_m of InGaAs (V_{DS}=0.5 V), Si and Ge VNW MOSFETs

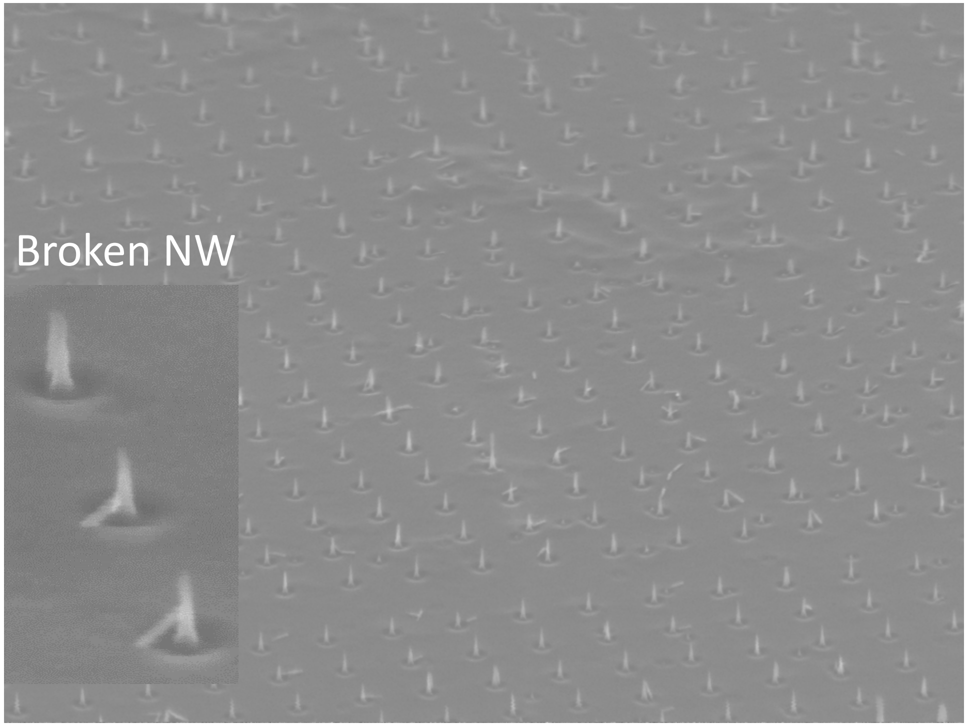


- InGaAs competitive with Si
- Need to demonstrate VNW MOSFETs with D<10 nm

InGaAs VNW Mechanical Stability for D<10 nm

8 nm InGaAs VNWs after 7 DE cycles:

8 nm InGaAs VNWs: Yield = 0%



Difficult to reach 10 nm VNW diameter due to breakage

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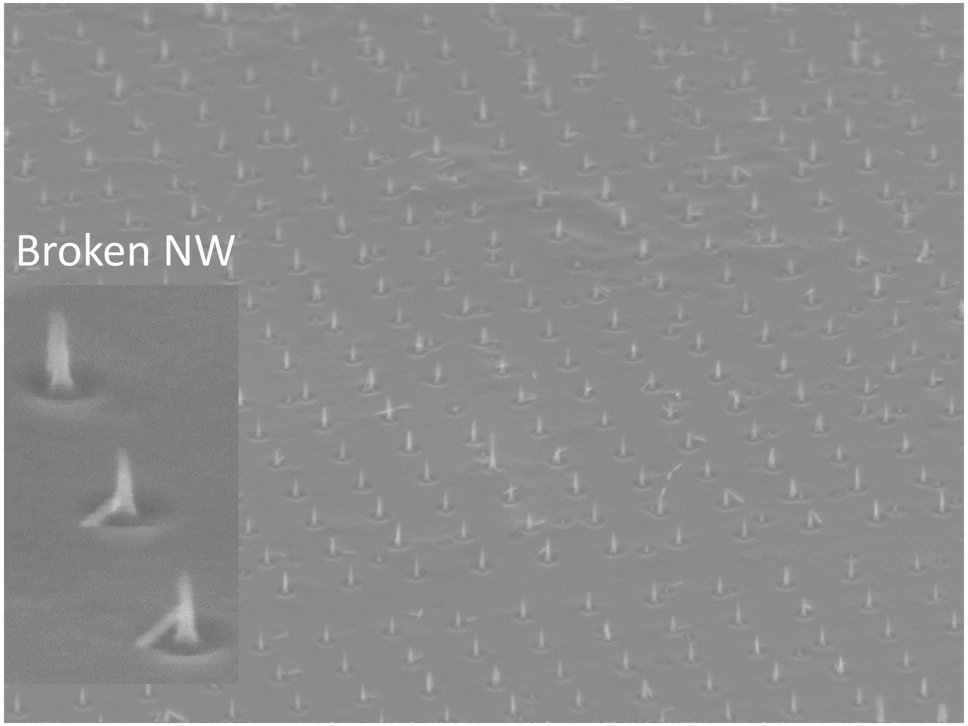


Water-based acid is problem:

Surface tension (mN/m):

- Water: 72
- Methanol: 22
- IPA: 23

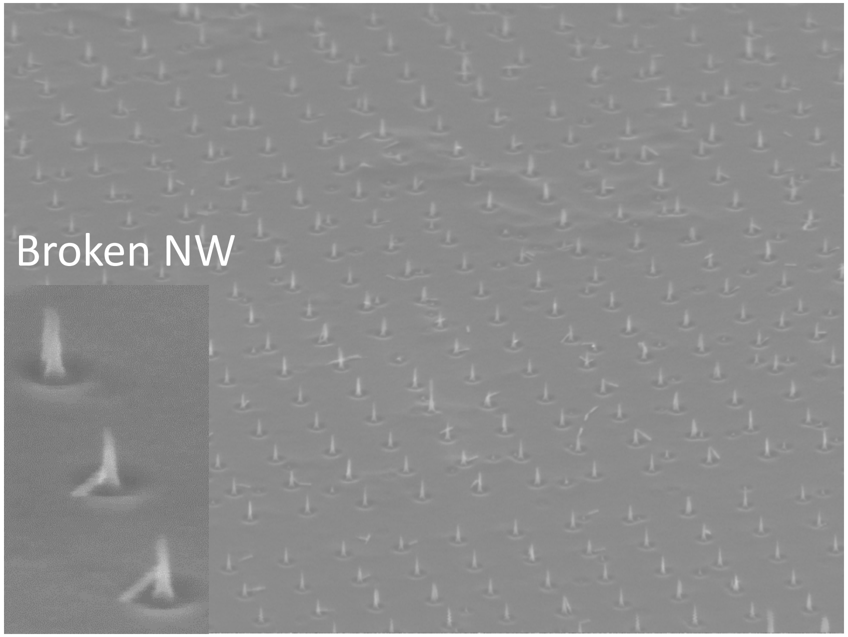
Solution: *alcohol-based digital etch*

Alcohol-Based Digital Etch

8 nm InGaAs VNWs after 7 DE cycles:

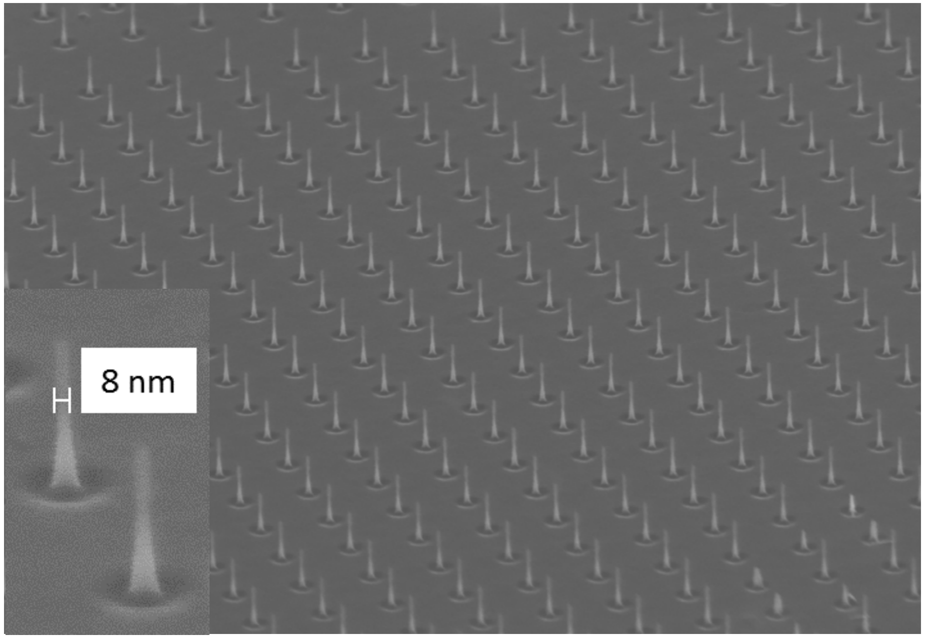
Lu, EDL 2017

10% HCl in DI water
Yield = 0%



Radial etch rate: 1.0 nm/cycle

10% HCl in IPA
Yield = 97%

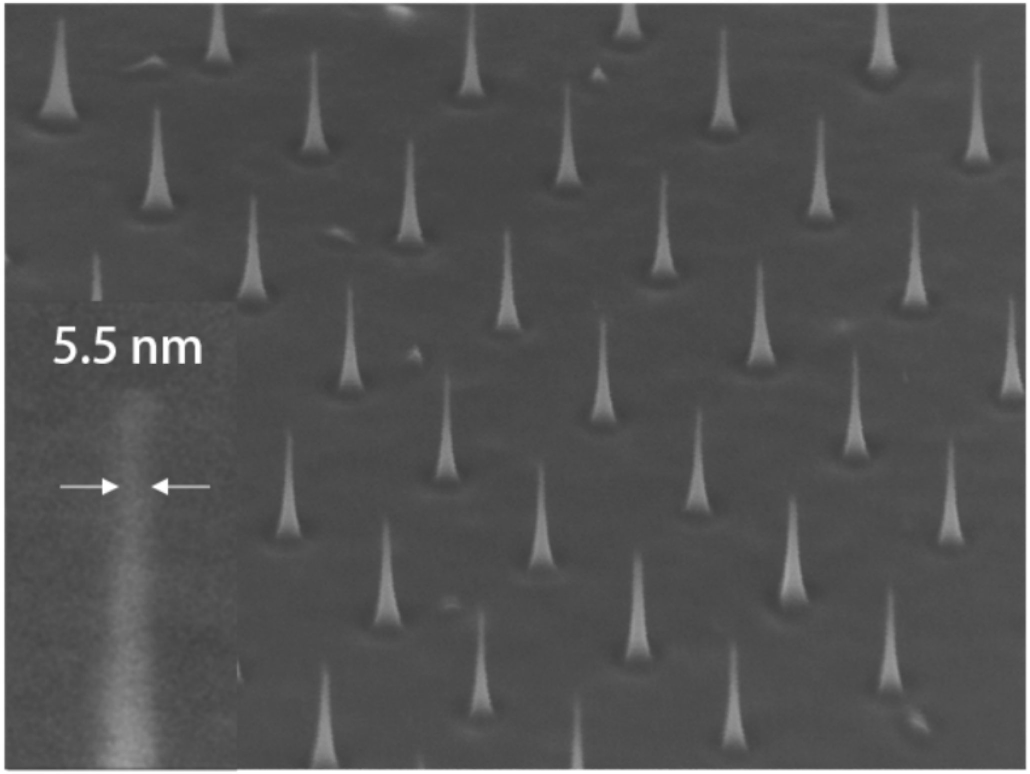


Radial etch rate: 1.0 nm/cycle

Alcohol-based DE enables D < 10 nm

D=5.5 nm VNW arrays

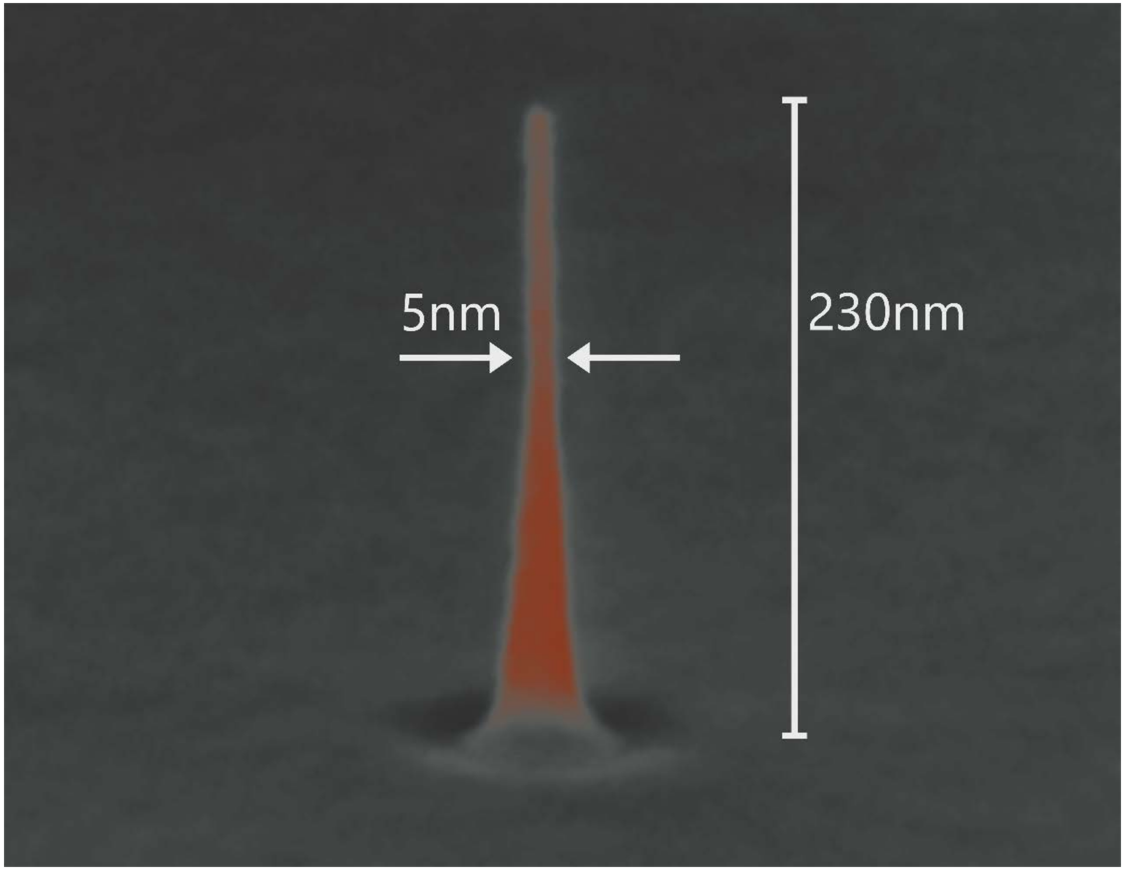
10% H_2SO_4 in methanol



90% yield

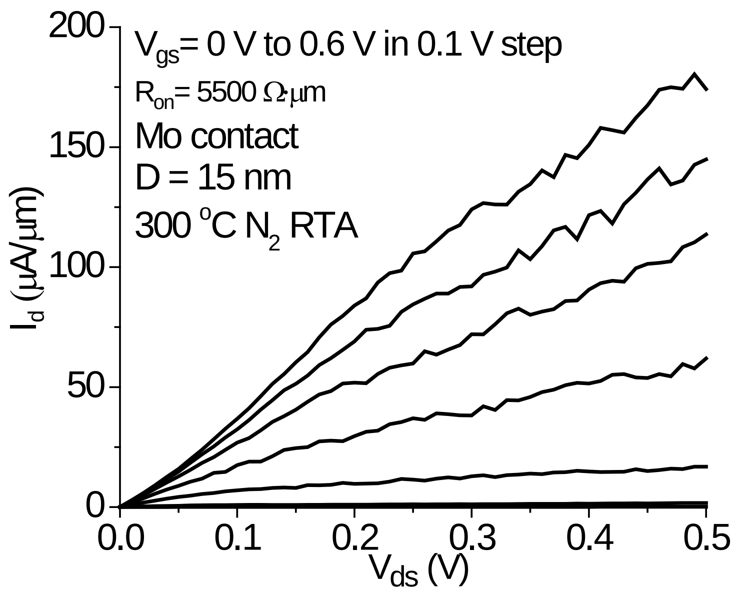
- H_2SO_4:methanol yields 90% at D=6 nm!
- Viscosity matters: methanol (0.54 cP) vs. IPA (2.0 cP)

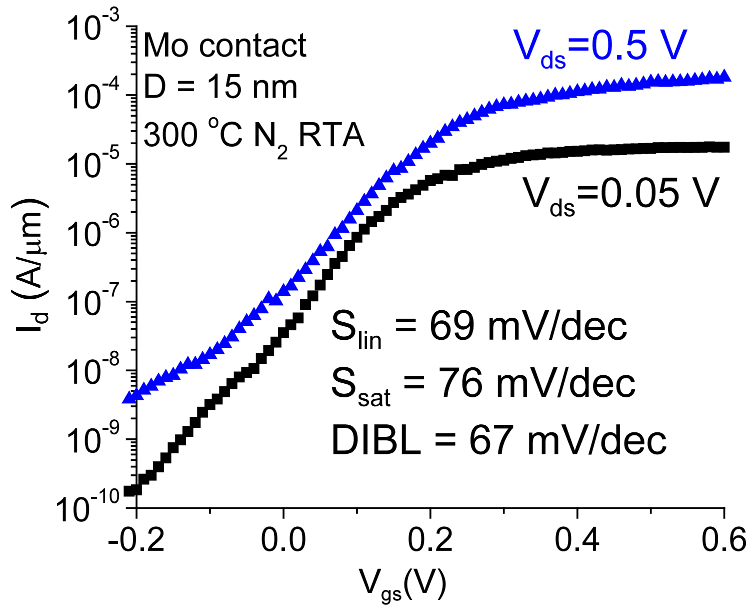
InGaAs Digital Etch

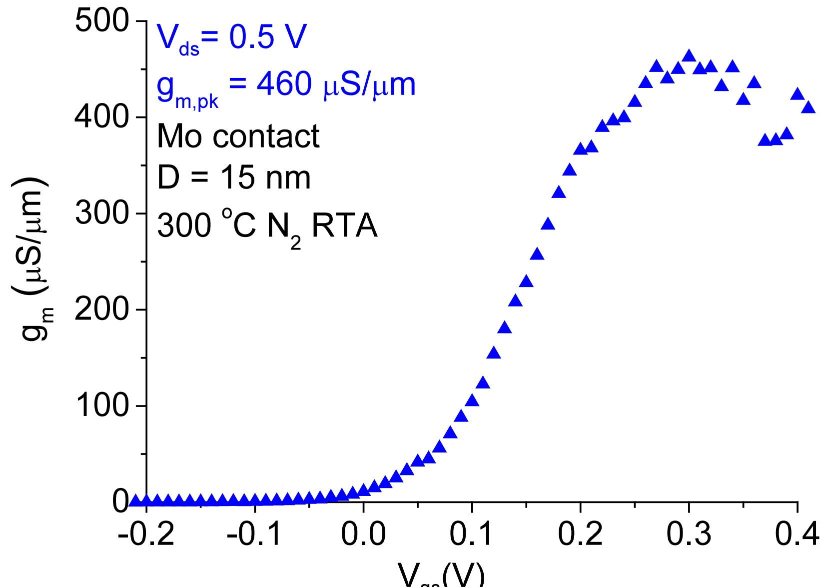


First demonstration of D=5 nm diameter InGaAs VNW
(Aspect Ratio > 40)

Latest! D=15 nm InGaAs VNW MOSFET







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Zhao, IEDM 2017

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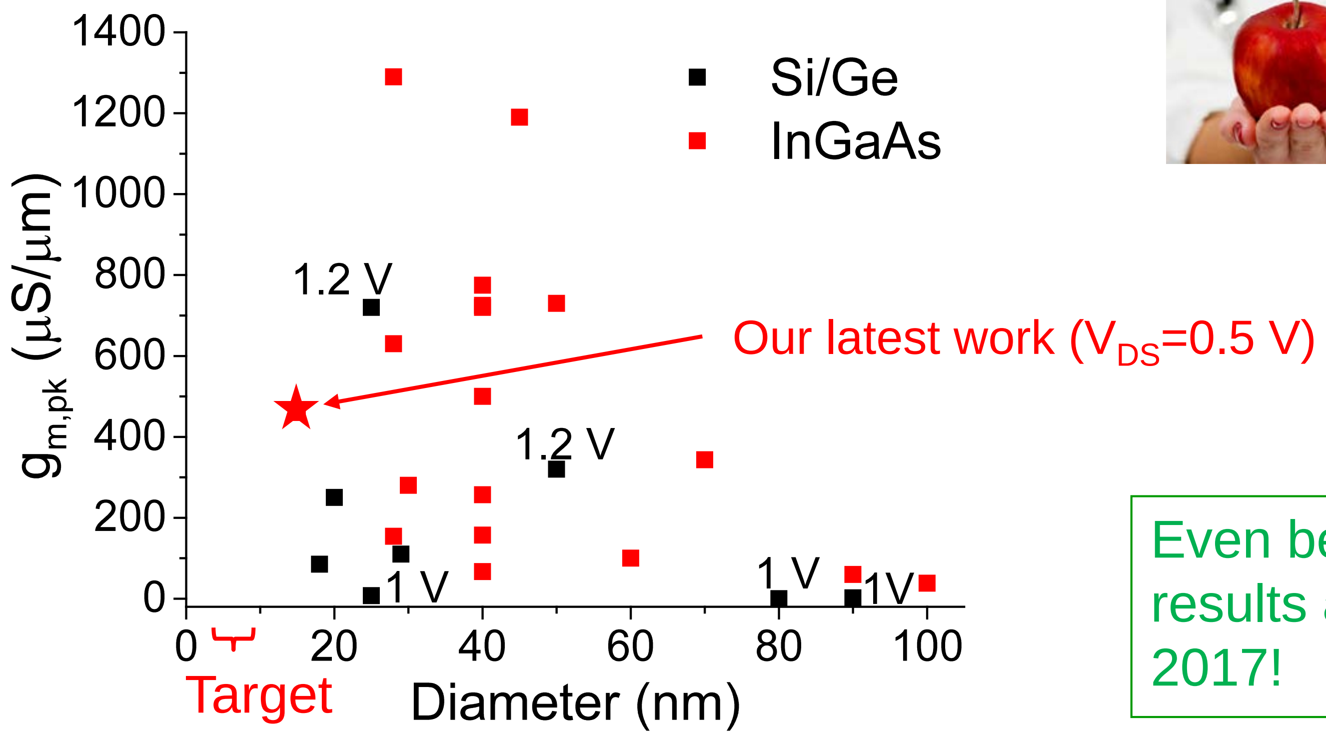
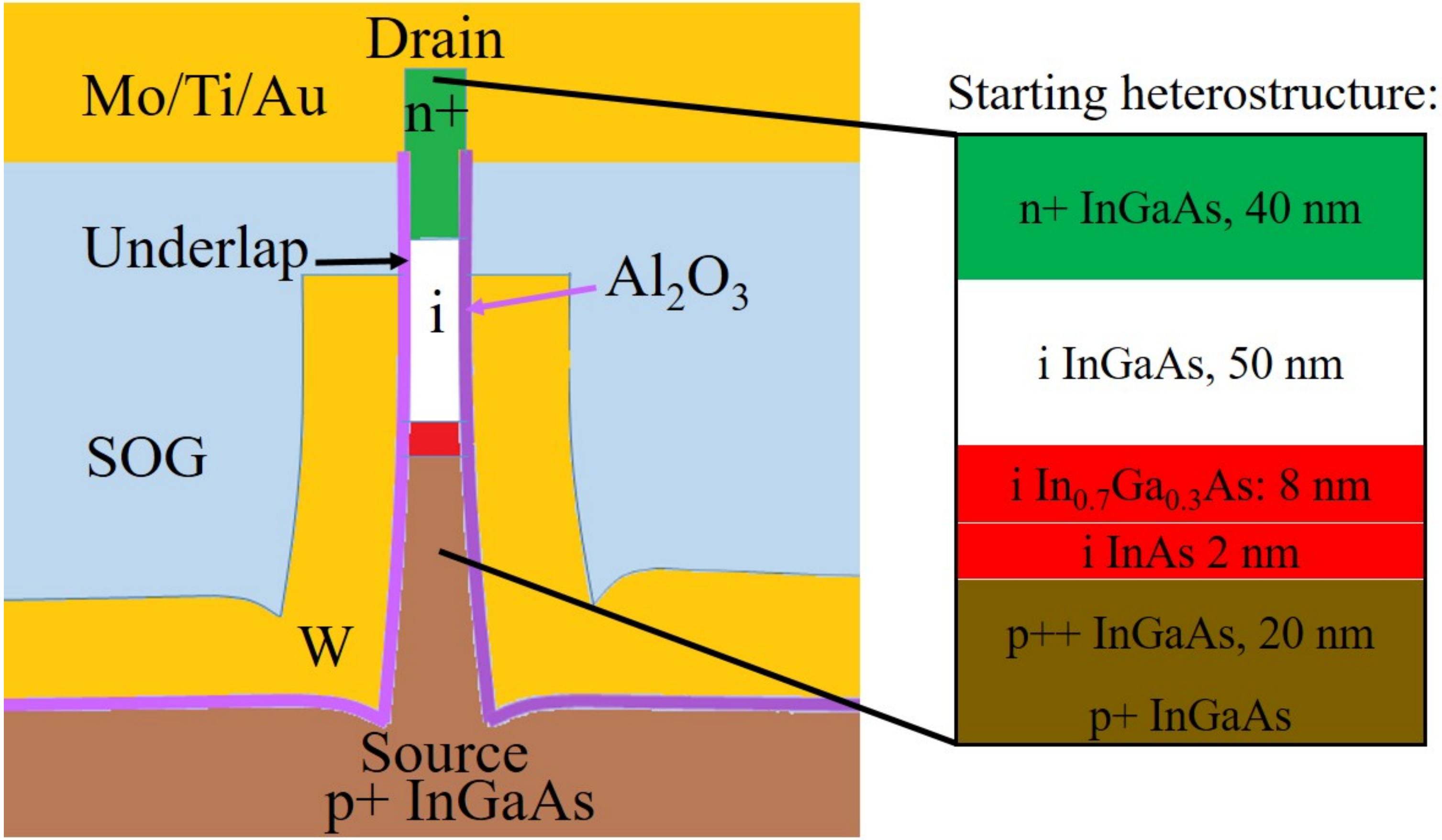


Even better results at IEDM 2017!

Most aggressively scaled VNW MOSFET ever

InGaAs/InAs heterojunction VNW TFETs @ MIT

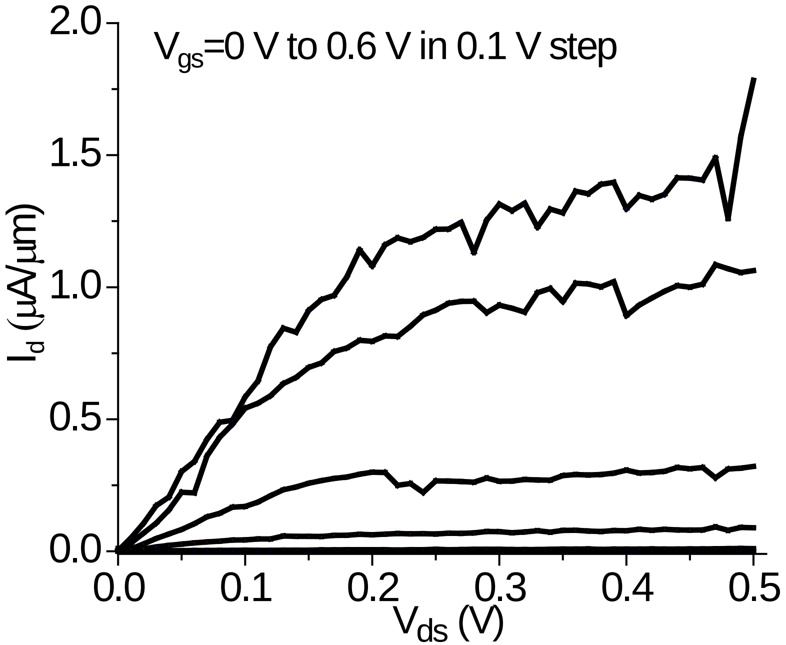


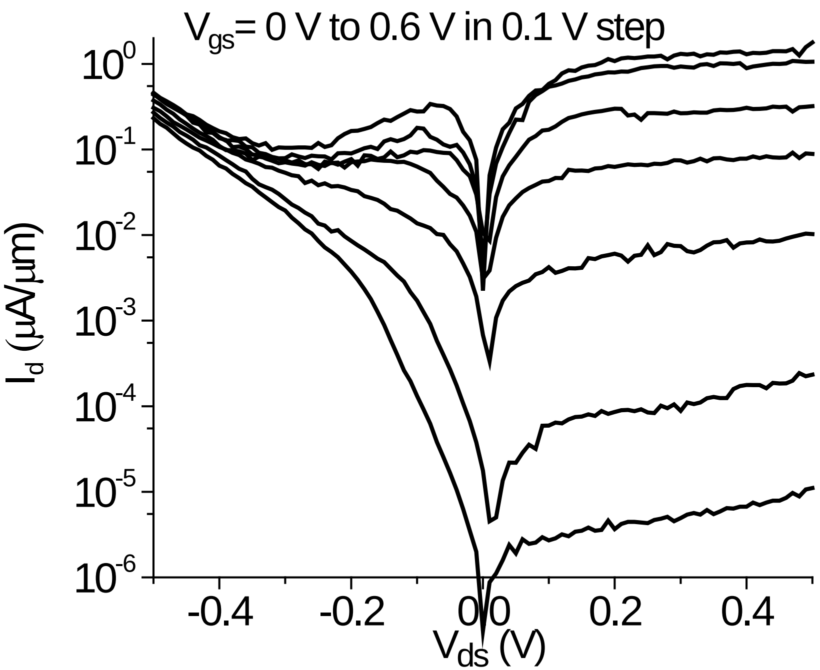
Top-down approach: flexible and manufacturable

Gen-2 InGaAs VNW-TFET

Single NW: D= 40 nm, L_{ch}= 60 nm, 3 nm Al_2O_3 (EOT = 1.5 nm)

New step: final RTA→ 10 fold reduction in D_{it}

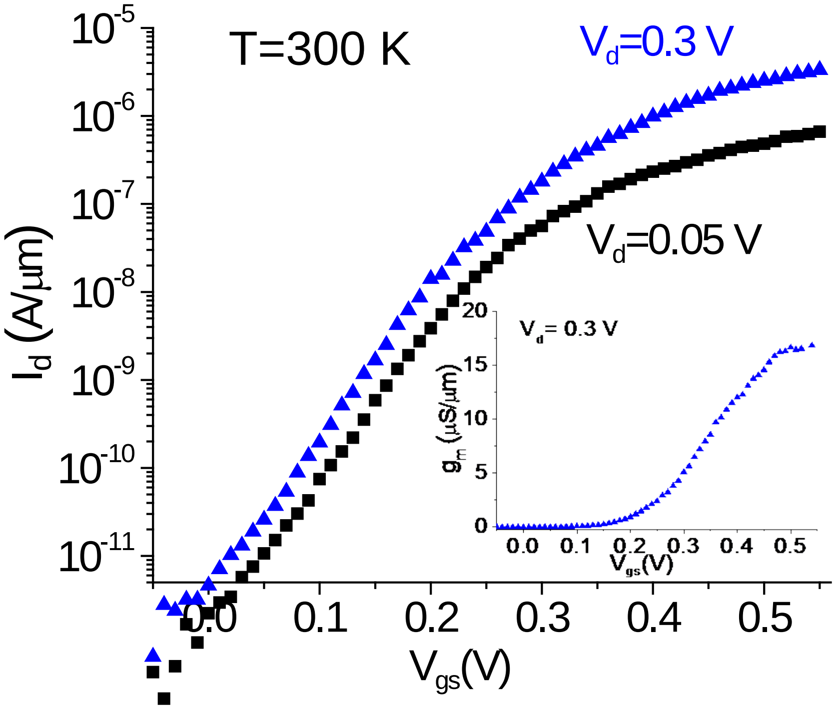


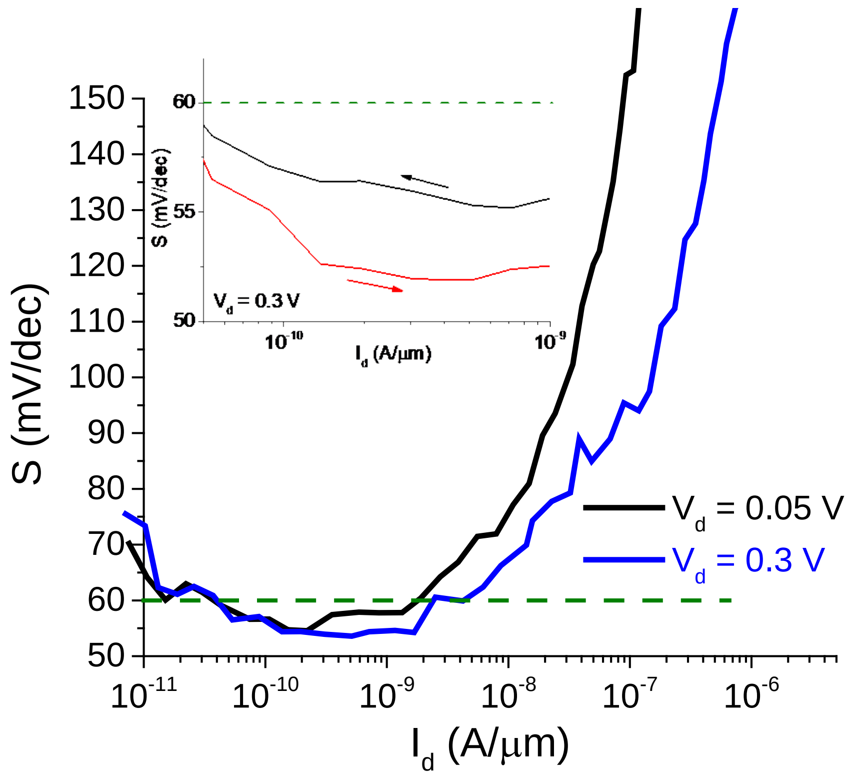


- Saturated output characteristics
- Clear negative differential resistance
- Peak to valley ratio of 3.4 @ V_{gs} = 0.6 V

Zhao, EDL 2017

NW-TFET subthreshold characteristics

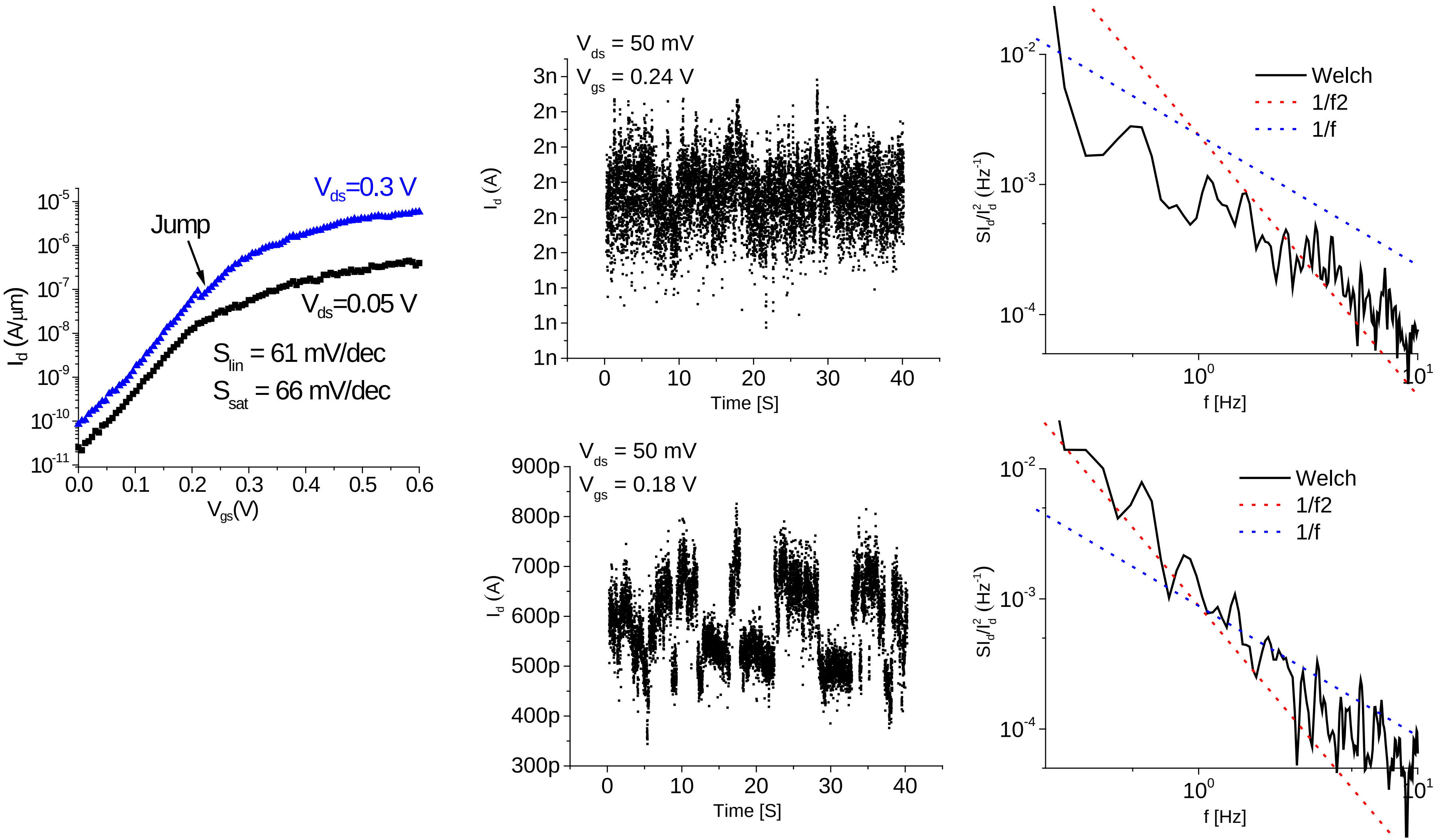




- Sub-thermal for 2 orders of magnitude of current
  - S_{lin} = 55 mV/dec
  - S_{sat} = 53 mV/dec

Zhao, EDL 2017

Random Telegraph noise (RTN) in TFETs



- RTN consistent with jump in subthreshold current
- Single-trap behavior visible

Conclusions

- Improved InGaAs etching technology: sub-10 nm nanowires with very high aspect ratio and high yield
- InGaAs VNW MOSFETs with record characteristics
- InGaAs VNW TFETs with subthermal behavior over 2 orders of magnitude of I_D
- Exciting new results to be presented at IEDM 2017