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5th Berkeley Symposium on Energy Efficient Electronics and Steep Transistor Workshop

Technology breakthrough by ferroelectric HfO_2 for ultralow power logic and memory

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The University of Tokyo

Oct. 19-20 2017, UC Berkeley

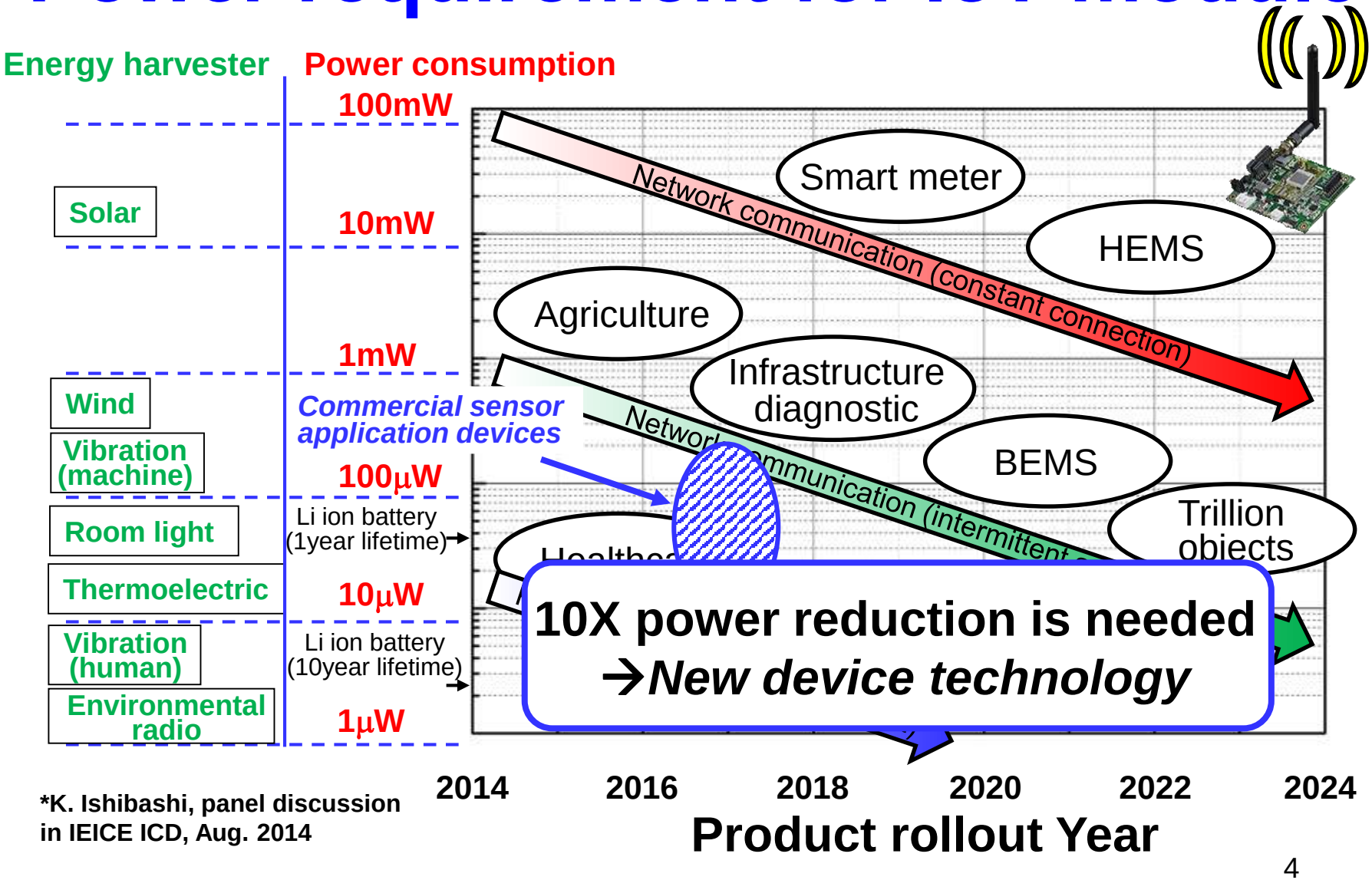
Self-introduction

- **2006 MS. in The University of Tokyo**
  - Room temperature operating silicon single electron transistor
  - Silicon nanowire FET
- **2010 Ph.D in Stanford University**
  - Stress and interface engineering of Ge CMOS
- **2010-2014 IBM Watson Research Center**
  - Beyond 14nm CMOS technology research
    - SiGe, Ge, III-V, UTBSOI, fin, nanowire
  - 14nm SOI technology development
- **2014 Associate prof. in The University of Tokyo**
  - Integrated nanoelectronics for ultralow power application

Outline

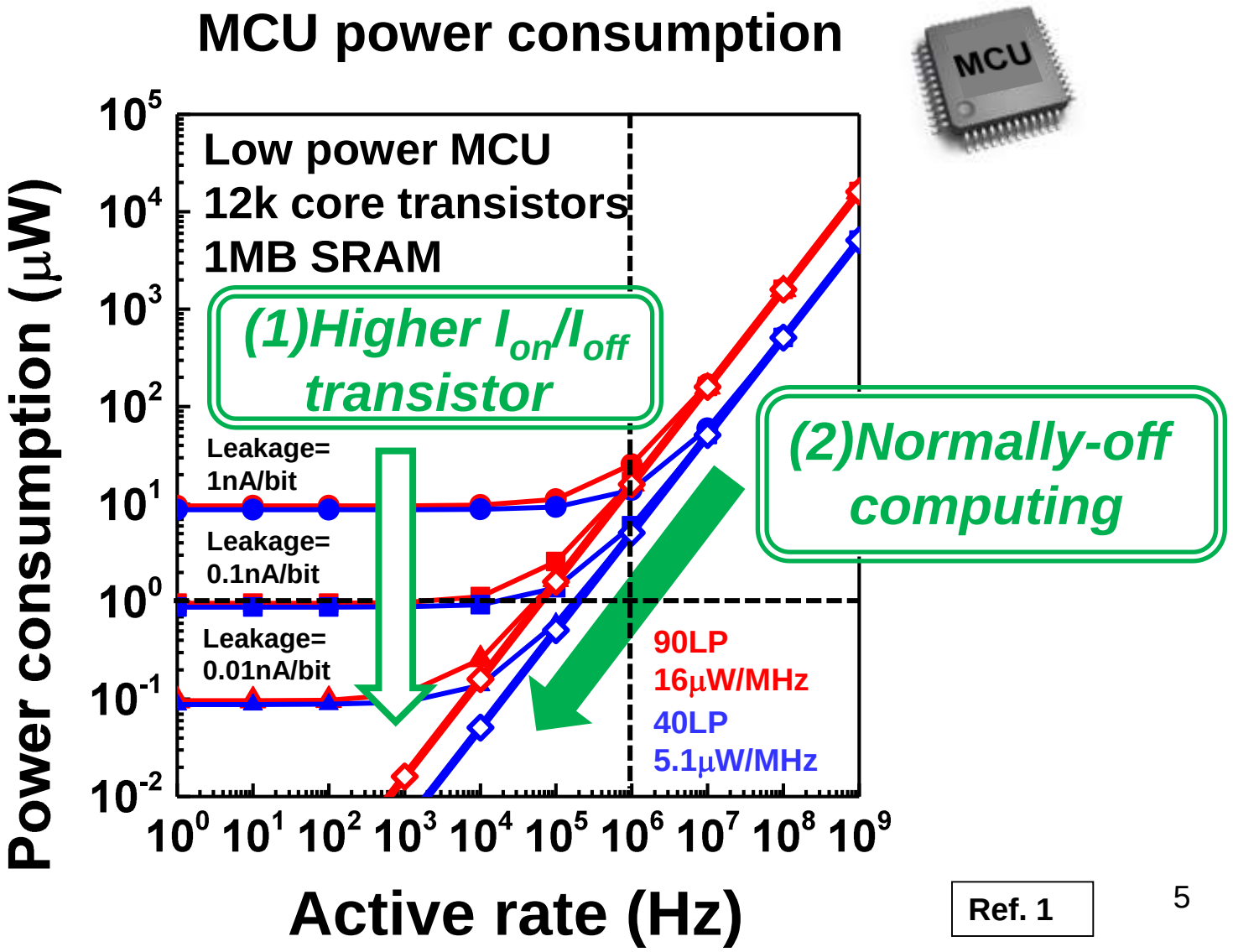
- **Introduction**
  - **Challenges for ultralow power IoT devices**
  - **Breakthrough: Ferroelectric HfO_2**
- **Logic application**
  - **Negative capacitance FET**
- **Memory application**
  - **Nonvolatile SRAM for normally-off computing**
- **Summary**

Power requirement for IoT module



*K. Ishibashi, panel discussion in IEICE ICD, Aug. 2014

Power requirement for MCU



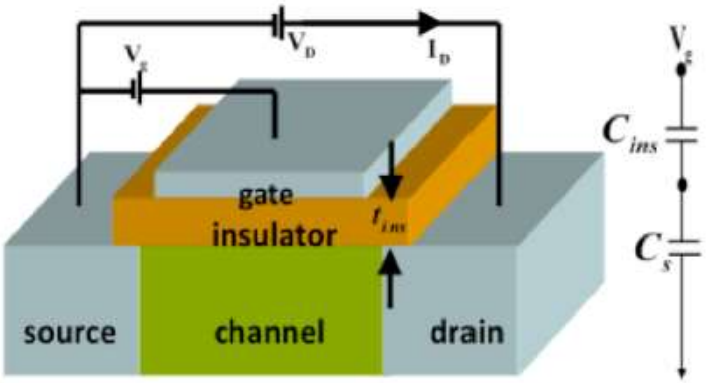
Ref. 1

(1) High I_{on}/I_{off} transistor: Negative Capacitance FET (NCFET)

S. Salahuddin, et al., Nano Lett. 2008

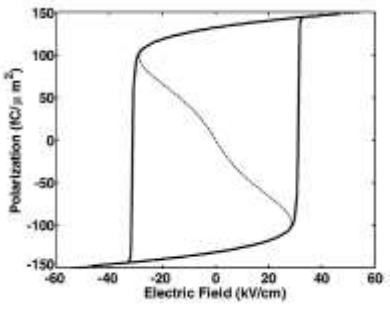
- **Subthreshold slope:**

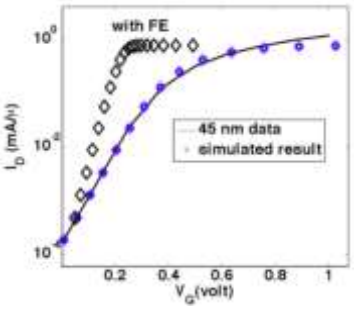
$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_{gs}} \right)^{-1} \approx 2.3 \frac{k_B T}{q} \cdot m = 60 \cdot \left(1 + \frac{C_s}{C_{ox}} \right)$$



- **Condition for SS<60mV/dec:**

$$S < 60 \rightarrow 0 < 1 + \frac{C_s}{C_{ox}} < 1 \rightarrow C_{ox} < 0, \quad |C_{ox}| > C_s$$

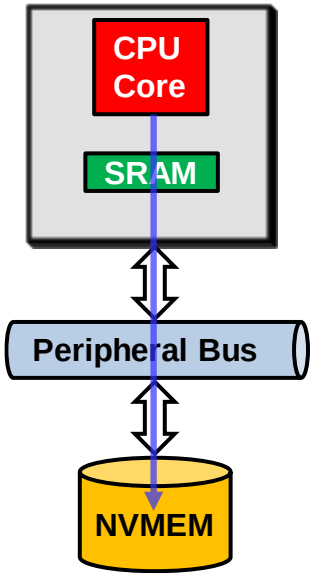
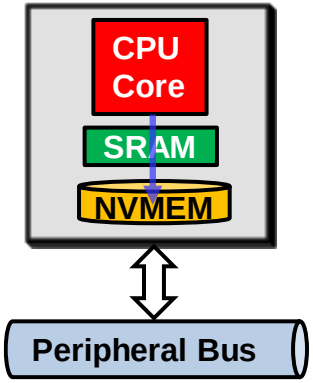
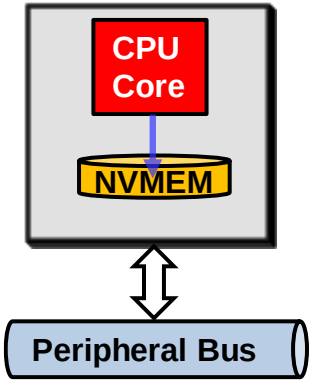
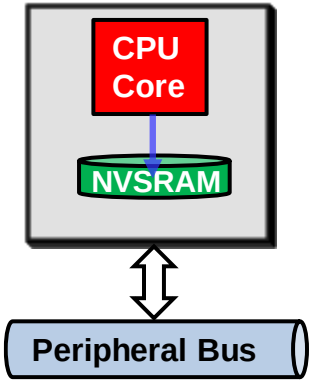




◎Negative capacitance is required.
→Ferroelectric gate insulator

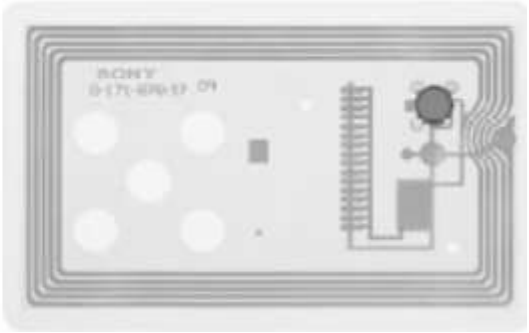
Ref. 2, 5-10

(2) Normally-off computing: Nonvolatile SRAM (NVSRAM)

Reference architecture: ARM Cortex-M0 64kB SRAM 256kB EEPROM				
Capacity	Large	Medium	Medium	**Small**
Backup/recovery	Slow	Medium	Medium	**Fast**
Power	Large	Medium	Medium	**Small**
Process cost	small	Medium/High	Medium/High	**?**

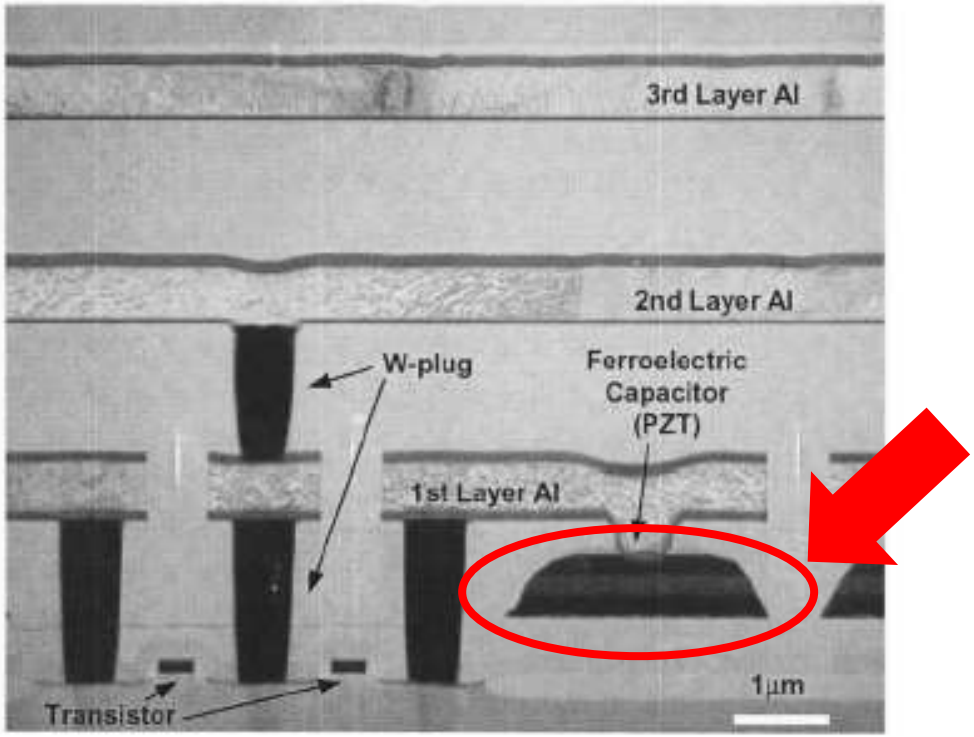
◎NVSRAM can be a promising solution for low power IoT.

→Low voltage operating ferroelectric-based NVSRAM



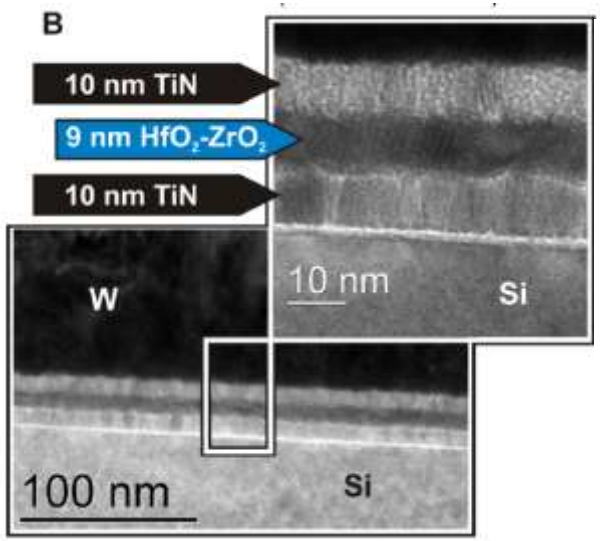
https://www.sony.co.jp/Products/felica/

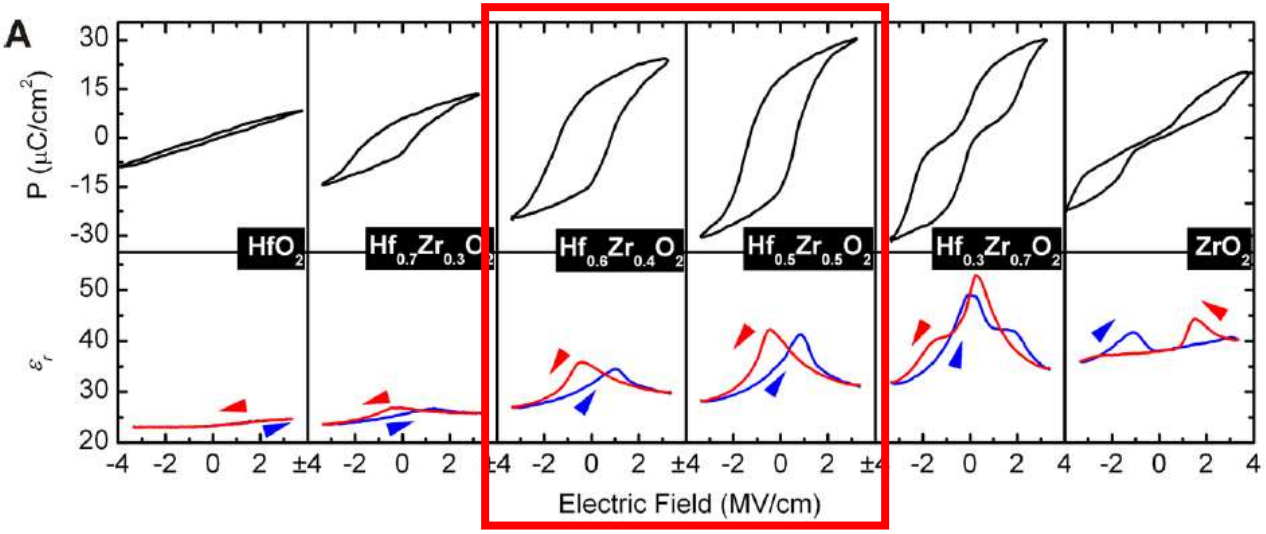
http://pr.fujitsu.com/jp/news/2001/08/2.html



Material breakthrough: FE-HfO_2

J. Müller et al., "Ferroelectricity in Simple Binary ZrO_2 and HfO_2", Nano Lett.,12, 4318 (2012)





- Discovery of ferroelectricity in sub-10nm HfO_2 thin film →CMOS compatible material and it is scalable.
- FE-HfO_2 opens new paths for ultralow power IoT.

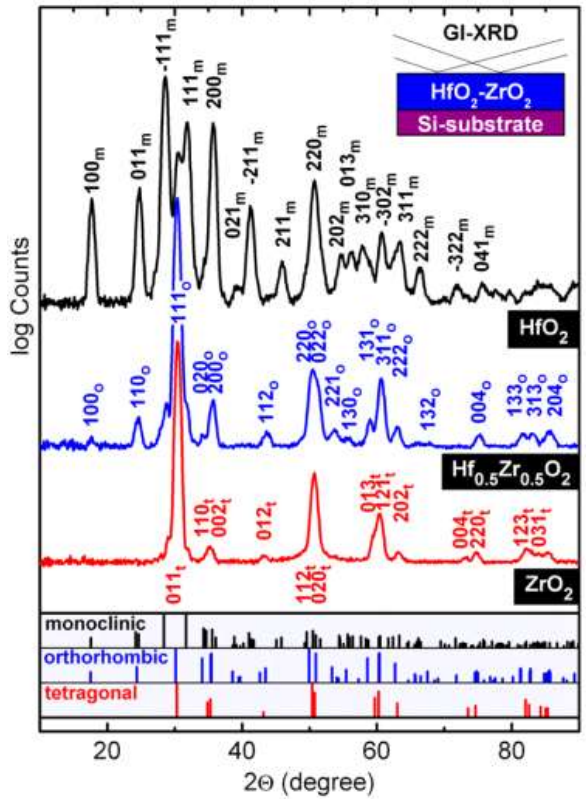
Ref. 4

Origin of ferroelectricity in HfO_2

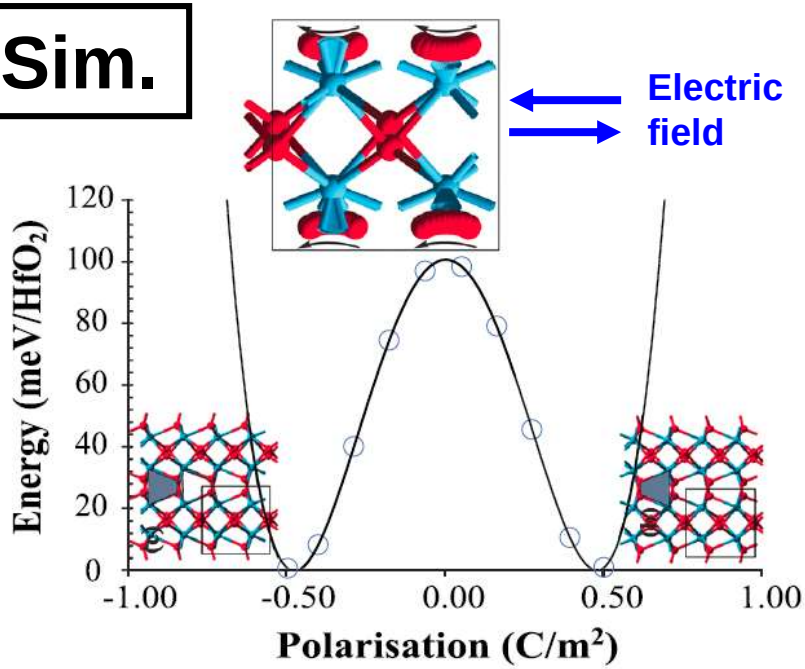
J. Müller et al., Nano Lett. 12, 4318 (2012)

S. Clima et al., APL 104 092906 (2014)

Exp.



Sim.



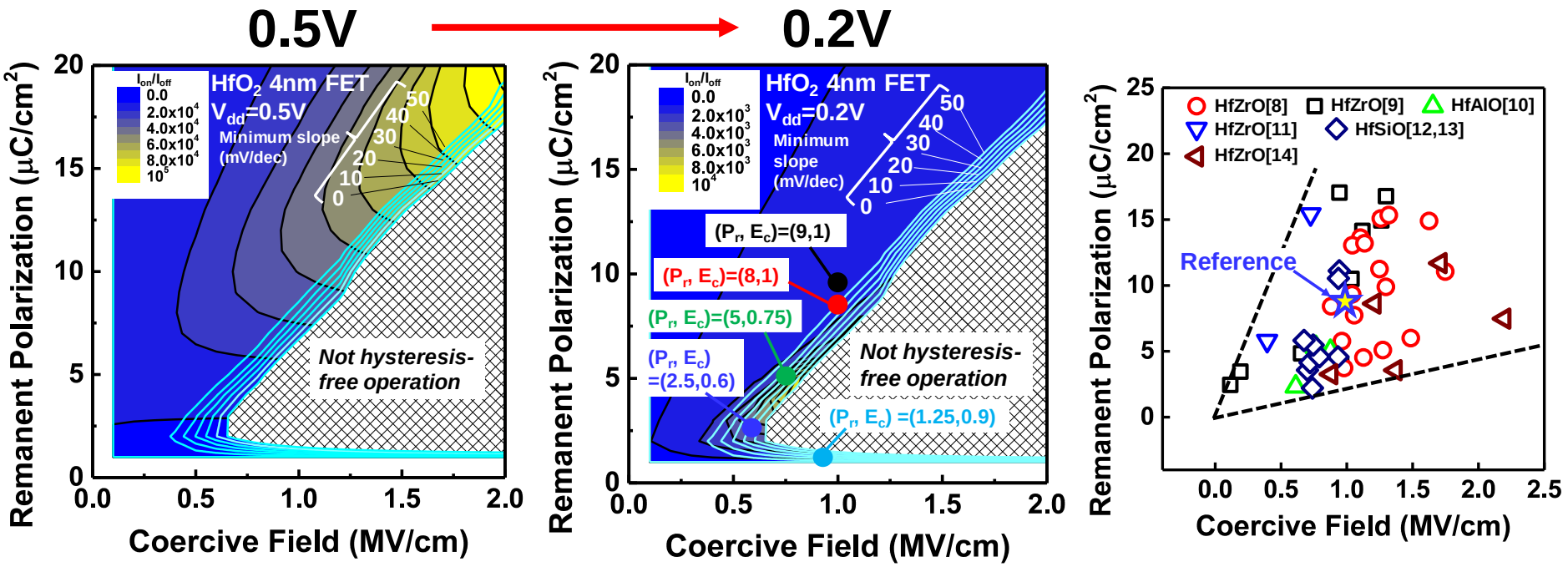
- **Orthorhombic phase appears by doping metal element. Oxygen ions are responsible for polarization.**

Logic applications of FE-HfO_2

Ultralow voltage NCFET design

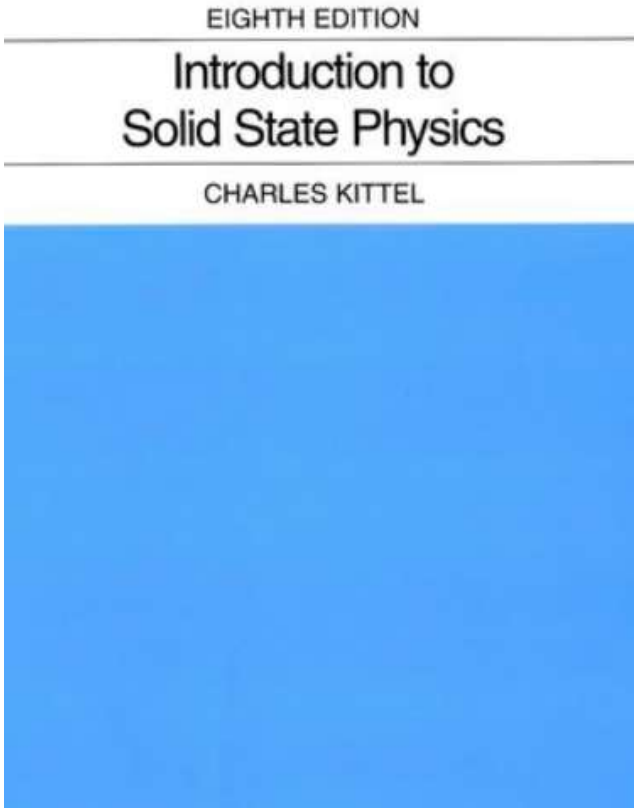
M. Kobayashi et al., AIP advances 2016

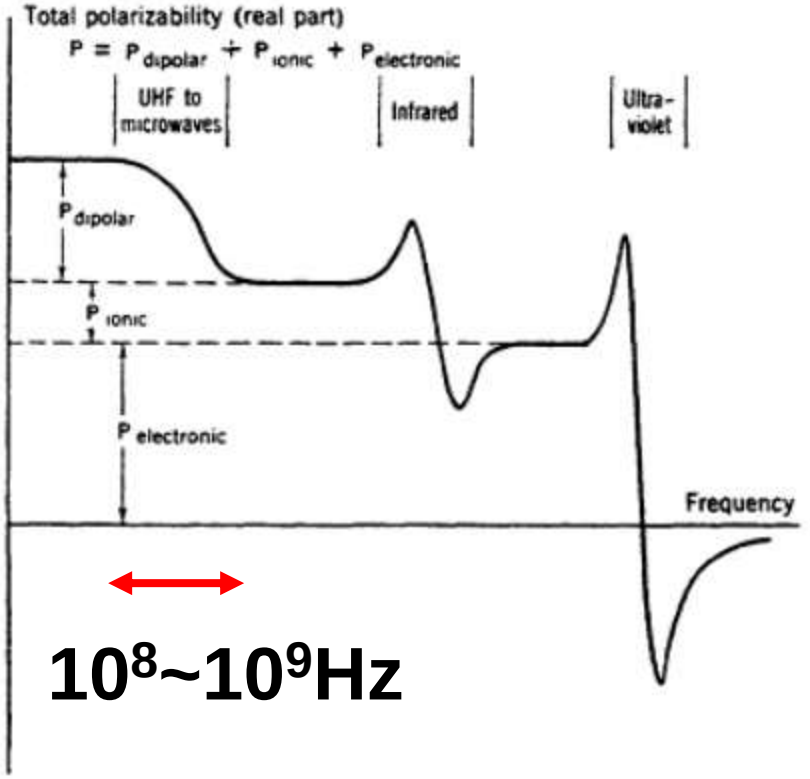
○ Planer FET: Na=1e18cm^{-3}, 4nm HfO_2, targeting 0.2V operation



Design window exists at 0.2V, and material choice is there for FE-HfO_2.

Ref. 10


EIGHTH EDITION
Introduction to
Solid State Physics
CHARLES KITTEL

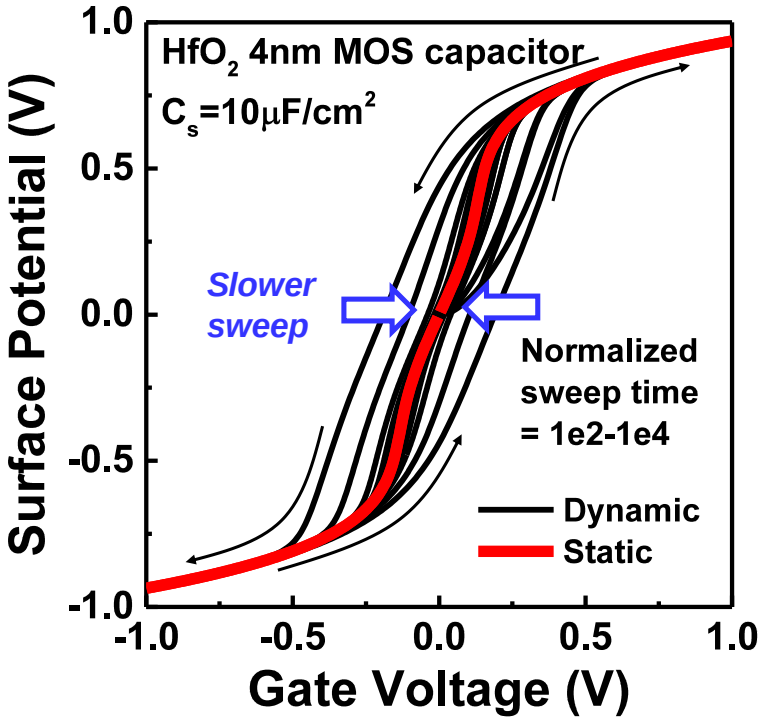

Total polarizability (real part)
P = P dipolar + P ionic + P electronic
UHF to microwaves
Infrared
Ultra-violet
P dipolar
P ionic
P electronic
Frequency

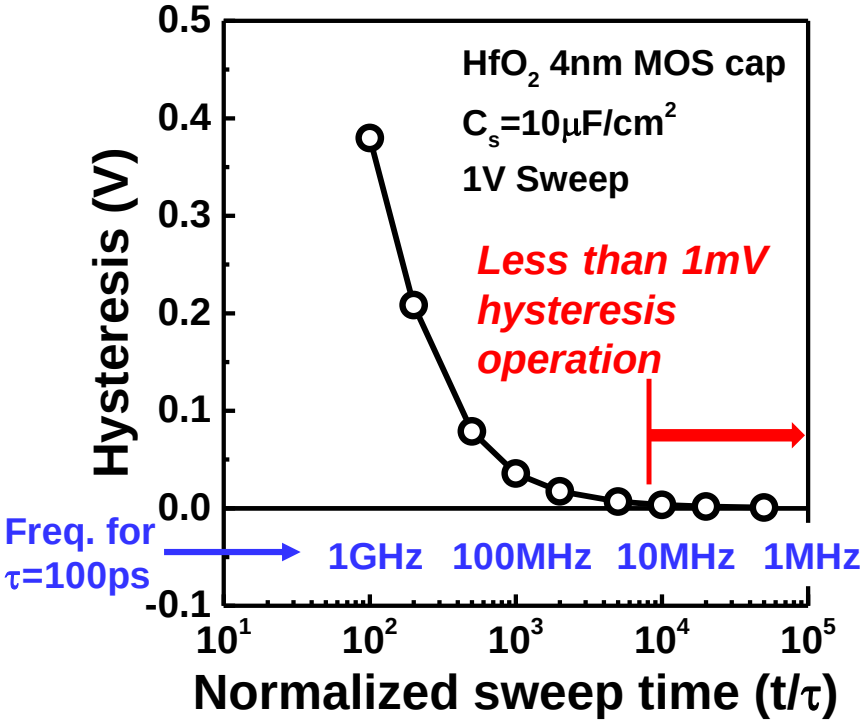
10^8~10^9Hz

Operation speed of NCFET

M. Kobayashi et al., AIP advances 2016

○ Planer FET: Na=1e18cm^{-3}, 4nm HfO_2, targeting 0.2V operation





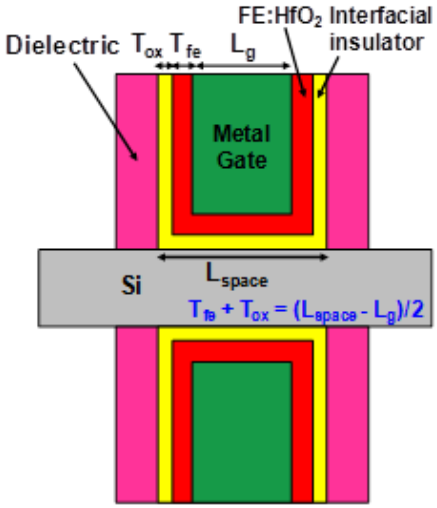
Suppose ~100ps time constant, NCFET can operate at >10MHz without hysteresis.

Ref. 10

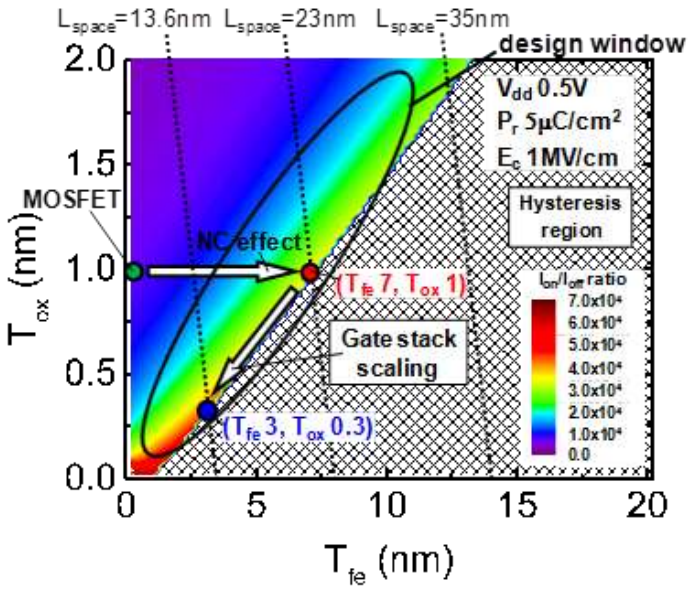
Scalability of NCFET

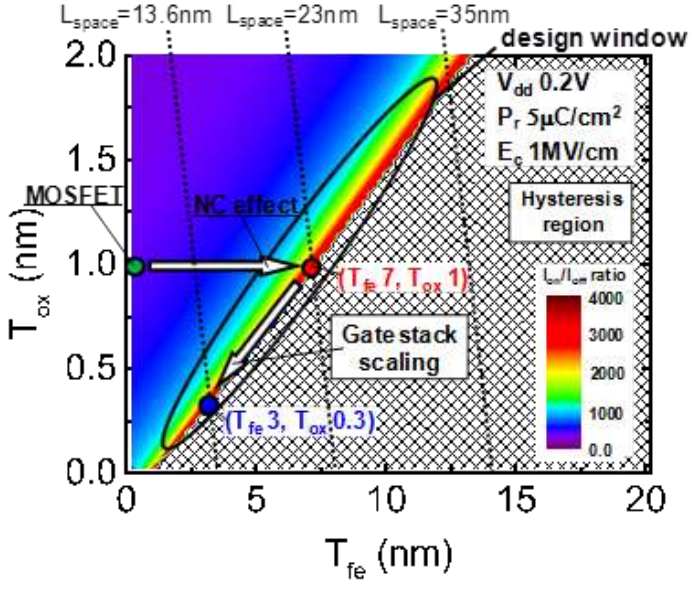
K. Jang et al., Silicon Nano Workshop 2016

○ Fin FET: high aspect ratio/double gate, Na=1e15cm^{-3}, targeting 0.2V



0.5V → 0.2V





Very thin FE-HfO_2 gate stack can fit in advanced gate last process, with steep slope.

Ref. 8

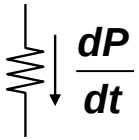
Transient modeling of NCFET

M. Kobayashi et al., IEDM 2016

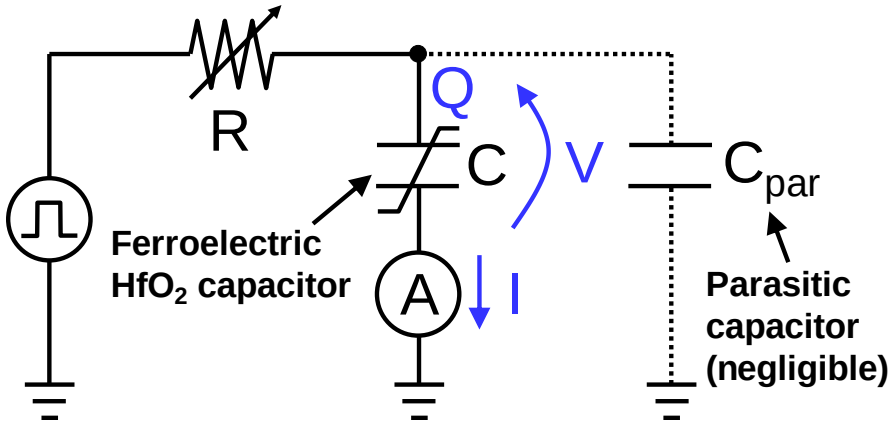
Landau-Khalatnikov equation

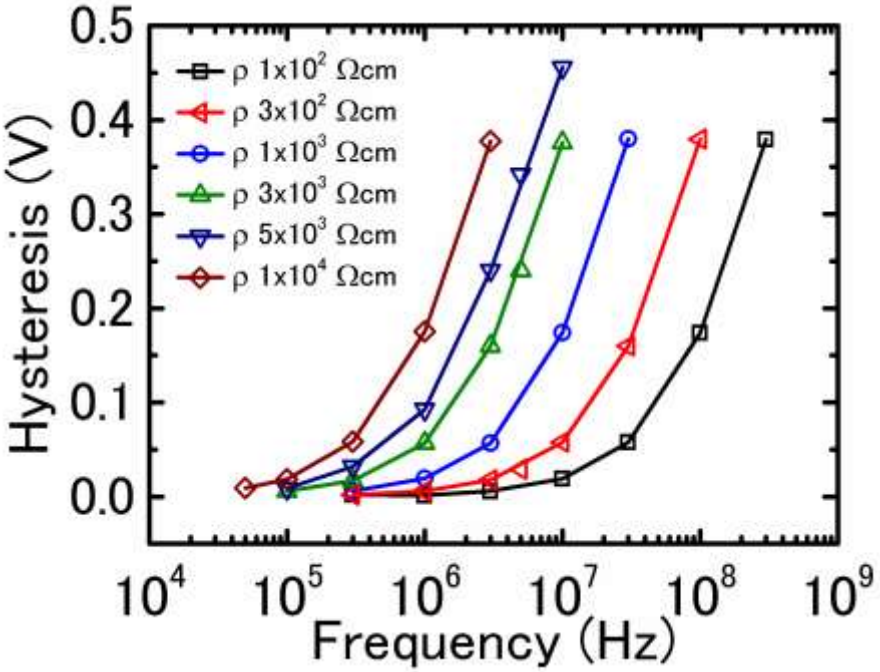
Dynamic term

$$\rho\frac{dP}{dt} = -\frac{dU}{dP}$$

ρ  $\frac{dP}{dt}$

$$U(P,E) = \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 - E\cdot P$$





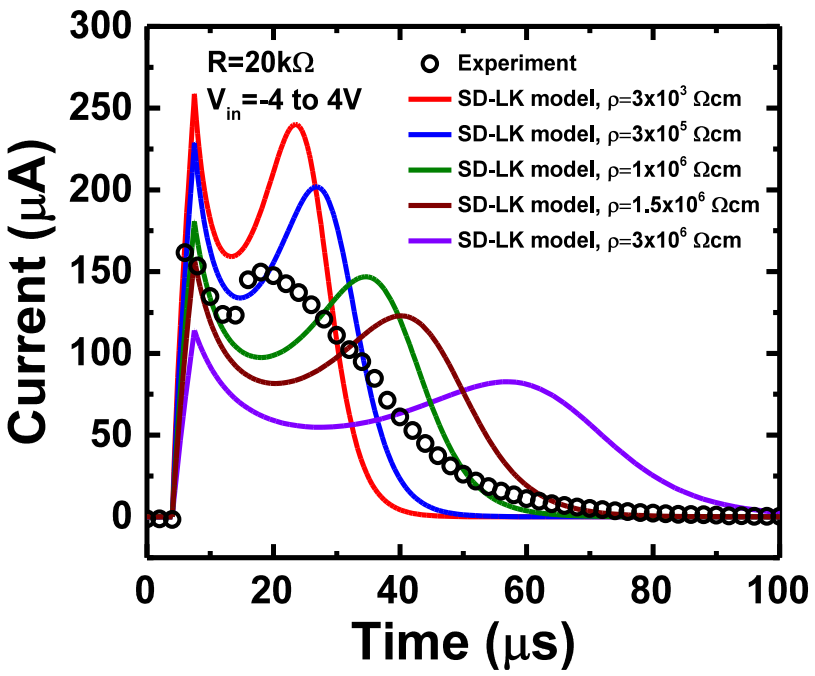
Ref. 6,12

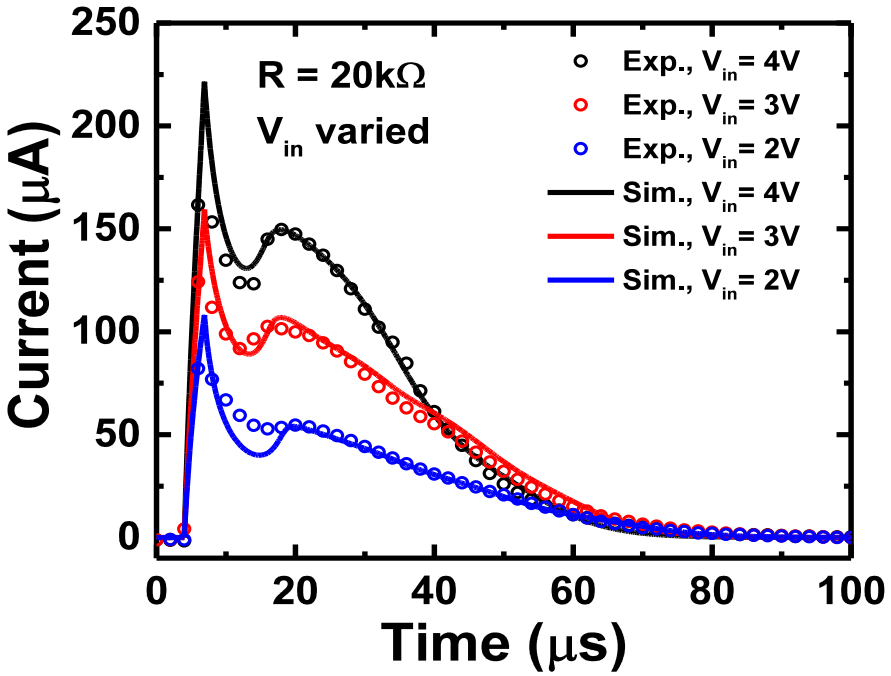
Extracted ρ from transient characteristics, NCFET can operate at > 10MHZ with FE-HFO_2.

Transient modeling of NCFET

K. Jang et al., Silicon Nano Workshop 2017

Single domain → **Multiple domain**

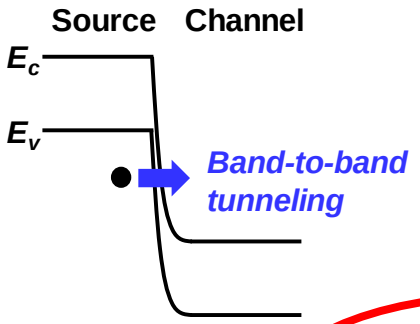




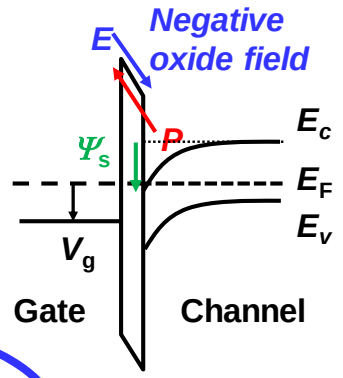
Multiple domain model improved fitting accuracy to experimental data.

Toward super steep slope FET

Transport term **Voltage divider term**



$$SS = 2.3\frac{k_B T}{q}\left(1+\frac{C_d}{C_{ins}}\right)$$



TFET

- Low on-current
- Limited range of steep slope @low I_d
- Process complexity
- Asymmetric layout

Ref. 13,14

NCFET

- High on-current
- Simple process
- Symmetric layout
- Limited range of steep slope @high Q_s

Ref. 2,5-10

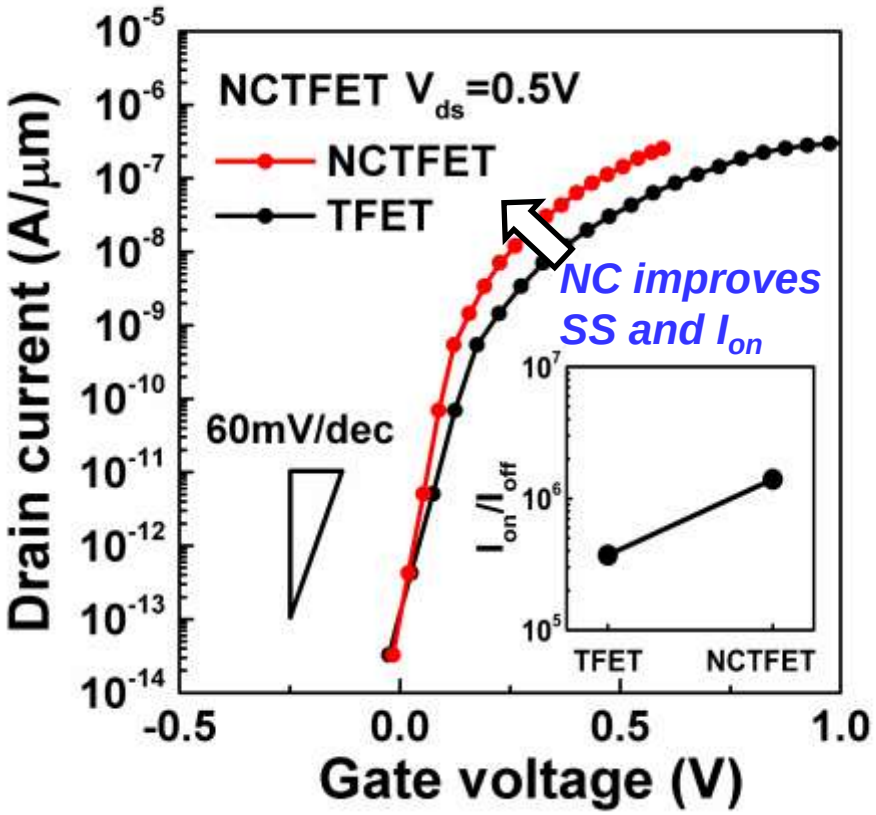
Super Steep Transistor

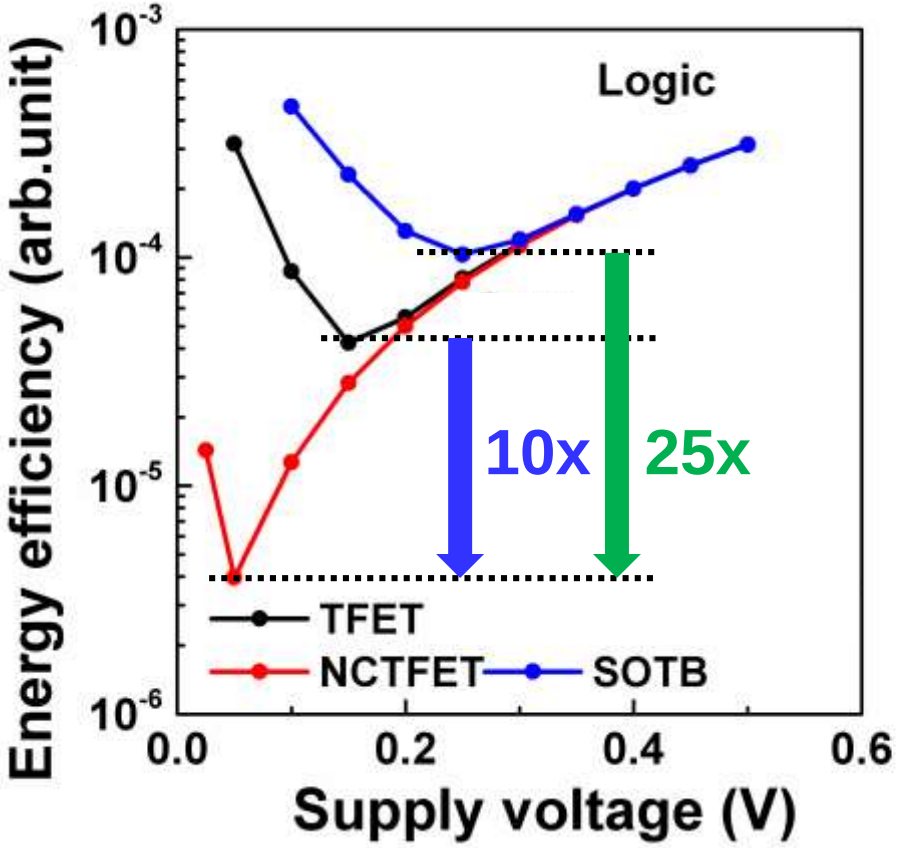
Ref. 15-17

High on-current, wide range of steep slope → high I_{on}/I_{off} at lower V_{dd}

Negative capacitance TFET

M. Kobayashi et al., IEEE trans. Nanotechnology, 2017



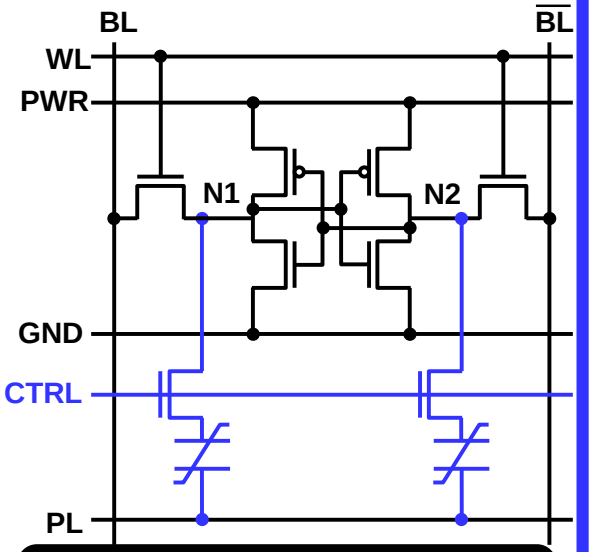
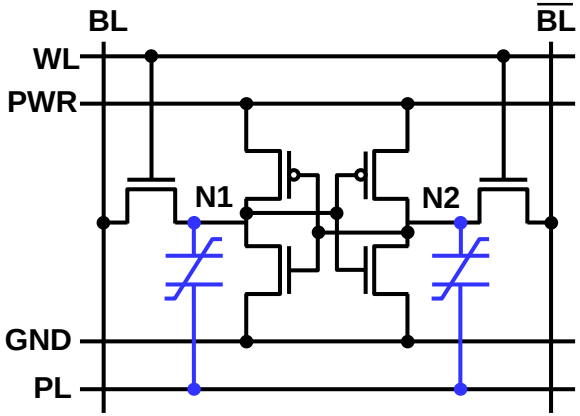
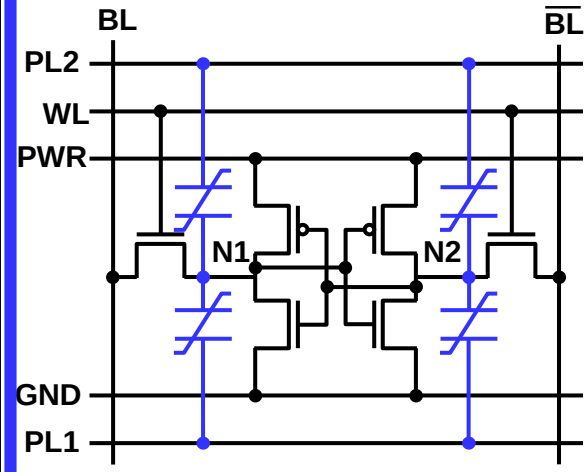


Negative capacitance can boost I_{on}/I_{off} of TFET and improve energy-efficiency by 10X.

Ref. 17

Memory applications of FE-HfO_2

NVSRAM with ferroelectric cap.

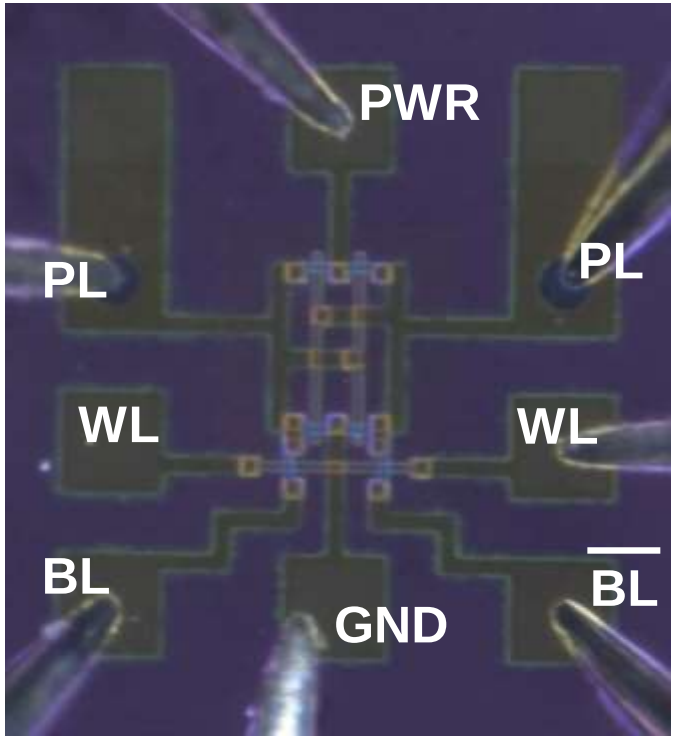
Shadow RAM S.S.Eaton et al., ISSCC 1988 p.130	2-cell NVSRAM T. Miwa et al., VLSI Symp. 2001 p.129	4-cell NVSRAM S. Masui et al., JSSC 38 5 715 (2003)
		
△8Trs are needed	○ Simple operation ○ Simple integration ○ Moderate margin	○ Wide margin △ 4 Cells are needed △ 2 PLs are needed

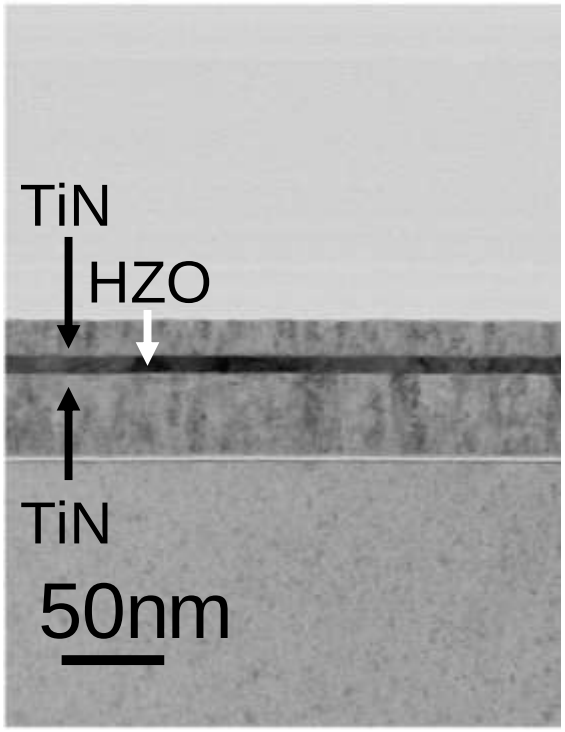
Nonvolatility can be given to SRAM by backend ferroelectric capacitor.

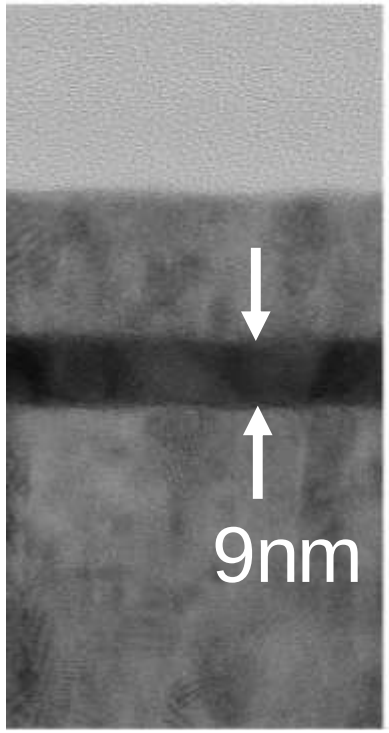
Ref. 3,18,19

NVSRAM with FE-HfO_2 cap.

M. Kobayashi et al., VLSI symposium, 2017





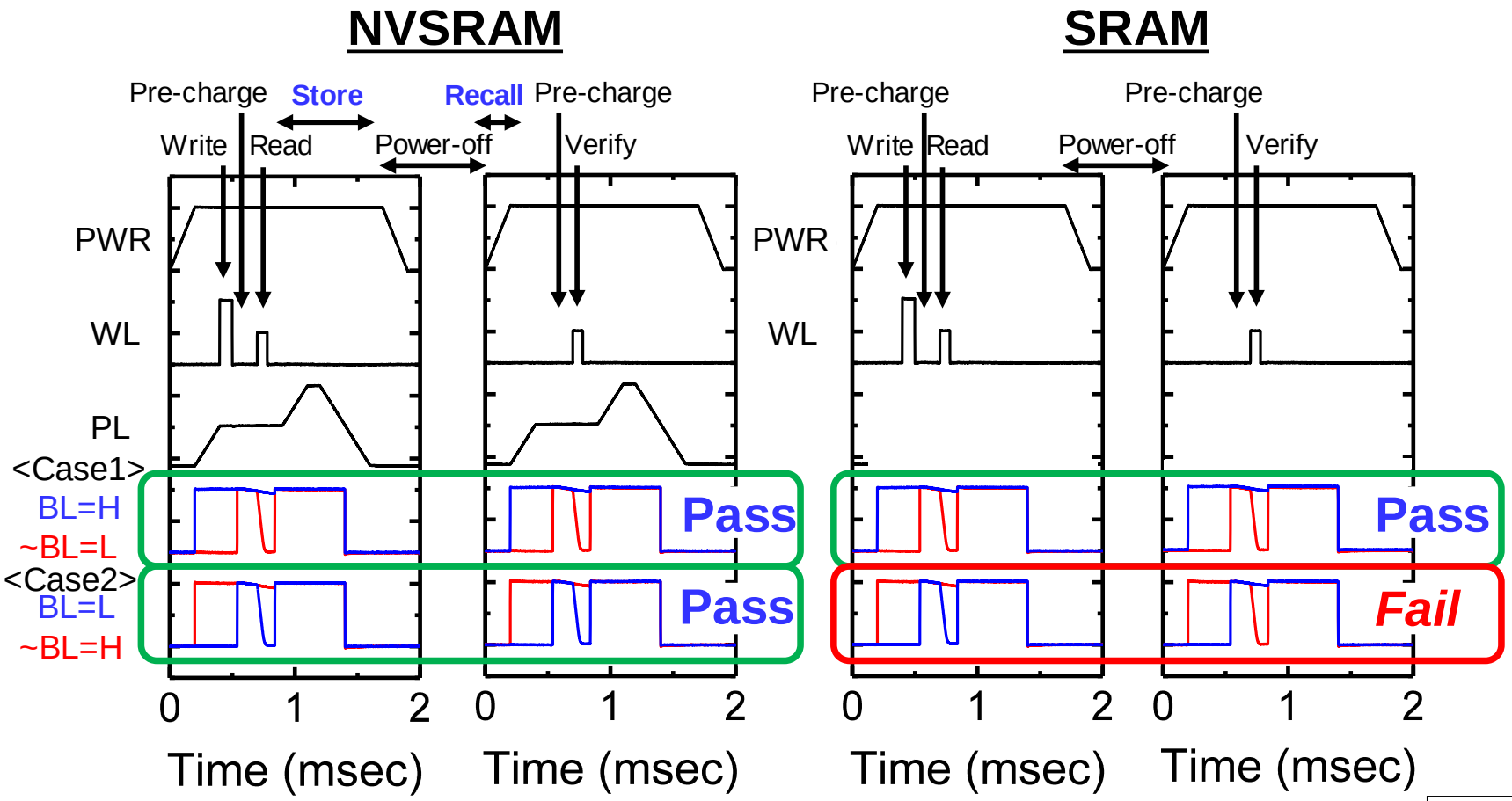


Prototype NVSRAM was fabricated in university's lab integrating FE-HfO_2 on CMOS SRAM

Ref. 20

Store/recall operation demo.

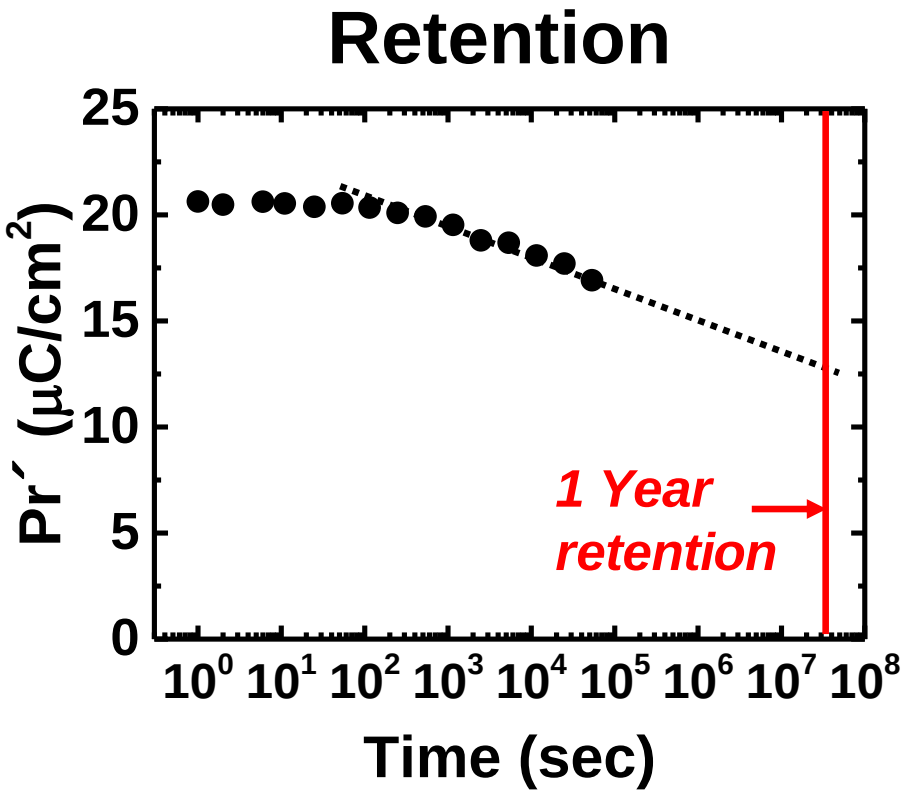
M. Kobayashi et al., VLSI symposium, 2017

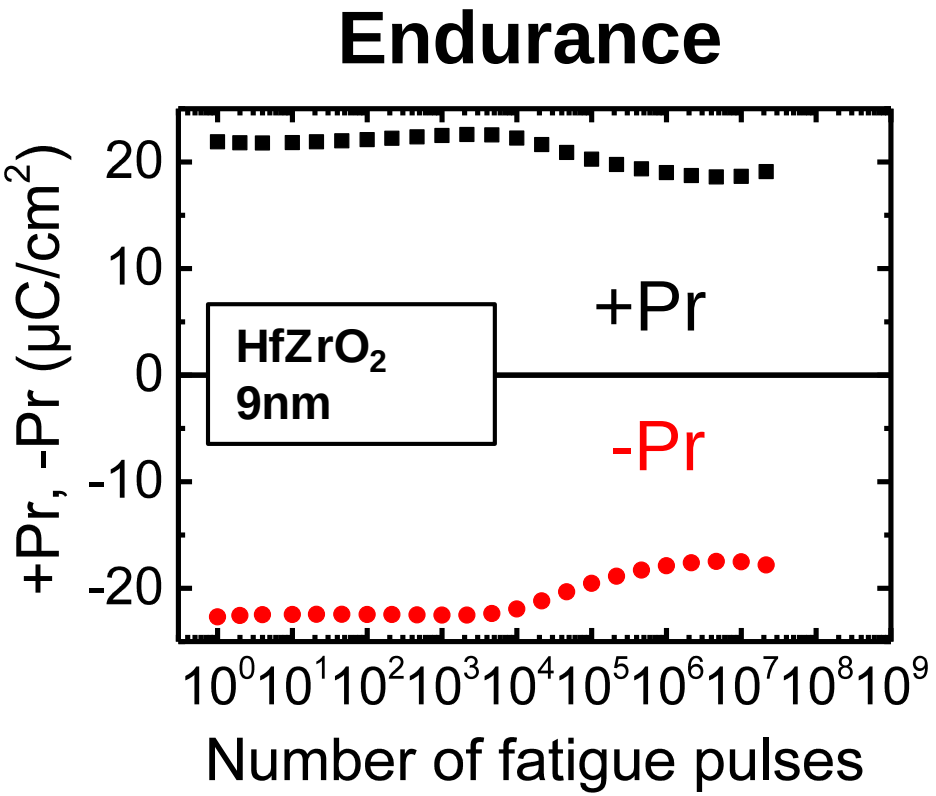


Store/recall operation was demonstrated.

Ref. 20

Retention and endurance of FE-HfO_2 cap.





Need further development for
10 years retention and >10^9 endurance

Summary

- **Device technology challenge for ultralow power IoT application.**
  - **High I_{on}/I_{off} transistor**
  - **Normally-off computing**
- **Ferroelectric HfO_2 can be a break-through for:**
  - **Negative capacitance FET**
  - **Nonvolatile SRAM**

  at low cost.

Acknowledgement

- **Lab members**

Nozomu Ueyama (M)

Kyungmin Jang (D)

Collaboration

Prof. Toshiro Hiramoto

- **Government funding**

PRESTO SAKIGAKE

科研費 KAKENHI

- **Partners**

TEL TOKYO ELECTRON

SCREEN

IBM

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