5th Berkeley Symposium on Energy Efficient Electronics & Steep Transistors Workshop
10:45-11:05, Oct. 19, 2017 @Banatao Auditorium on the 3rd floor of Sutardja Dai Hall at the UC Berkeley campus, San Francisco, CA, USA

Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing for IoT Applications

Takahiro Hanyu[1,2,3]

[Contributors] D. Suzuki[5], M. Natsui[1,2,3], N. Onizawa[5], S. Ikeda[1,3,4], T. Endoh[1,3,6], and H. Ohno[1,3,4]

[1]Center for Spintronics Integrated Systems, Tohoku University, JAPAN
[2]Laboratory for Brainware Systems, RIEC, Tohoku University, JAPAN
[3]Center for Innovative Integrated Electronic Systems (CIES), Tohoku University, JAPAN
[4]Laboratory for Nanoelectronics and Spintronics, RIEC, Tohoku University, JAPAN
[5]Frontier Research Institute for Interdisciplinary Sciences, Tohoku University, JAPAN
[6]Dept. of Electrical Engineering, Tohoku University, JAPAN
http://www.csis.tohoku.ac.jp/

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Outline

- **Background & Motivation**

  ~Nonvolatile Logic-in-Memory Architecture~

- Design of Nonvolatile FPGA
- VLSI CAD Environment
- Conclusions & Future Prospects

Background: IoT/IoE Era

IoT: Internet of Things
IoE: Internet of Everything

Processor	Sensor Interface
Radio	Memory

Power-Constrained SoC

→ Sensors, actuators, Button cells, etc...

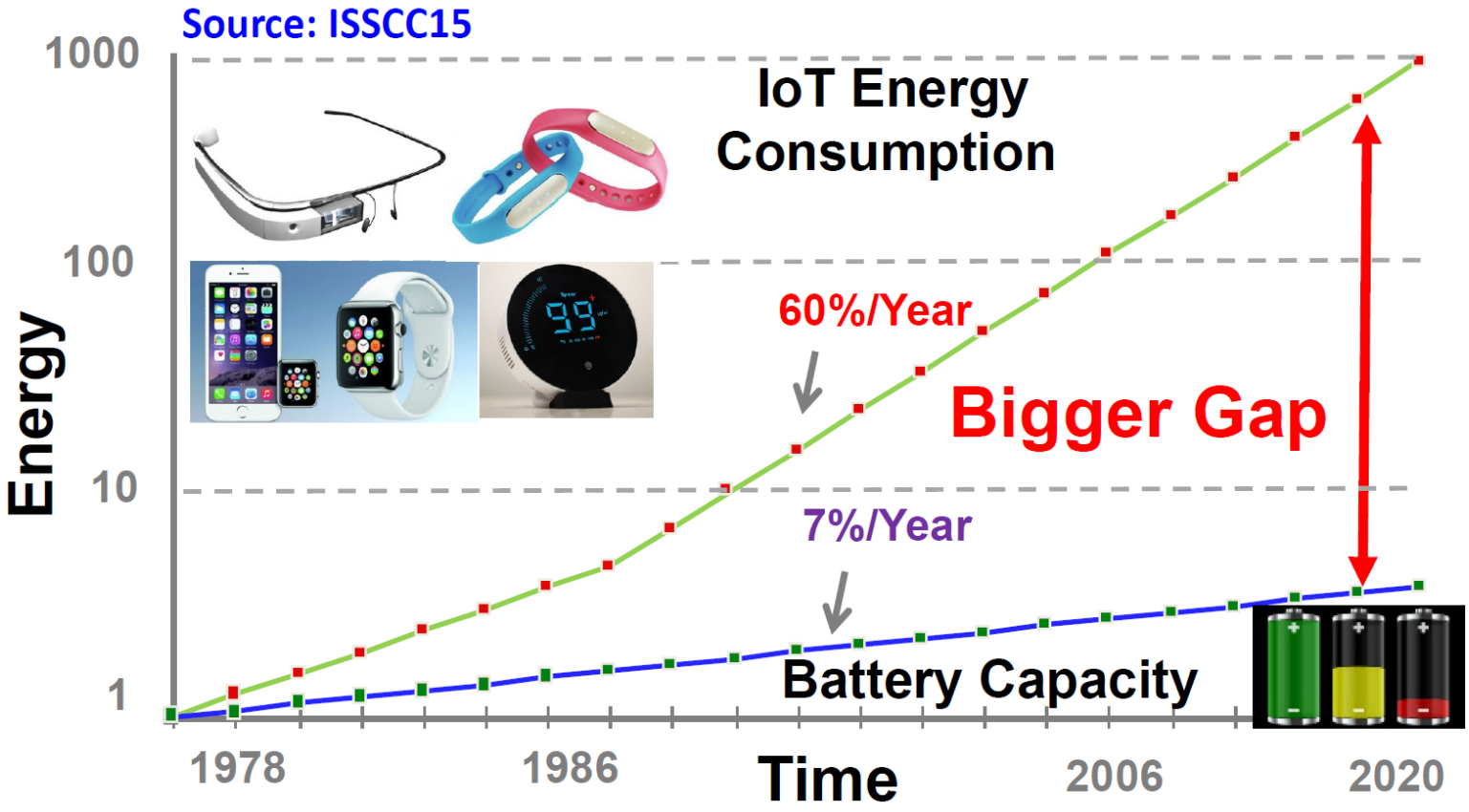
Processor	Sensor Interface
Radio	Memory
Security	Display
Power management	Video

Middle/high-End IoT SoC

→ Automotive, cloud, smartphone, etc...

Require a variety of VLSI Processors under Power-Dissipation Limit

Problem: Energy Gap

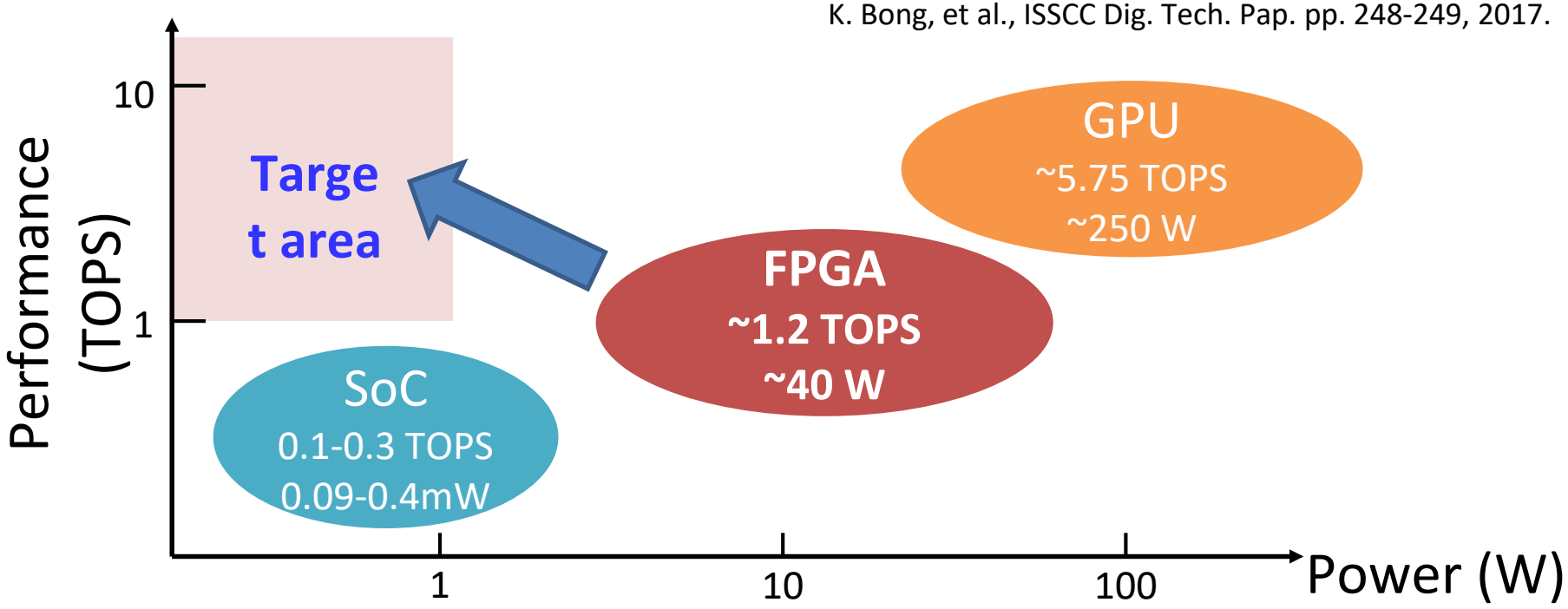


[Ref.] Y. Liu, et al., ISSCC, pp. 84-85, Feb. 2016.

Standby power consumption is a critical issue for IoT applications.

Recent Trends in DNN Hardware

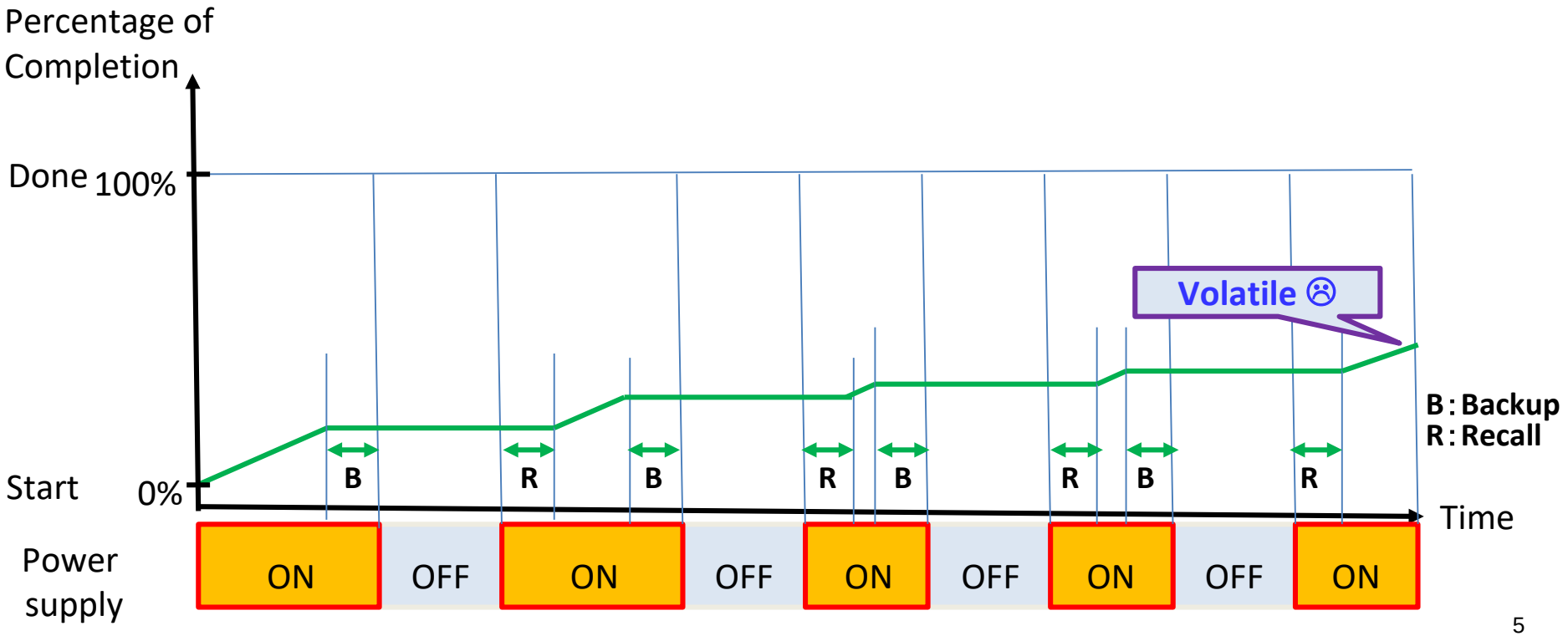
K. Bong, et al., ISSCC Dig. Tech. Pap. pp. 248-249, 2017.



FPGAS is a key device to realize "energy-efficient" hardware.

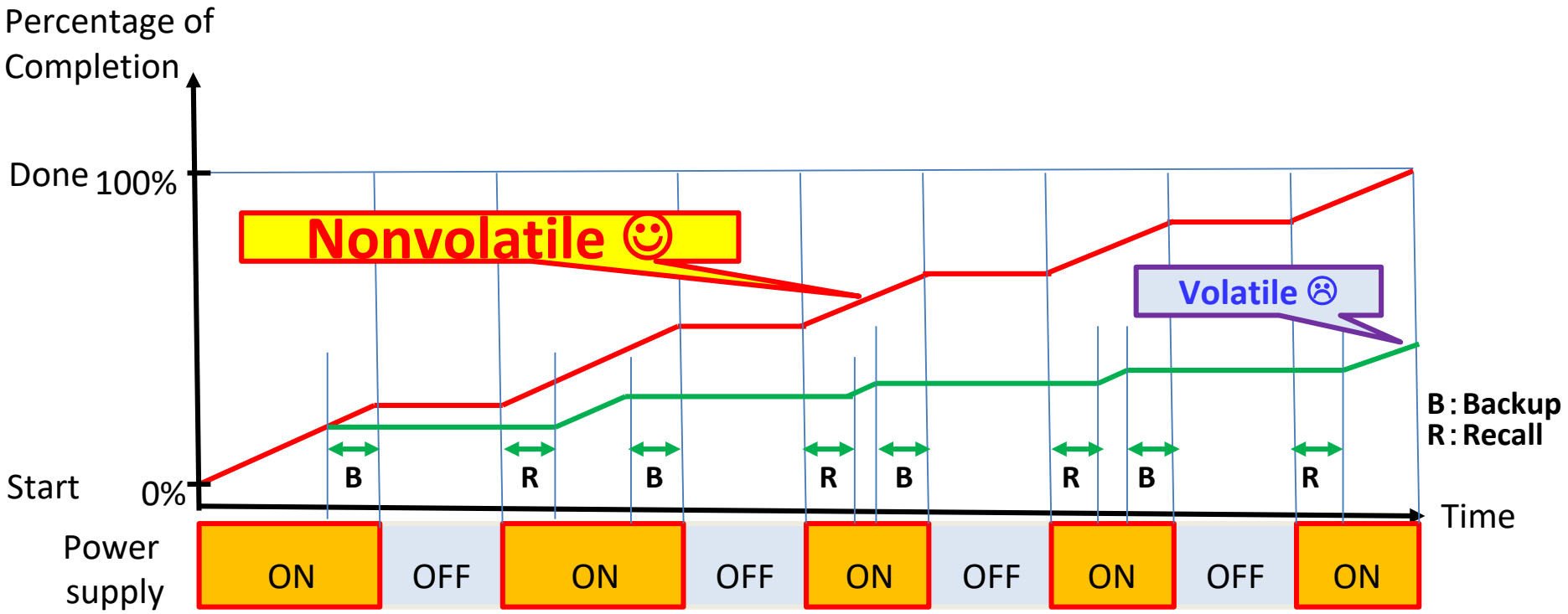
Power-Supply Stability Problem

1) **Power supply is frequently shut down in IoT applications.**
2) Processing overhead is serious in conventional volatile processor, because **data** must be **backup/recall to/from external NVM.**



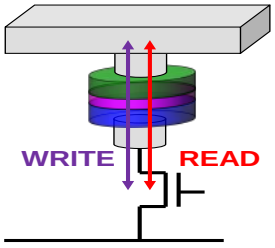
Power-Supply Stability Problem

1) **Power supply is frequently shut down in IoT applications.**
2) Processing overhead is serious in conventional volatile processor, because **data** must be **backup/recall to/from external NVM.**
3) **Immediate** backup/recall are possible in a **nonvolatile** processor.

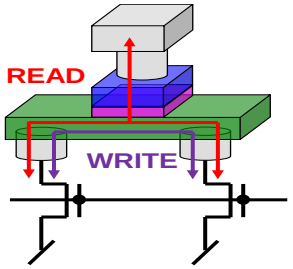


Nonvolatile Memories

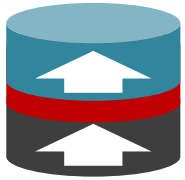
	Flash	FRAM	Spin device
Access speed	Middle	**High**	**High**
Non-destructive read	**Good**	Weak	**Good**
Write endurance	Bad	Weak	**Good**
Scalability	**Good**	Weak	**Good**
Operation voltage	Bad	Weak	**Good**



2-Terminal

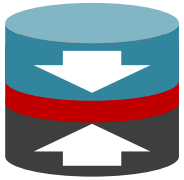


3-Terminal



Low resistance

"0"

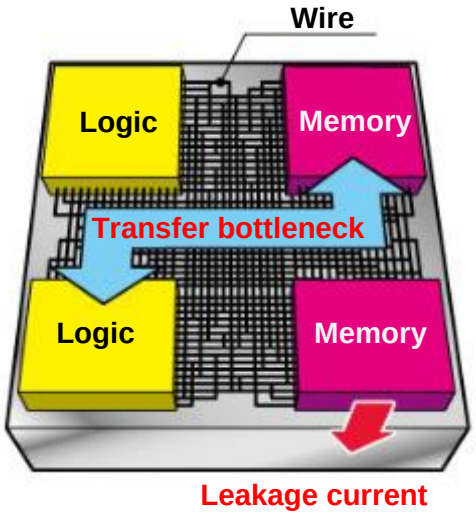


High resistance

"1"

What is a Nonvolatile VLSI?

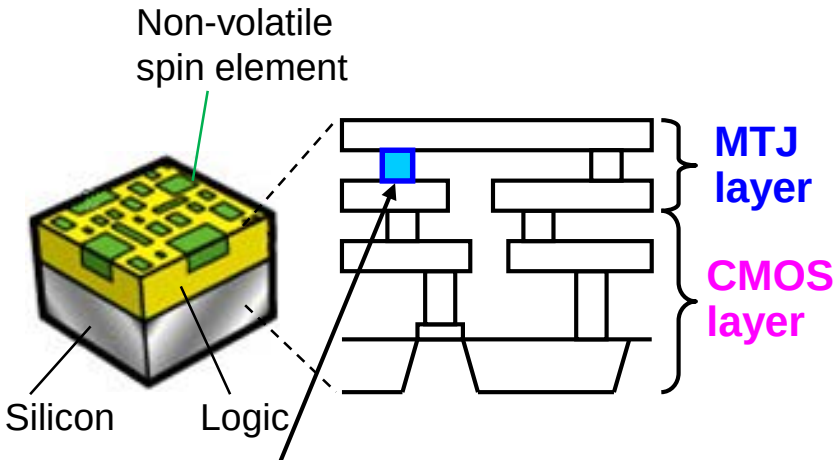
Conventional architecture



-Logic and memory modules are separated
-Many interconnections between modules
-Wire delay dominates chip performance
-Global wires requires large drivers
-On-chip memory is volatile
-Power supply must be continuously applied

Delay: Long, Static power: High

Logic-in-memory architecture



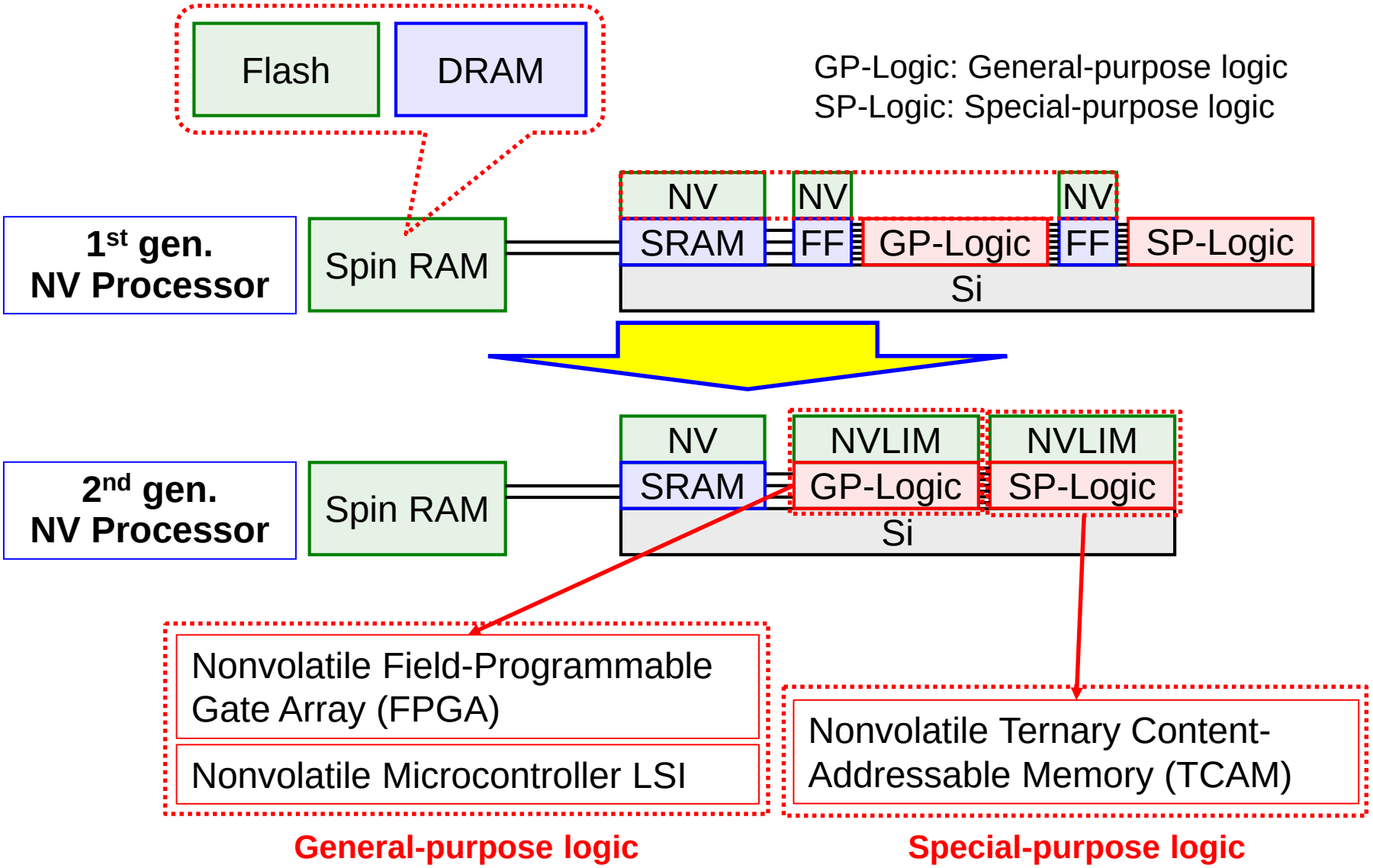
Magnetic Tunnel Junction (MTJ) device

-Non-volatility
-Fast writability
-CMOS compatibility
-Unlimited endurance
-Scalability
-3-D stack capability

-Storage is nonvolatile
-MTJ devices are put on the **CMOS** layer
-Storage/logic are merged

Delay: Short, Static power: Low

Nonvolatile VLSI Processor Architecture



Outline

- Background & Motivation

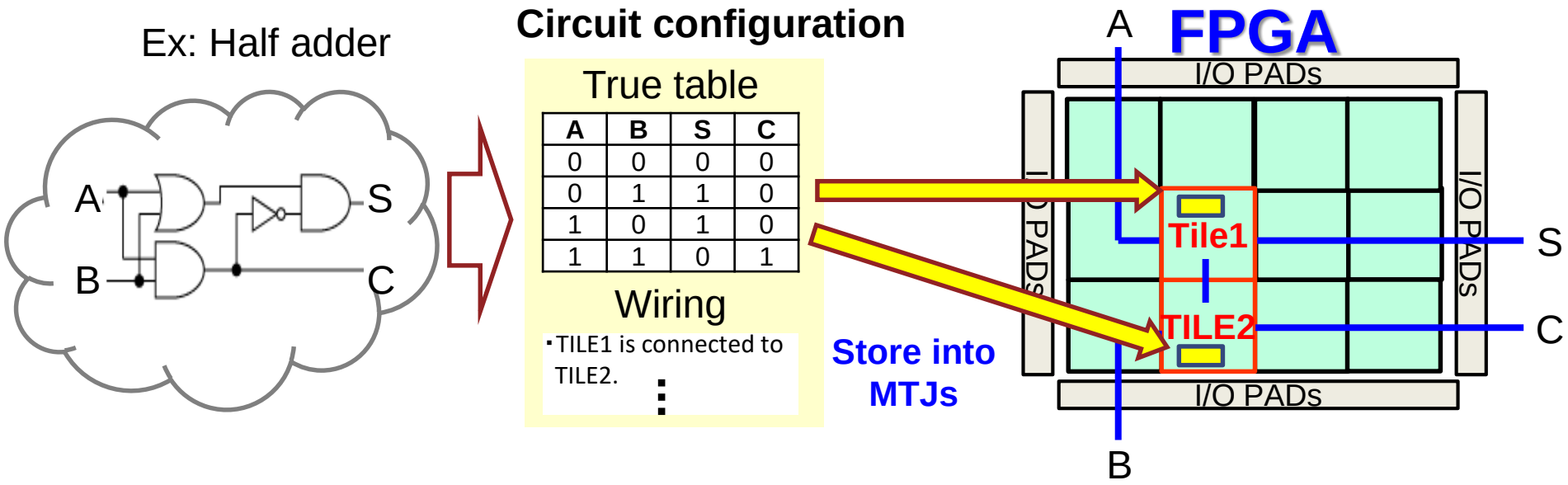
  ~Nonvolatile Logic-in-Memory Architecture~

- **Design of Nonvolatile FPGA**

- VLSI CAD Environment

- Conclusions & Future Prospects

FPGA (Field-Programmable Gate Array)

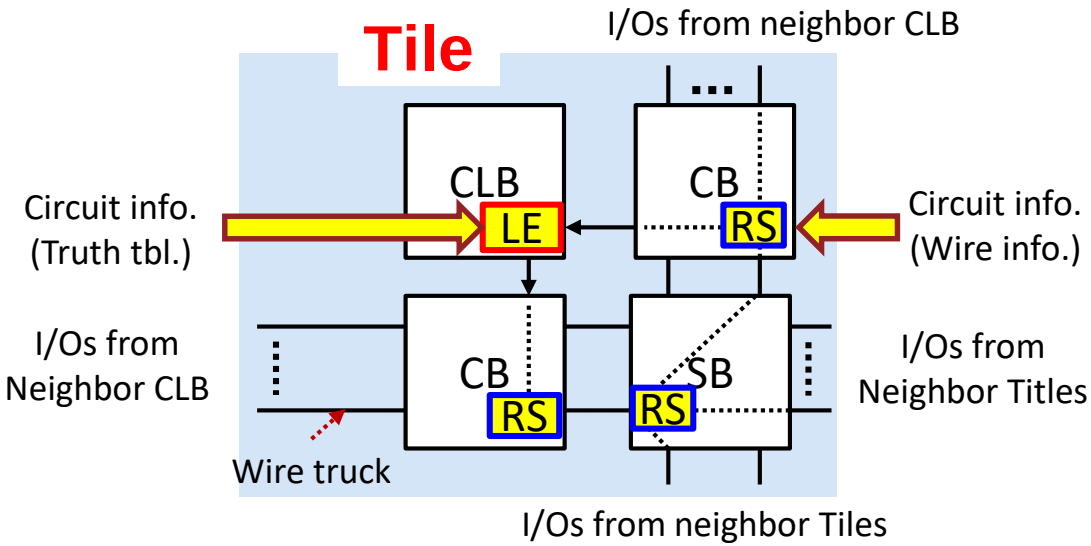


- Circuit functions are programmable by users.
- Circuit configuration including wiring is stored into MTJs. Therefore, there is no re-storing even when power supply is OFF and ON again.

Suited to power-supply control

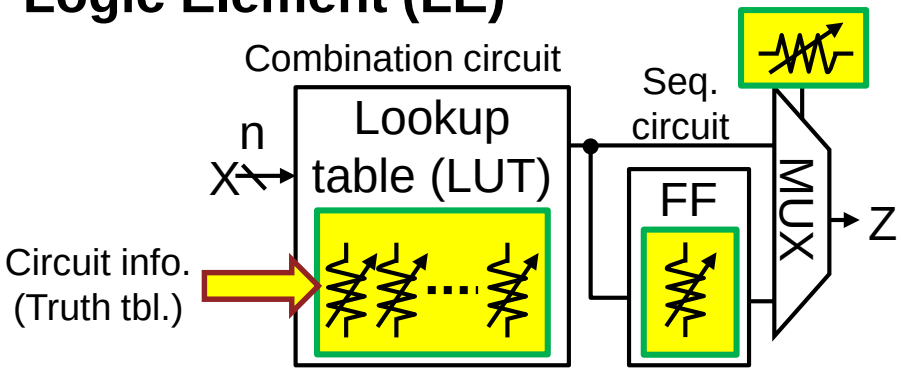
The use of MTJs together with power gating makes standby power reduced

Structure of TILE



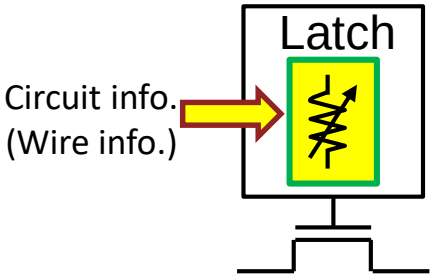
- Configurable logic block (CLB)
  → Logic function of Tile
- Connection Block (CB)
  → Connect to neighbor CLB
- Switch Block (SB)
  → Connect to neighbor Titles

Logic Element (LE)



- Design arbitrary comb./ seq. circuits.
- FF is changed to nonvolatile one.

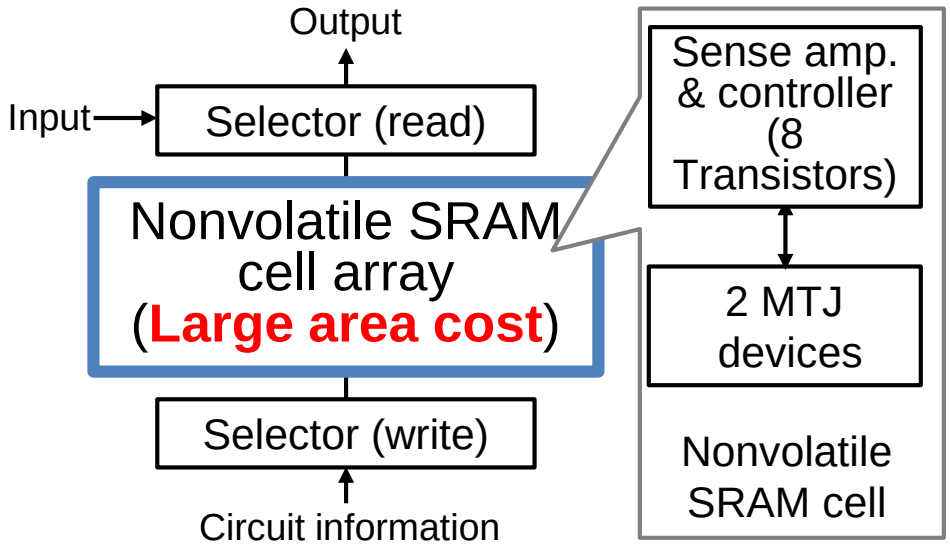
Routing switch (RS)



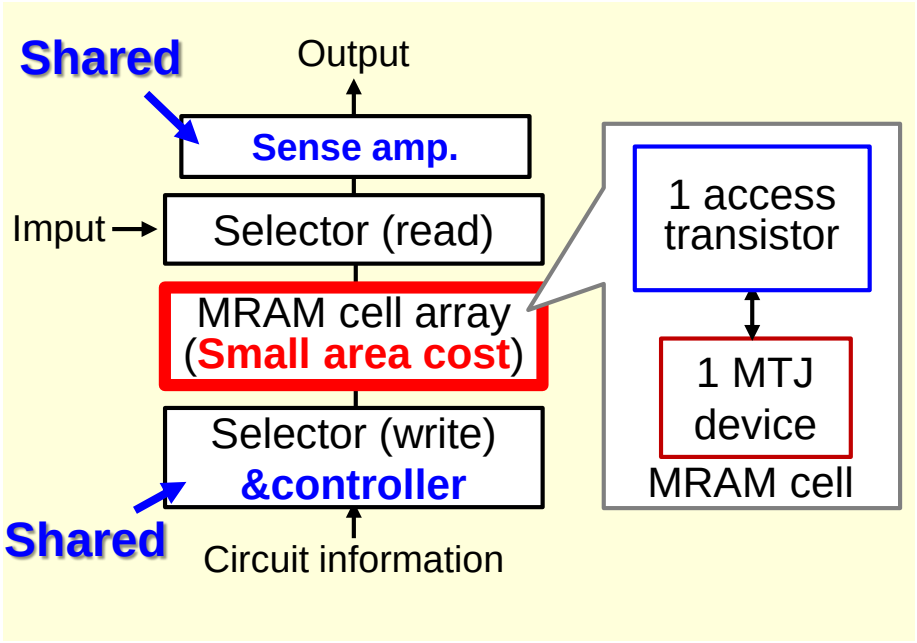
- NMOS pass gate with NV-latch determines wire-truck information.

Logic-in-Memory(LIM) Architecture

■ **LIM-based nonvolatile lookup table (NV-LUT) circuit**

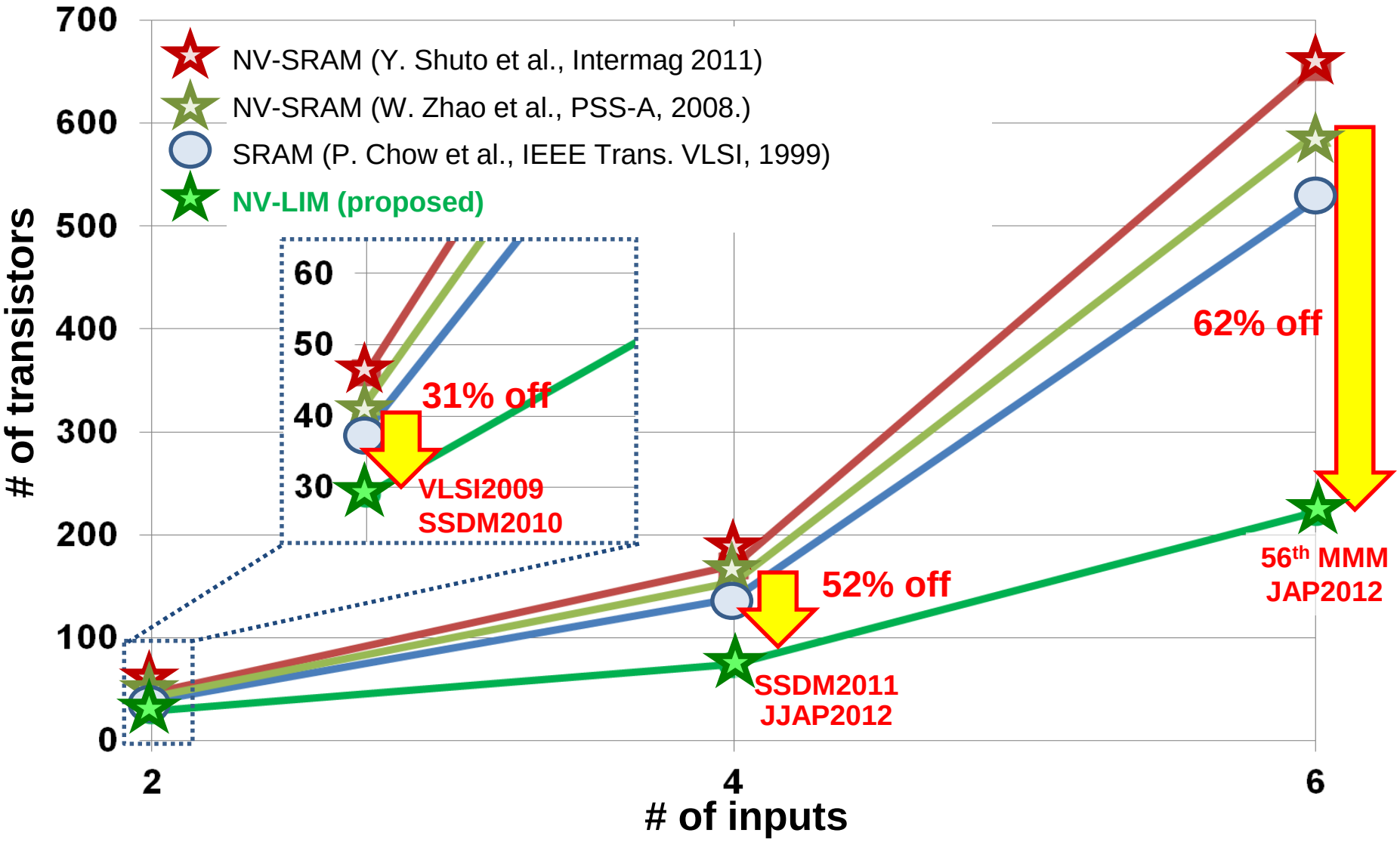


Nonvolatile SRAM-based (conventional)



LIM-based (proposed)

Comparison of Multi-Input LUT circuit



Logic-in-Memory(LIM) Architecture

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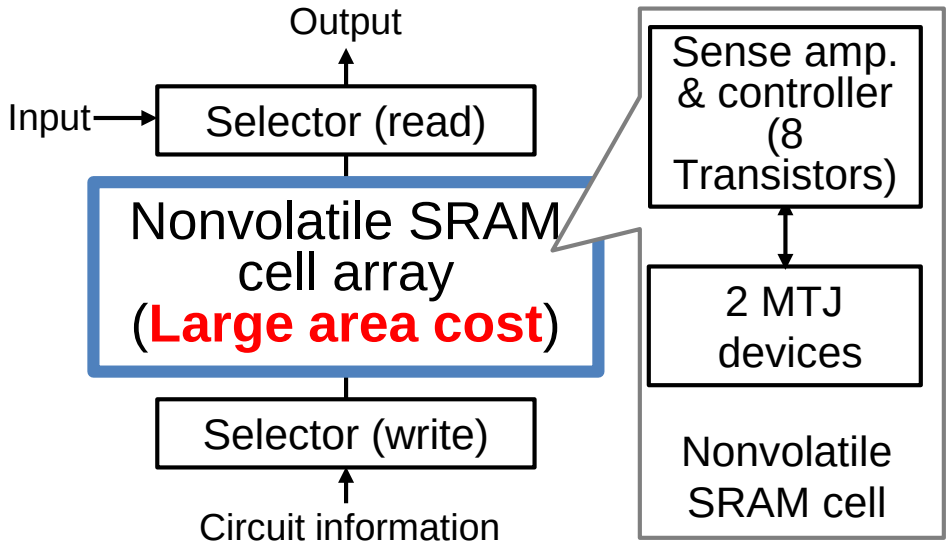
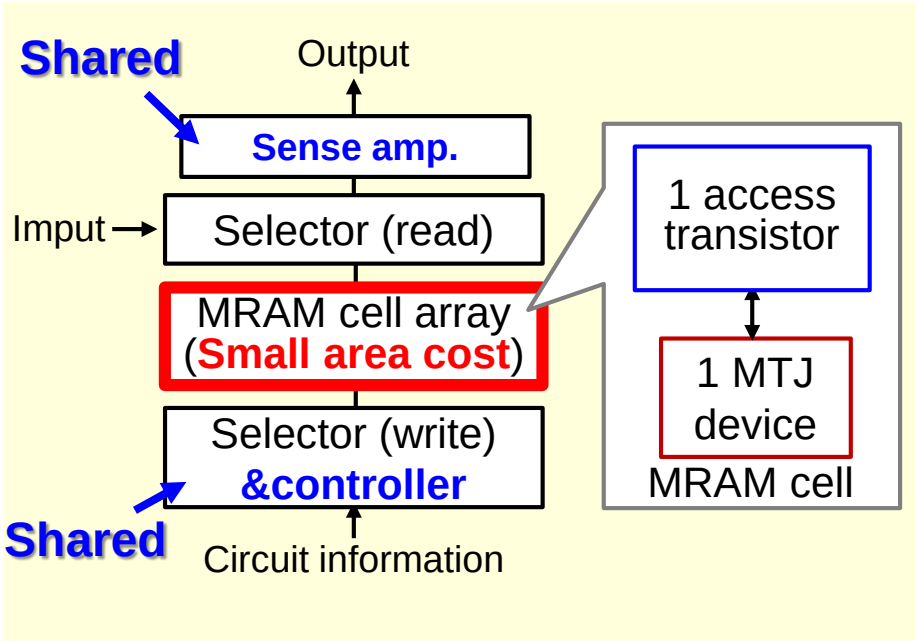
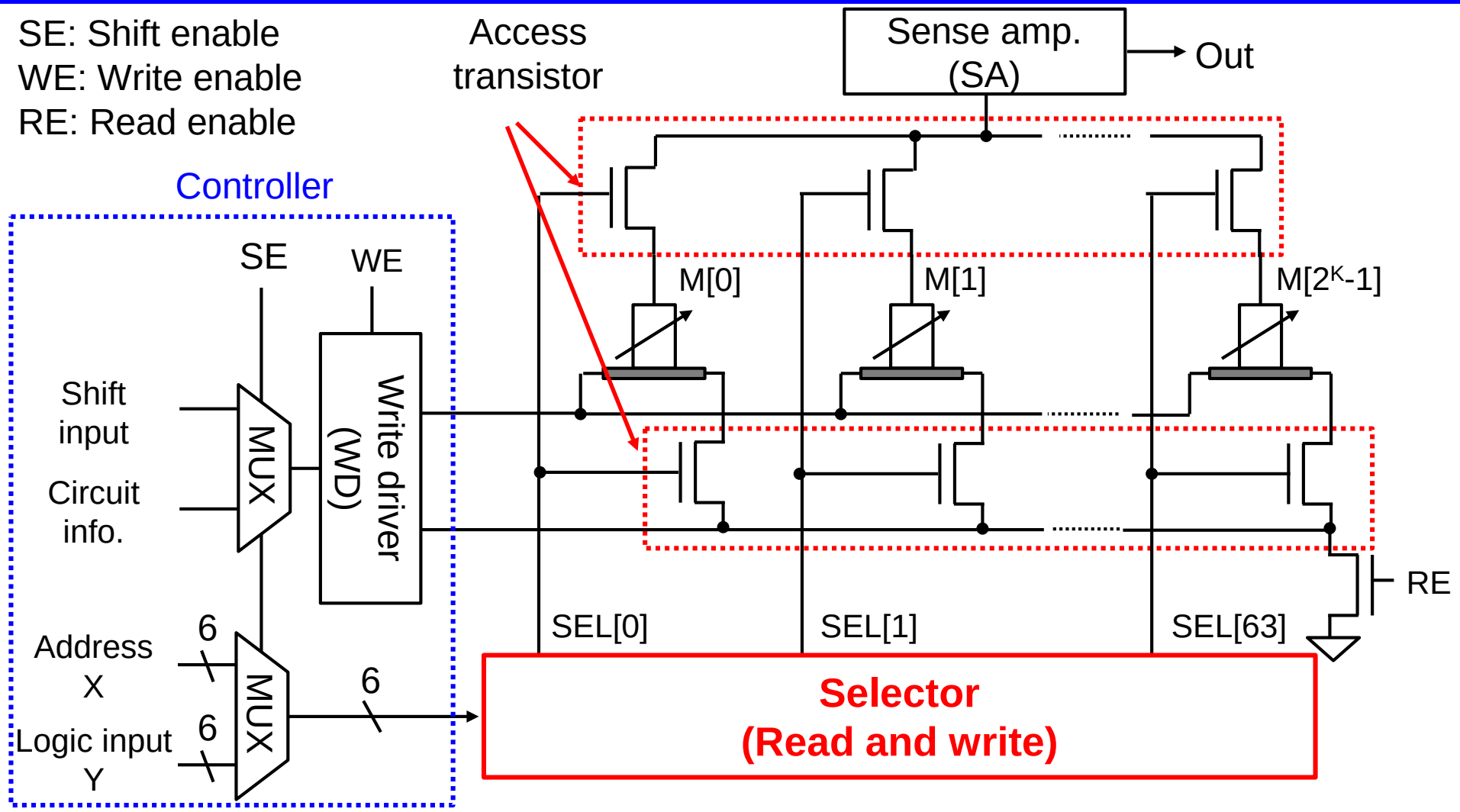


Nonvolatile SRAM-based (conventional)



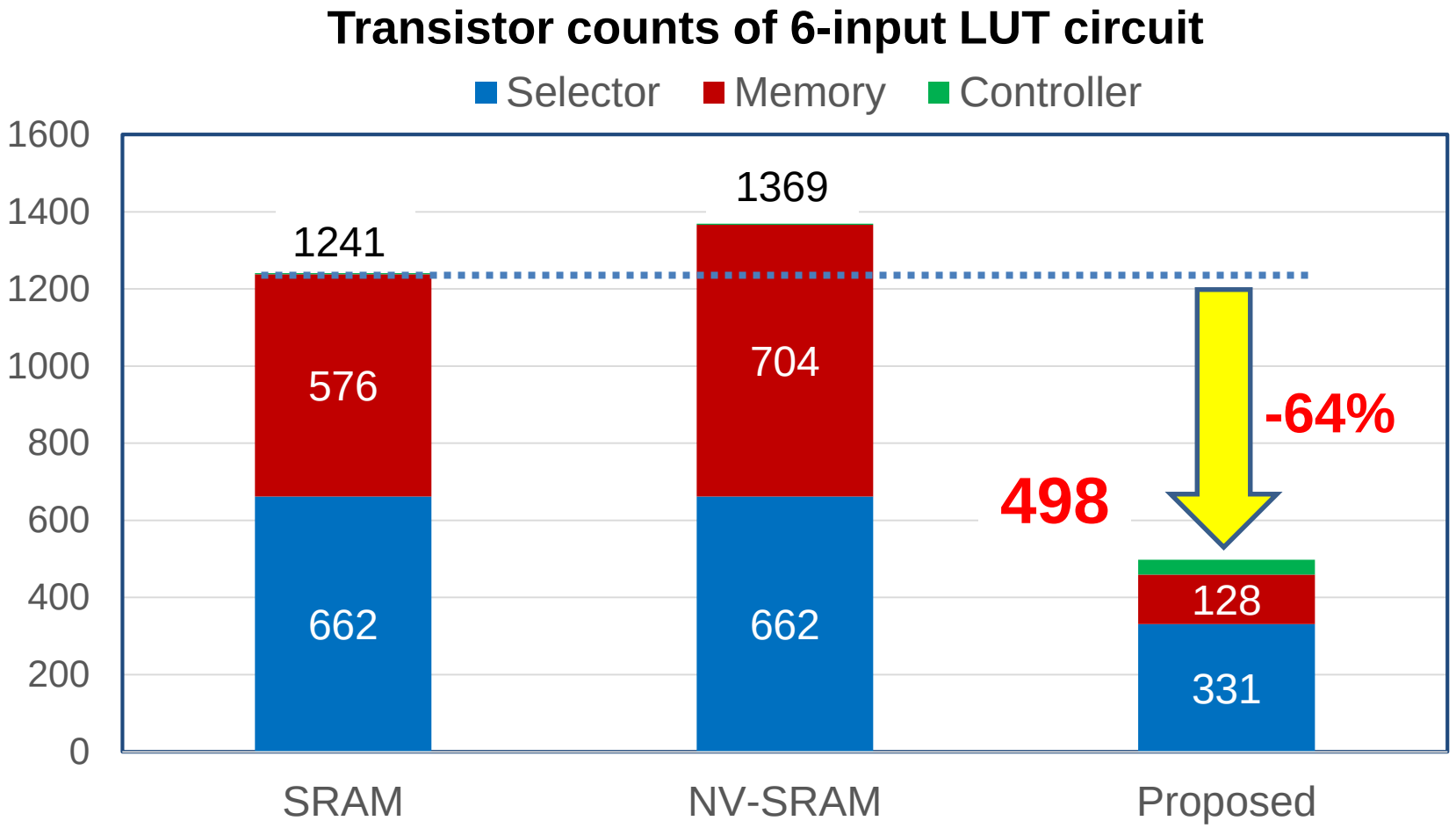
LIM-based (proposed)

NV LUT Circuit



Hardware cost for the selector is reduced.

Comparison of Tr. Counts

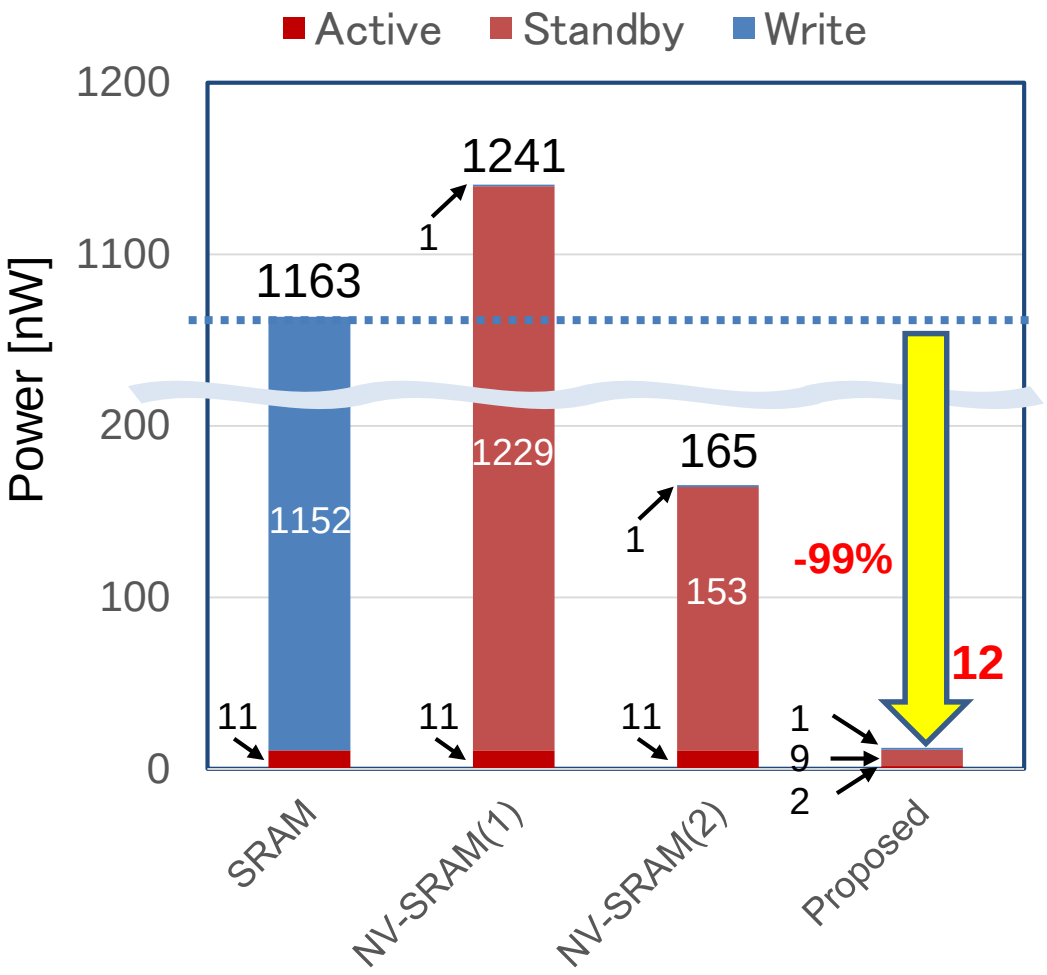


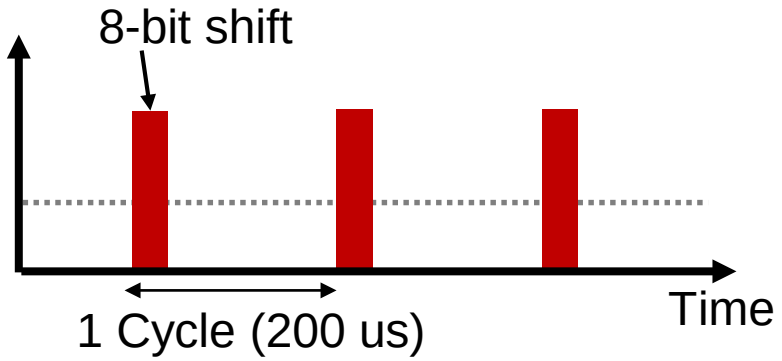
- LIM-based circuitry → Transistor counts reduction in memory part
- Selector is shared in both read and write operations

64% of transistor counts reduction compared to SRAM-based LUT circuit

Comparison of Power Dissipation

Power consumption of 6-input LUT circuit





- 90nm CMOS technology
- Write current:100uA@2ns
- NV-SRAM (1)
  Store data into MTJ devices every time after 1-bit shift operation
- NV-SRAM (2)
  Store data into MTJ devices only before power off

99% of power reduction compared to SRAM-based LUT circuit

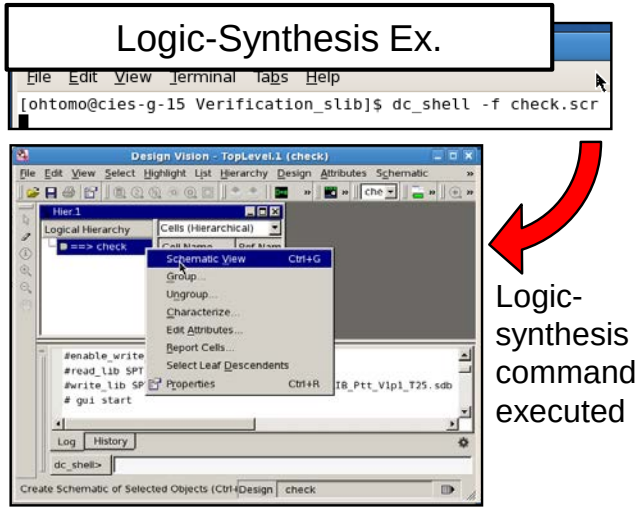
Outline

- Nonvolatile Logic-in-Memory Architecture Overview
- Design of an NV FPGA
- **Other Possibility**
- Conclusions & Future Prospects

VLSI CAD for MTJ/MOS-Hybrid Circuit Design

Logic Synthesis

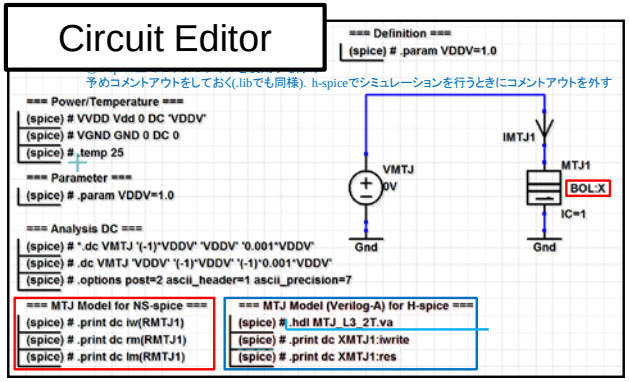
Logic-Synthesis Ex.



Logic-synthesis command executed

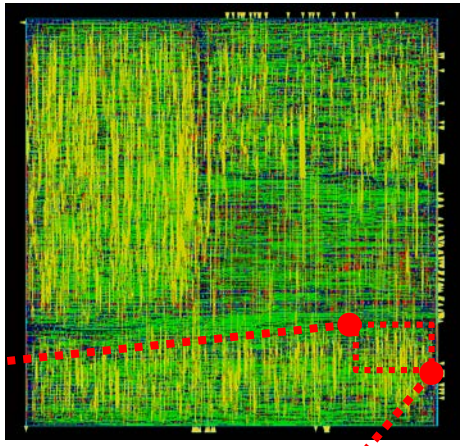
Circuit Simulation

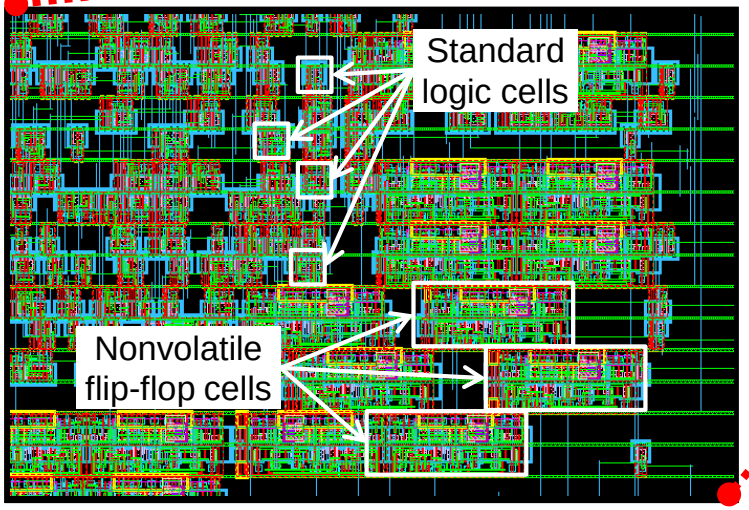
Circuit Editor



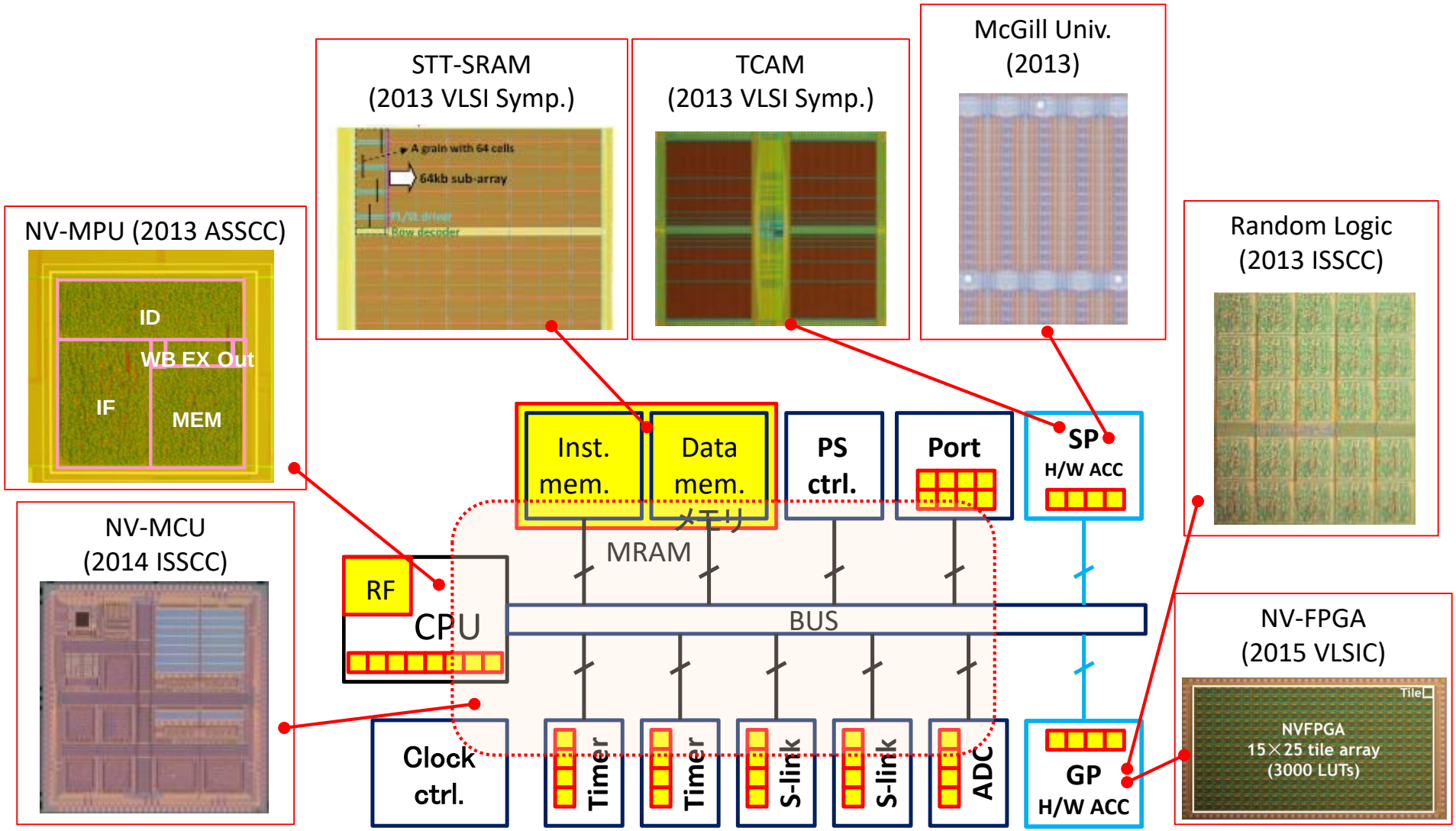
Layout

Layout result





Fabricated Nonvolatile Components



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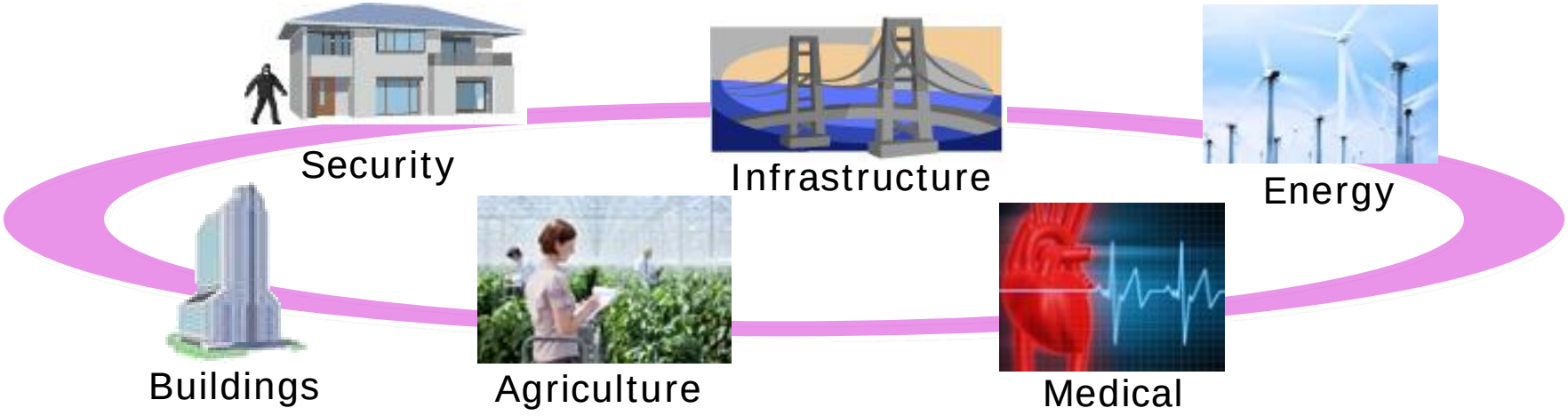
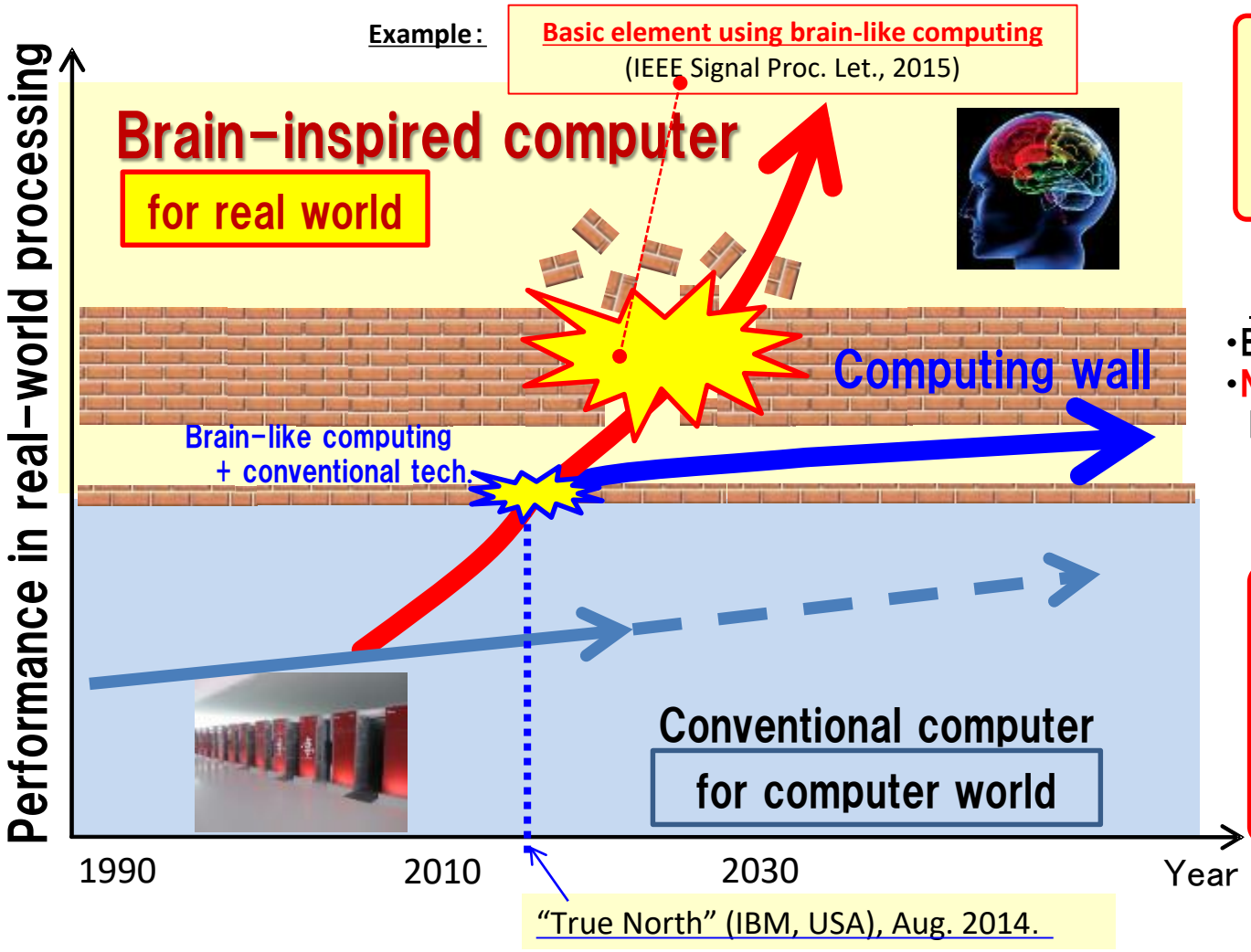
Conclusions & Future Prospects

- Propose a **MOS/MTJ-hybrid** circuit (nonvolatile logic-in-memory circuit using MTJ devices) style for IoE applications
- Key technologies; novel NV LUT Design & VLSI CAD environment to realize practical LSI.

⇨ It could open **ultra-low-power** IoT application paradigm.



Towards Brain-Inspired LSI



"Brainware"
Software/hardware-mixed structure

IBM, USA(Aug. 7, 2014)
"True North" hardware
- Big gain for brain-like comp.
- Not reached to goal of real brain-like computing

<Aim of PJ>
- Explore mechanism & architecture for brainware.
  (Brainware LSI PJ:start in 2014)
- Tohoku U. has a world-class MTJ fabrication process technology.

→Open up a real brain-like computing paradigm!