# Center for Energy Efficient Electronics Science

*A National Science Foundation Science & Technology Center*

# Fabrication of InAs Field Effect Transistors

**Megan Stephanz[1], Jared Carter[2], Eli Yablonovitch[2]**

[1]University of Utah, [2]University of California, Berkeley

## Abstract

One way to further continue the reduction in energy consumption in computing is to reduce the supply voltage in computing circuits. New lower-voltage transistors are required to reduce the supply voltage to less than 300 mV. The Indium Arsenide Bilayer Tunnel Field Effect Transistor (InAs BT-FET) is one attempt to create a new low voltage transistor. The device will be fabricated by transferring ribbons of epitaxially grown InAs from its native substrate of gallium antimonide to silicon chips. Afterwards, appropriate places to build transistors will be identified and utilized before the BT-FETs will be tested and characterized.

## Motivation and Hypothesis

- Electronic devices have made leaps and bounds in energy efficiency as transistors become smaller following Moore's Law.
- Moore's Law is reaching its limit as transistors near the atomic scale.
- If we want to continue improving energy efficiency in computing, a new, low voltage transistor is needed.
- We believe that InAs TFETs are a possible low voltage solution to this problem.

## Sensitive TFET Switching Mechanism

- Unlike standard transistors, the switching mechanism of TFETs relies on the crossing and anti-crossing of energy bands.
- Applying a reverse bias to a pn junction causes the valence and conduction bands of the p and n type semiconductor respectively to approach one another.
- TFETs make use of this: abruptly allowing current to flow when bands come into alignment.

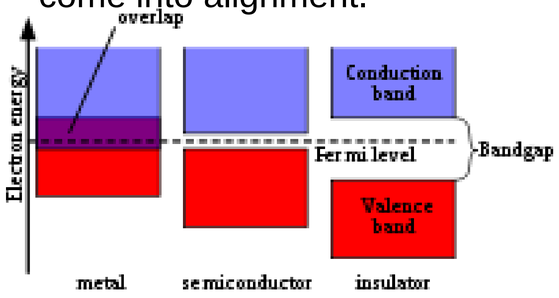


Fig 1: Conductivity of materials depends on energy bands [1]

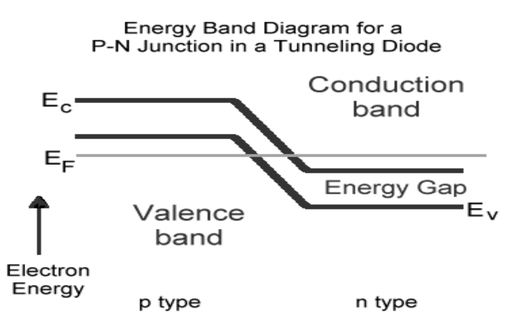


Fig 2: Energy bands across a pn-junction [2]

## Methods: Fabrication of InAs TFETs

- Transfer of InAs nano-ribbons to silicon chip

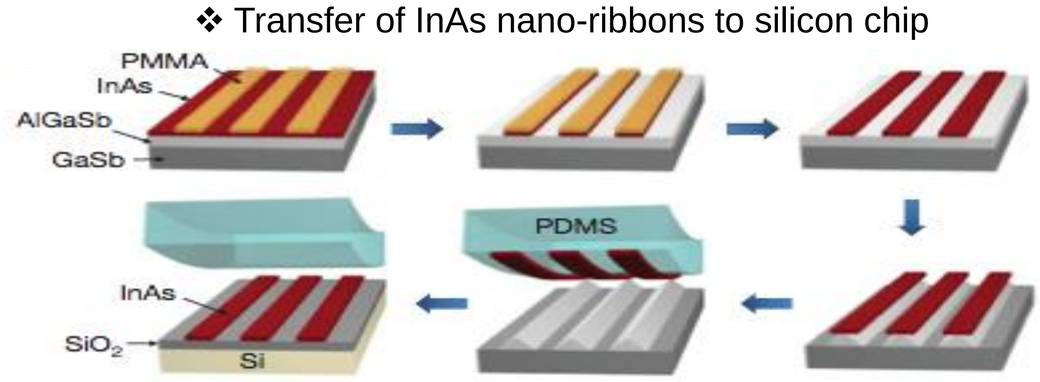


Fig 3: Flowchart of InAs transfer process [3]

- Mapping of adequate nano-ribbon placement locations
- Deposition of oxides and etching of electrodes

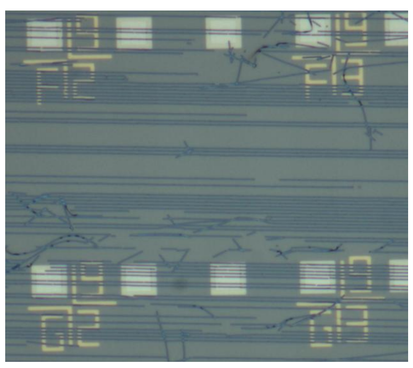

Fig 4: Adequate nano-ribbons at 50x magnification

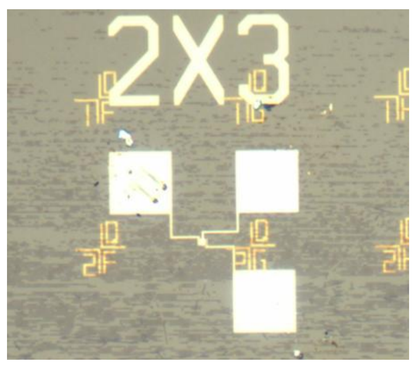


Fig 5: A finished NFET made with similar fabrication technology as a finished TFET

## Device Analysis and Results

- In the absence of completed TFETs, measurements were taken of the available NFETs using a MEMS Cascade probe station and a Semiconductor Parameter Analyzer.
- Transfer curves were taken of the drain current over varying gate voltage at constant drain voltages of both 50 mV and 500 mV for transistors of varying channel lengths and nano-ribbon counts, from which were extracted $I_{on,w}$, $I_{off,w}$, $I_{on}/I_{off}$, and subthreshold slope (SS).

| Channel Length (μm) | Nanoribbon Count | $I_{on,w}$ (μA/μm) | $I_{off,w}$ (μA/μm) | $I_{on}/I_{off}$ | Subthreshold Slope (mV/dec) |
|---|---|---|---|---|---|
| 4 | 7 | 6.41E+00 | 7.74E-05 | 9.14E+04 | 324 |
| 4 | 3 | 2.85E+00 | 5.04E-05 | 7.75E+04 | 340 |
| 4 | 3 | 5.20E+00 | 3.82E-05 | 1.50E+05 | 393 |
| 2 | 5 | 1.71E+01 | 2.65E-04 | 6.95E+04 | 367 |
| 2 | 3 | 2.60E+01 | 2.58E-04 | 1.07E+05 | 396 |
| 2 | 2 | 1.66E+01 | 2.44E-04 | 7.58E+04 | 342 |
| 1 | 7 | 1.50E-01 | 8.36E-04 | 1.70E+02 | 370 |
| 1 | 5 | 2.22E+01 | 5.46E-04 | 4.85E+04 | 446 |
| 1 | 5 | 2.17E+01 | 5.51E-04 | 5.09E+04 | 357 |
| 0.5 | 10 | 1.13E+01 | 1.66E-03 | 2.07E+04 | 369 |
| 0.5 | 7 | 4.30E+01 | 8.36E-04 | 6.55E+04 | 400 |
| 0.5 | 2 | 2.20E+01 | 2.07E-03 | 2.33E+04 | 340 |
| 0.25 | 9 | 5.45E+01 | 5.42E-03 | 7.29E+03 | 351 |

**Range of Data:**

- $I_{on,w}$: 0.15 to 54.5 μA/μm
- $I_{off,w}$: 3.82e-5 to 5.42e-3 μA/μm
- $I_{on}/I_{off}$: 1.7e2 to 1.07e5
- SS: 324 to 446 mV/decade

- The lowest subthreshold slope value found among the NFETs is still more than five times the current limitation of 60 mV/decade. This is due to the high interface trap density (~5e13 $cm^2/eV$) at the gate insulator-InAs interface.

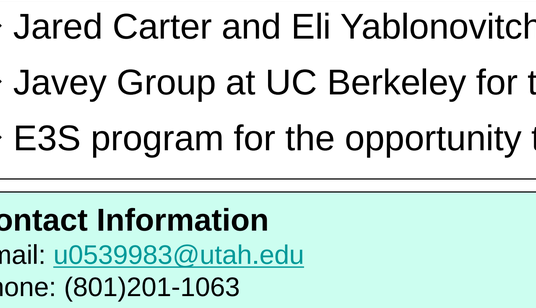


Fig 6: 4x7 NFET, Lowest Subthreshold Slope

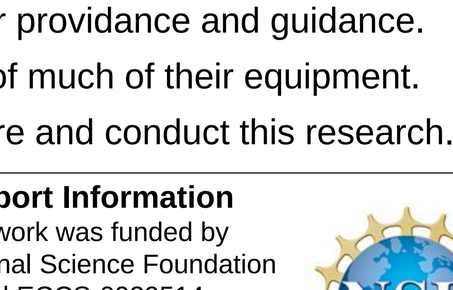


Fig 7: Comparative schematic of desirable TFET and MOSFET slopes [4]

## Conclusion and Next Steps

- We were successful in inducing n-channels in layer transferred InAs with performance in line with older results, although the subthreshold slopes could be improved.
- The poor subthreshold slopes can be attributed to interface traps at the insulator-InAs interface. More careful modeling of the $D_{it}$ of that interface will allow us to extract the 'intrinsic steepness' of the TFETs.
- In the future, we must continue by finishing completion of TFET devices and conducting the appropriate measurements.

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**Contact Information**
Email: u0539983@utah.edu
Phone: (801)201-1063

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**Figure References:**
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