Germanium Vertical Field Effect Transistor

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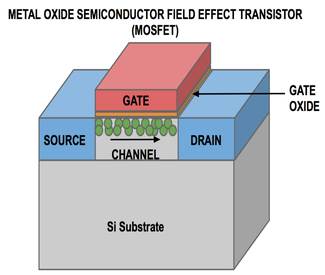
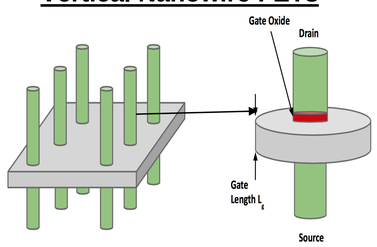
Abstract — To increase the density of transistors on an integrated-circuit "chip" without further scaling down the transistor gate length, a vertically oriented germanium-channel field-effect transistor (Ge-vFET) design is proposed. Technology computer-aided design (TCAD) simulations of Ge-vFET devices indicate that a high on-off current ratio, up to 7 orders of magnitude, can be achieved if the gate-length (L_g) to channel width ($W_{channel}$) ratio is sufficiently large. The optimal dopant concentration for this junctionless FET design is found to be ~10^{17} cm^{-3}.

Introduction

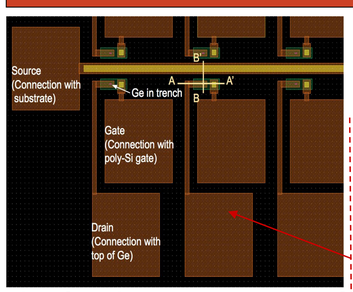
- Parasitic resistances & capacitances become increasingly significant when conventional planar metal-oxide-semiconductor field-effect transistors (MOSFET) are miniaturized for high device density
- Higher density can be achieved by vertically orienting the FETs, without the need to reduce gate length (L_g) or gate-to-contact spacing (L_s)



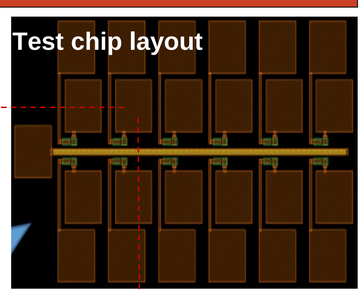
Vertical Nanowire FETs



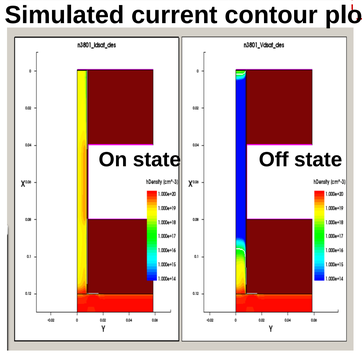
Experimental Procedures



Test chip layout

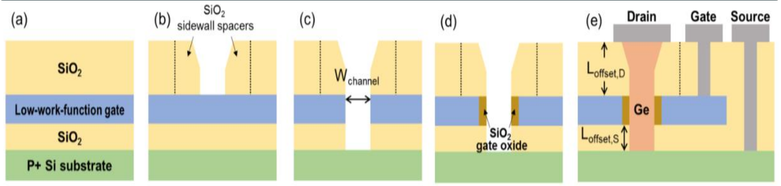


Simulated current contour plots



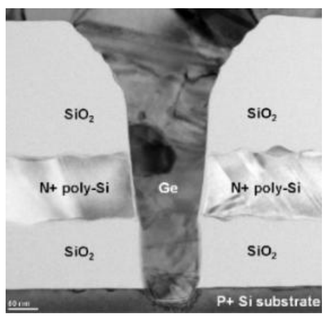
- Measurements of fabricated Ge vFET *I-V* characteristics were made using a Cascade wafer-probe station
- Technology computer-aided design software, Sentaurus Device, was used to simulate Ge-vFET *I-V* characteristics to guide design optimization

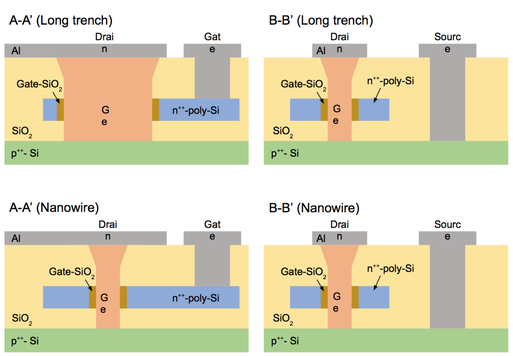
Ge-vFET Fabrication Process



Cross-sectional views illustrating the Ge-vFET fabrication process:
(a) Initial spacer/poly-Si gate/spacer layer formation over doped Si substrate
(b) Sub-lithographic hole/trench definition using self-aligned sidewall spacers
(c) Channel hole/trench formation
(d) Gate dielectric formation by thermal oxidation
(e) Selective Ge growth in hole/trench, followed by contact hole formation and metallization

Cross-sectional transmission electron micrograph (XTEM) of a faricated Ge-vFET:

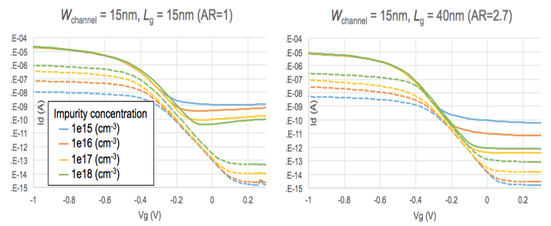


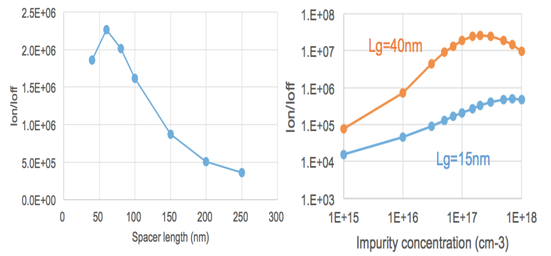


The Ge channel can comprise either a vertical fin formed in a trench (top diagram) or a nanowire formed in a hole (bottom diagram)

References:
[1] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Transactions on Electron Devices*, Vol. 59, pp. 1813-1828, 2012.
[2] Colinge, J.-P. "Junctionless transistors", Future of Electron Devices, Kansai (IMFEDK), 2012 IEEE International Meeting, pp. 1-2, 2012.

Ge-vFET Simulation Results





- On-state current (I_{ON}) and on/off current ratio improve with increased $L_g/W_{channel}$ ratio
- Spacer thickness should be optimized for maximum on/off current ratio
- The optimal channel dopant concentration is ~10^{17} cm^{-3}

Conclusions

Ge-vFETs potentially can achieve good performance characteristics with a smaller footprint than conventional planar MOSFETs.
Practical challenges for realizing the promise of Ge-vFET technology include the formation of high-quality Ge in nanometer-scale trenches and holes, and the formation of a high-quality gate insulating layer.

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