**Germanium Vertical Field Effect Transistor**

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**Abstract** — To increase the density of transistors on an integrated-circuit “chip” without further scaling down the transistor gate length, a vertically oriented germanium-channel field-effect transistor (Ge-vFET) design is proposed. Technology computer-aided design (TCAD) simulations of Ge-vFET devices indicate that a high on-off current ratio, up to 7 orders of magnitude, can be achieved if the gate-length ($L_g$) to channel width ($W_{channel}$) ratio is sufficiently large. The optimal dopant concentration for this junctionless FET design is found to be $\sim 10^{17}$ cm$^{-3}$.

**Introduction**

- Parasitic resistances & capacitances become increasingly significant when conventional planar metal-oxide-silicon field-effect transistors (MOSFET) are miniaturized for high device density
- Higher density can be achieved by vertically orienting the FETs, without the need to reduce gate length ($L_g$) or gate-to-contact spacing ($L_c$)

**Ge-vFET Fabrication Process**

- On-state current ($I_{ON}$) and on/off current ratio improve with increased $L_g/W_{channel}$ ratio
- Spacer thickness should be optimized for maximum on/off current ratio
- The optimal channel dopant concentration is $\sim 10^{17}$ cm$^{-3}$

**Cross-sectional views illustrating the Ge-vFET fabrication process:**

1. Initial spacer/poly-Si gate/spacer layer formation over doped Si substrate
2. Sub-lithographic hole/trench definition using self-aligned sidewall spacers
3. Channel hole/trench formation
4. Gate dielectric formation by thermal oxidation
5. Selective Ge growth in hole/trench, followed by contact hole formation and metallization

**Ge-vFET Simulation Results**

- Measurements of fabricated Ge vFET I-V characteristics were made using a Cascade wafer-probe station
- Technology computer-aided design software, Sentaurus Device, was used to simulate Ge-vFET I-V characteristics to guide design optimization

**References:**


**Conclusions**

Ge-vFETs potentially can achieve good performance characteristics with a smaller footprint than conventional planar MOSFETs.

Practical challenges for realizing the promise of Ge-vFET technology include the formation of high-quality Ge in nanometer-scale trenches and holes, and the formation of a high-quality gate insulating layer.

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