Reliability of SiC power MOSFETs

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Abstract

Silicon Carbide (SiC) is an important semiconductor for high power electronics because of its unique properties, such as high electrical breakdown, high thermal conductivity, and high saturated electron drift velocity. Recently, these characteristics have been exploited in fabricating SiC power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET). Understanding the behavior and failure mechanism of these power devices through aging is of particular importance, because of their applications in high power switching circuitry.

Methodology

Accelerating the device aging via electrical stress, monitoring its main figures of merit (FOM):

- On-resistance (R_{on})
- Threshold voltage (V_t)
- Subthreshold swing (S)
- Saturation current (I_{dsat})

A variety of stress conditions were considered in order to understand device degradation.

A measurement system was developed in order to characterize and stress the transistor up to 200 V and 100 mA.

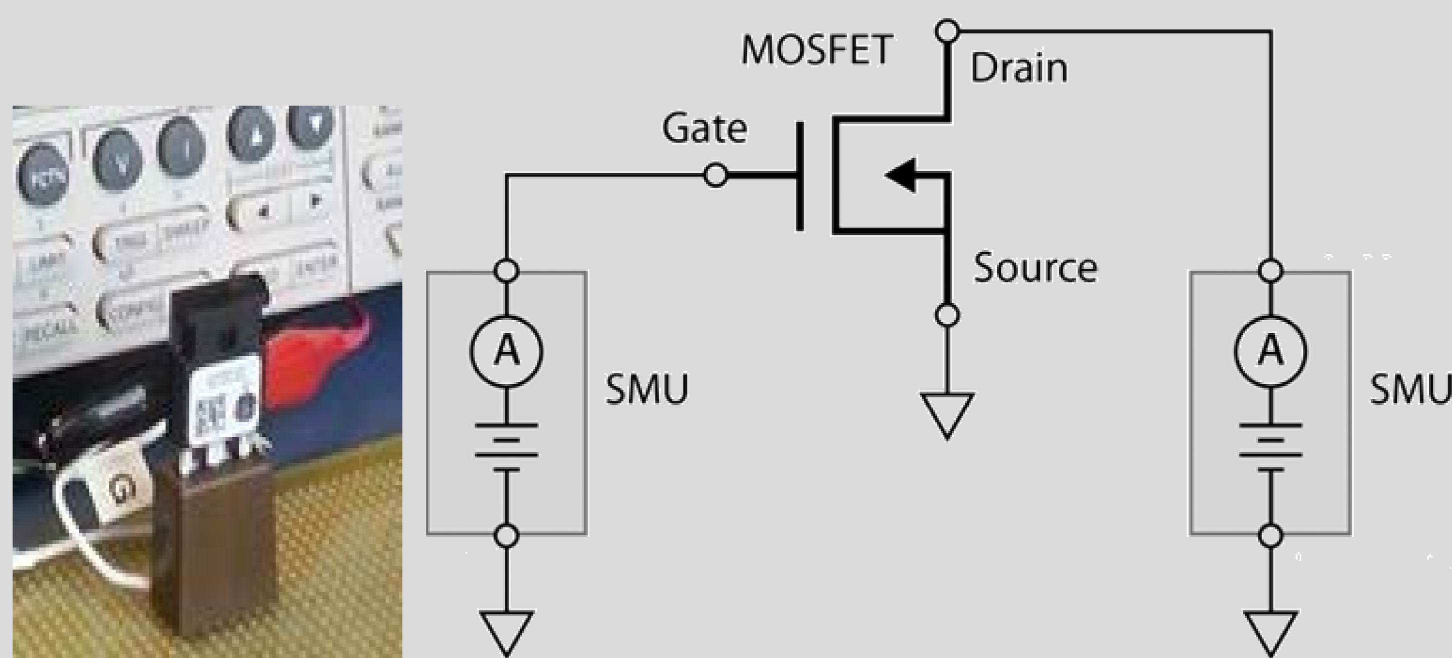

Figure 1. (Left) SiC power MOSFET in a Transistor Outline (TO) package. The device can hold up to 1200V V_{ds} and 20A I_{ds}. (Right) Circuit diagram of stress system for MOSFET testing.

Results

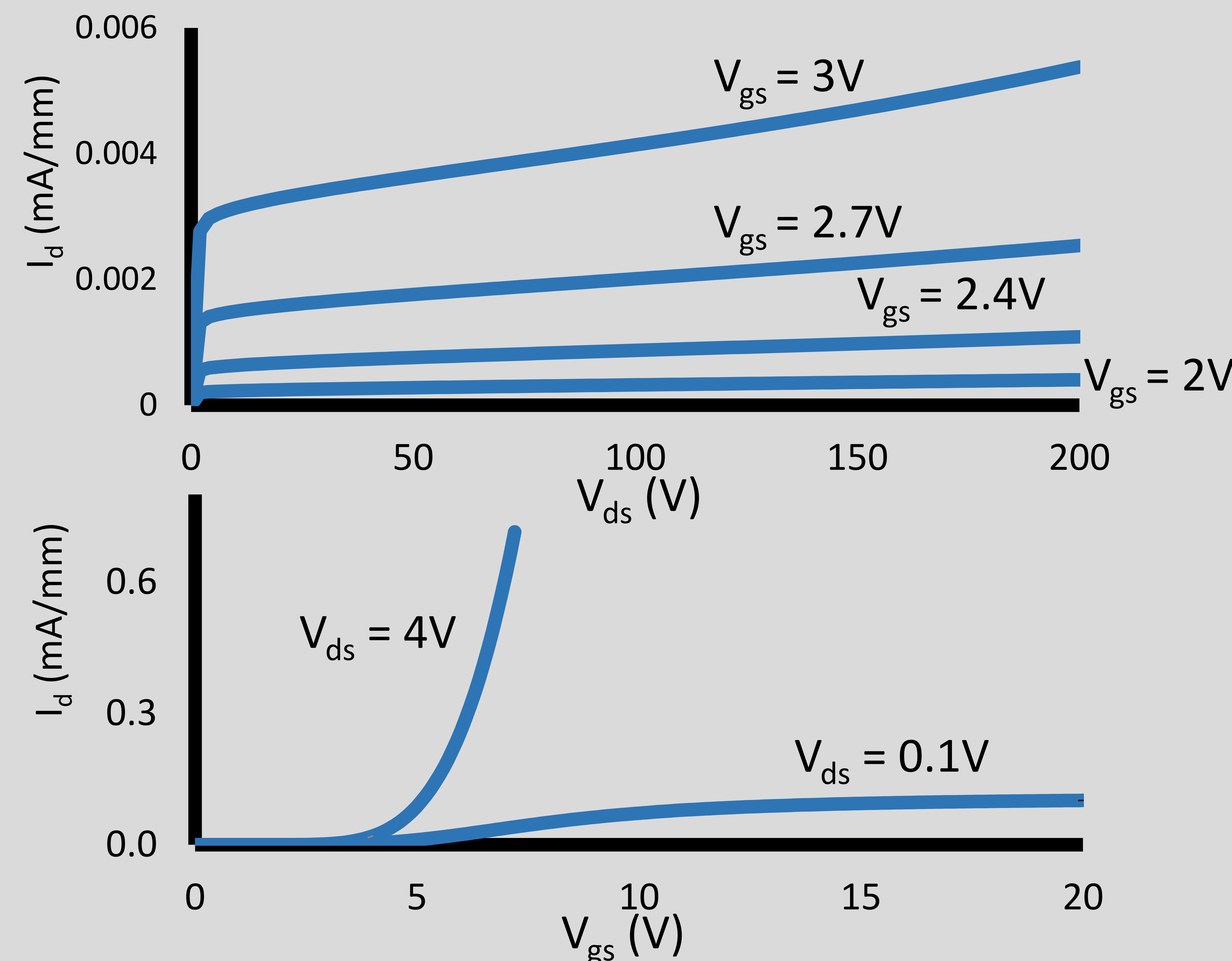

Figure 2. Output (up) and Transfer (down) characteristics of a virgin SiC MOSFET, as obtained in our measurement system.

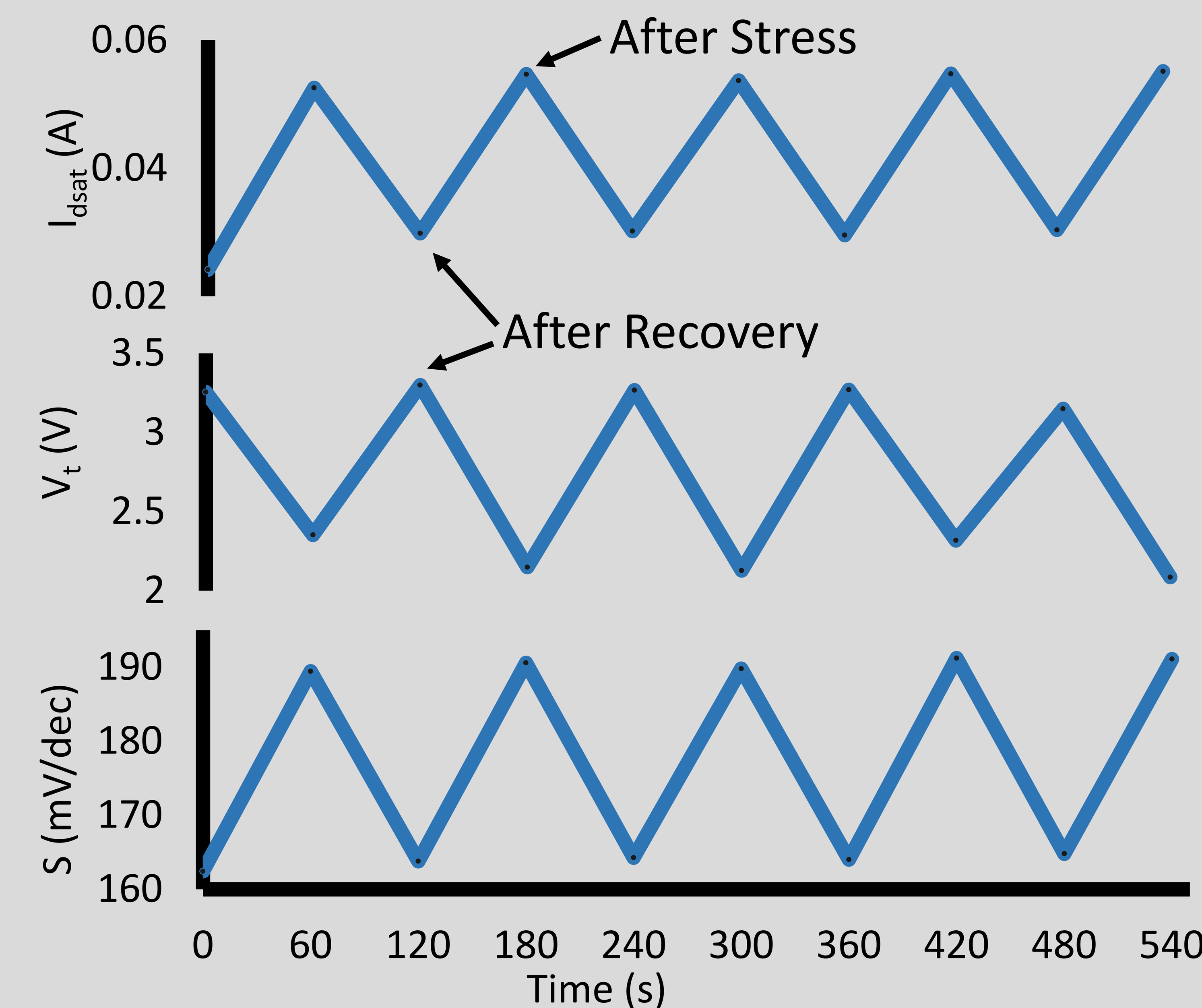

Figure 3. Device FOM during typical stress test consist of 5 cycles of 1 minute stress of Vgs = 4V and Vds = 200V and 1 minute of recovery. (top) Current Saturation (middle) threshold voltage and (bottom) subtreshold swing .

Discussion

The positive bias stress causes a negative shift in V_t and consequently I_{dsat} increases. The fact that the degradation is fully recoverable suggest that the observed degradation is due to carrier trapping. In addition , the degradation in S suggests that part of the traps are at the Oxide-Semiconductor interface.

FOM	Degradation (%)	Recovery Time (s)
Vt	35%	49
S	16%	50
Isat	150%	30

Table 1. Degradation of the device in percentages after 1 minute of stress and its full recovery time.

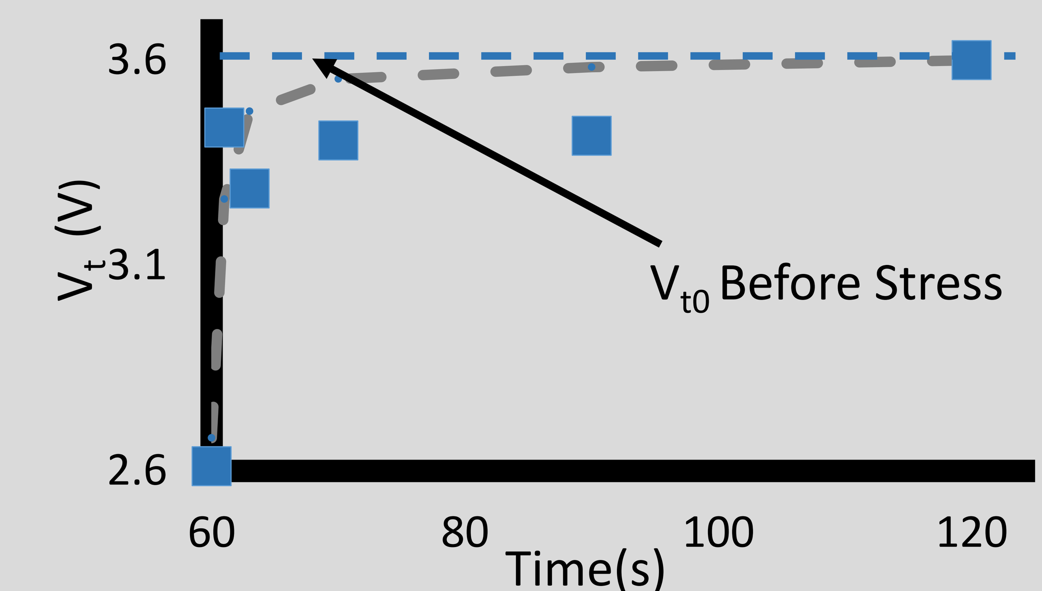

Figure 4. Recovery time of threshold voltage after 1 minute of stress applied. Gray dashed line – exponential fit of data.

Conclusions

We have developed a measurement system to study the aging process of high power SiC MOSFETs. Using this system, we found stress conditions which accelerate the device aging but do not cause permanent damage.

Future work:

- Understanding the conditions that creates permanent damage and looking for physical reason.
- Develop a model to predict the Remaining Useful Life of the device.

References

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