Center for Energy Efficient Electronics Science
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Back-gated Sub-4 Layer $MoTe_2$ Ultra-thin Body p-MOSFETs

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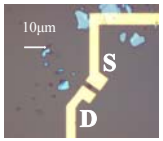
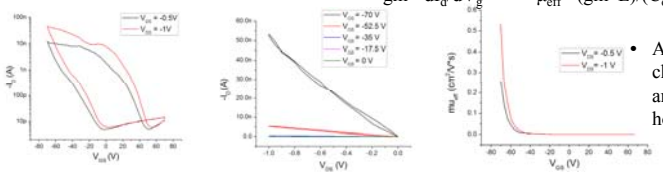
Abstract
Molybdenum ditelluride ($MoTe_2$) is a heavy carrier concentration 2D layered semiconductor, investigated to achieve high I_{on}/I_{off} ratio as a p-MOSFET with quasi-Ohmic S/D contacts. Back-gated sub-4 layer $MoTe_2$ p-MOSFETs were fabricated and the drain current (I_d) – gate voltage (V_g) characteristics were measured at room temperature. I_{on}/I_{off} and the effective mobility values were extracted. Contact studies were performed using Pt/Au and Pd/Au and the impact of annealing were investigated.

Introduction
- Using 2D layered semiconductors for multi-gate and ultra-thin body MOSFET applications.
  - Overcome short channel effects and optimized power consumption.
  - Channel thickness as small as 0.7nm.
  - E.g. Monolayer double-gated MoS_2 MOSFETs and Monolayer top-gated WSe_2 p-FETs [1, 2]
- Fabricated back-gated ultra-thin body p-MOSFETs with $MoTe_2$.
  - Hole mobility reported up to 20 $cm^2/V*s$ and $I_{on}/I_{off} \sim 10^6$ [3].
  - Ability to achieve quasi-ohmic contact to metals without doping due to its heavy carrier concentration of ~1e21 cm^{-3}.
- Study the electrical characterization of sub-4 layer $MoTe_2$ pMOSFETs at 300K and hole mobility.
- Contact study (Pd/Au vs. Pt/Au) and further contact improvement.

Results
Pt/Au Contacts ~3 layers thick, L=1.8 µm, W= 1.6 µm

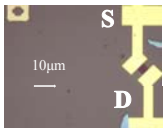
Mobility and transconductance extracted through:
$gm = dI_d/dV_g$ $\mu_{eff} = (gm*L)/(C_{ox}*W*Vds)$





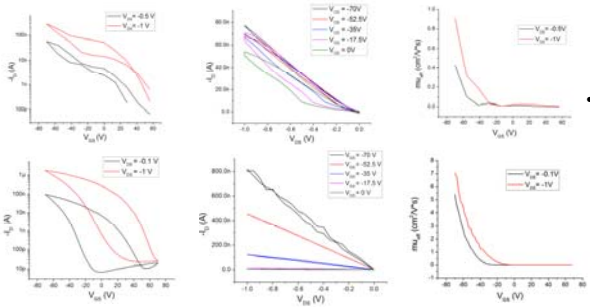
- Almost no change after annealing for 1 hour @ 100 ° C

Pd/Au Contacts ~4 layers thick, L= 3.5 µm, W= 3.4 µm



Before annealing for 1 hour @ 100° C

After annealing for 1 hour @ 100° C



- Drain current 10x after annealing

References
[1]B. Radisavljevic et al., "Single-Layer MoS_2 Transistors," *Nat. Nano.*, vol. 6, no. 3, pp. 147-150, Mar. 2011.
[2]H. Fang et al., "High-Performance Single Layered WSe_2 p-FETs with Chemically Doped Contacts," *Nano Lett.*, vol. 12, no. 7, pp. 3788-3792, Jun. 2012.
[3]N. R. Pradham et al., "Field-Effect Transistors Based on Few-Layered α-$MoTe_2$," *ACS Nano*, vol. 8, no. 6, pp. 5911-5920, May, 2014.

Acknowledgements
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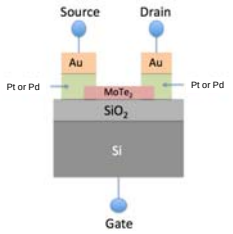
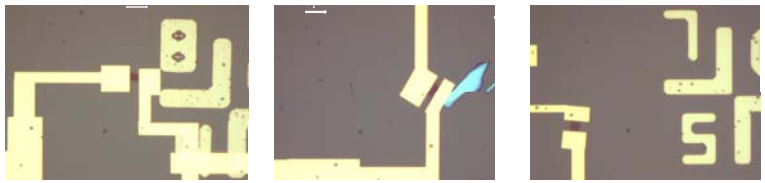
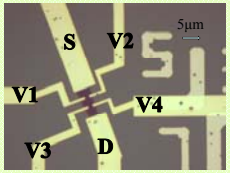
Fabrication Process
- Exfoliate $MoTe_2$ flakes onto Si/SiO_2 (260nm) substrate
- Electron-beam lithography (EBL) (optional; mask: Xe)
- Xe etching for flake uniformity (optional)
- EBL (mask: S/D)
- Metal deposition (Pt/Au: 10/30 nm or Pd/Au: 10/30 nm)
- Lift-off
- For optional top-gate: EBL (mask: gate). Atomic layer deposition (ALD) of 20nm of ZrO_2 high-k dielectric, 30nm of Au evaporation
- Lift-off

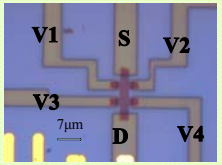




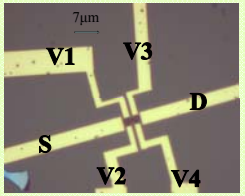
Conclusions
- Quasi-ohmic contact to $MoTe_2$ was obtained by Pd/Au with Ion/Ioff ~10^4 and effective hole mobility ~7 $cm^2/V*s$.
- Pd/Au contact improvement after annealing due to the diffusion of Pd.
- Pd/Au is a better contact for $MoTe_2$ compared to Pt/Au.
  - Higher drain current (1.8 µA vs. 51nA) and higher Ion/Ioff (10^4 vs 10^3).
  - More straightforward evaporation process.

Future Work- 6 terminal Hall Measurements


Hall Bar Design



Bridge Design



- Perform Hall measurements with Pd/Au contacts from 100K to 300K.
- Extract mobility independent of contact at different temperature.

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Support Information
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