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Design Optimization of NEM Switch Fabricated in Standard 65nm CMOS Back-End-of-Line Process

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Abstract

The design of a single-pole/double-throw (SPDT) nano-electro mechanical (NEM) switch implemented using the metal interconnect layers available in a standard 65 nm CMOS back-end-of-line (BEOL) process is investigated for non-volatile NEM memory (NEMory) applications. The Coventorware MEMS+ finite element analysis (FEA) software tool is used to study design trade-offs. The device geometry and dimensions are optimized to minimize the switching energy, mechanical delay and settling time.

Introduction

Hybrid CMOS/NEM technology recently has been proposed to enable faster and more energy-efficient data searching as compared with CMOS technology [1]. This work investigates the design of a non-volatile SPDT NEM switch implemented using a standard 65 nm CMOS BEOL process, to elucidate trade-offs between performance and energy efficiency.

NEMory Cell Design

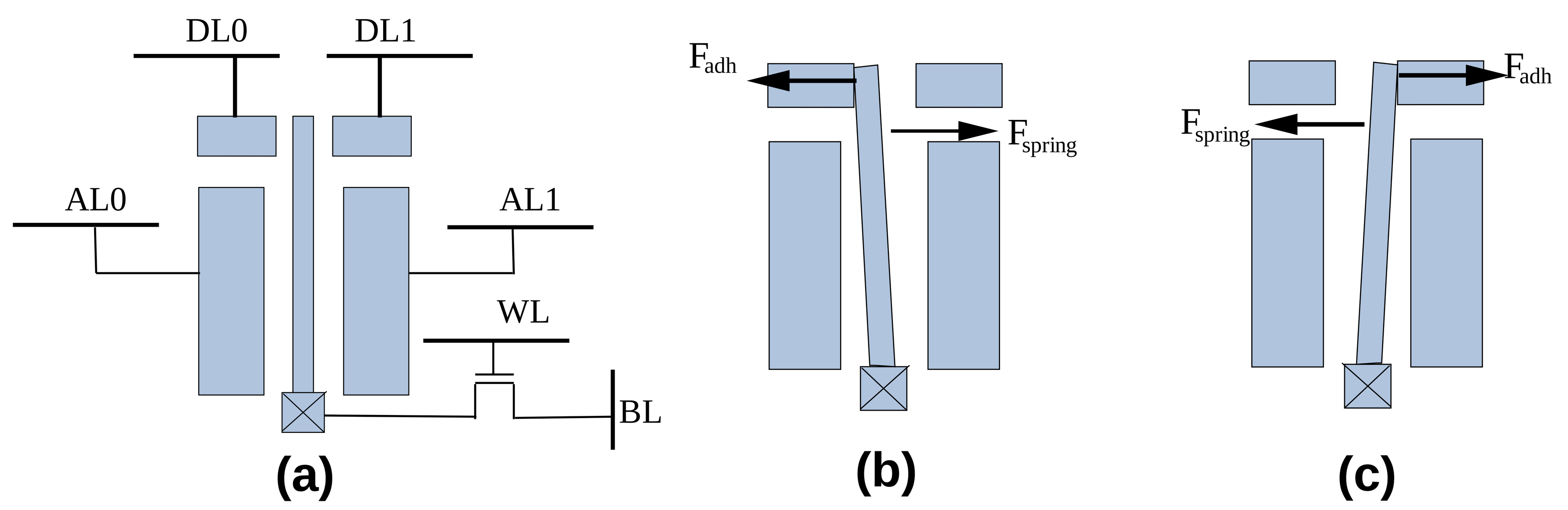

Fig. 1: (a) NEMory cell structure (b) NEM switch in "0" state (c) NEM switch in "1" state

- **NEMory cell comprises a vertically oriented beam, programmed to touch either data line: DL0 ("0" state) or DL1 ("1" state)**
- **To program the cell, a voltage (V_{prog}) is applied to either AL0 or AL1, bit line (BL) is pulsed low, and word line (WL) is pulsed high.**

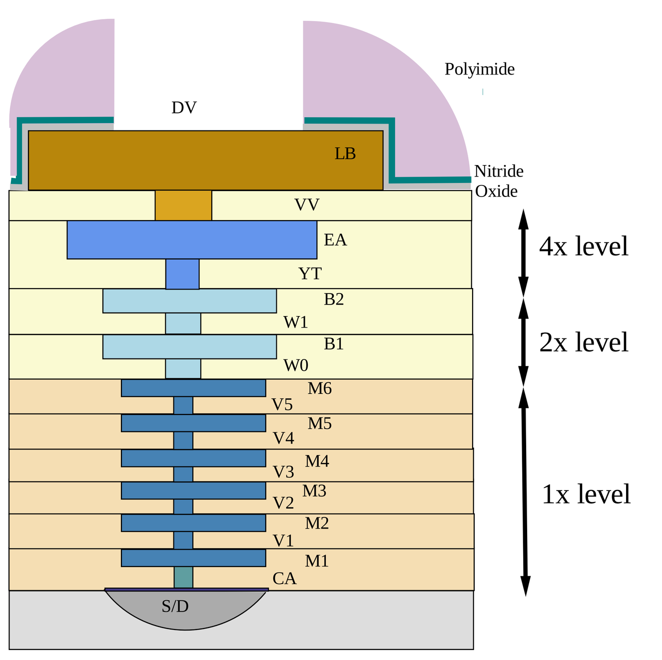

Fig. 2: Schematic cross-section of BEOL layers in 65 nm CMOS process

- **By implementing the NEM switch in BEOL layers, low-cost integration with CMOS and small cell area (footprint) can be achieved.**
- **In this work, multiple 1X metal layers, with minimum feature size and spacing of 100 nm, are used to implement the NEM switch.**
- **The vertically oriented beam is released by anisotropic and isotropic etching of the surrounding inter-metal dielectric material.**

BEOL NEM Switch Design Trade-Offs

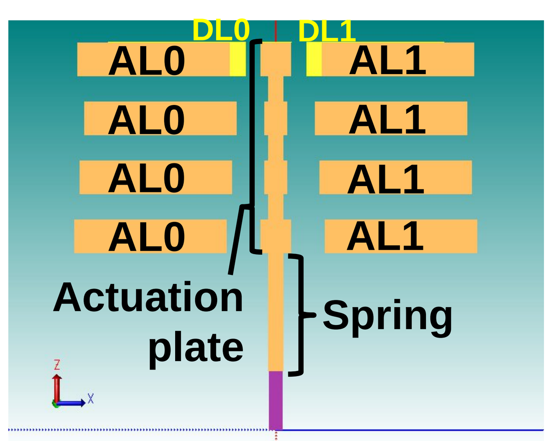

Fig. 3: Cross-sectional view of simulated SPDT NEM switch structure, from MEMS+

- **Reduction in spring stiffness provides for lower pull-in voltage (V_{PI}), but increases the likelihood of catastrophic pull-in to AL0/AL1.**
- **The actuation plate should be stiffer to reduce the possibility of catastrophic pull-in, but this increases the mass, resulting in slower switching speed.**
- **A larger actuation gap for the bottom AL layers results in reduced oscillation upon contact, but at the trade-off of increased V_{PI}.**

Design Optimization Approach

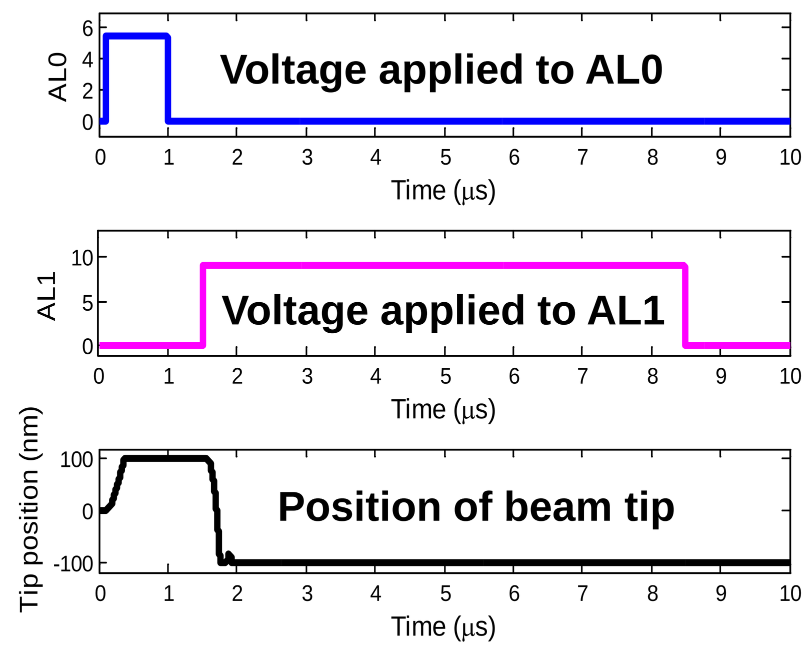

Fig. 4: Transient simulation waveforms of cell programming and reprogramming operations.

Parameter	Values
Stiffness, k_{eff}	0.37 N/m
Contact gap, g_d	100 nm
Contact area	100 nm × 220 nm
Actuation area	20 µm × 220 nm
Actuation gap, g_0	180 to 250 nm
Adhesive force, F_{adh}	45 nN
$V_{PI,program}$	5.5 V
$V_{PI,reprogram}$	9.0 V

- **For non-volatile operation, contact adhesive force (F_{adh}) must be greater than the beam's spring restoring force (F_{spring}).**
- **For reprogramming capability, the electrostatic force (F_{elec}) must be greater than $F_{adh} - F_{spring}$. To minimize F_{elec} and hence the switching energy, $F_{spring} \cong F_{adh}$.**
- **To reduce the possibility of catastrophic pull-in:**
  - **Add vias between actuation plate layers to reduce torsional motion**
  - **Make actuation plate thicker in M3 and M6 layers**

Results and Discussion

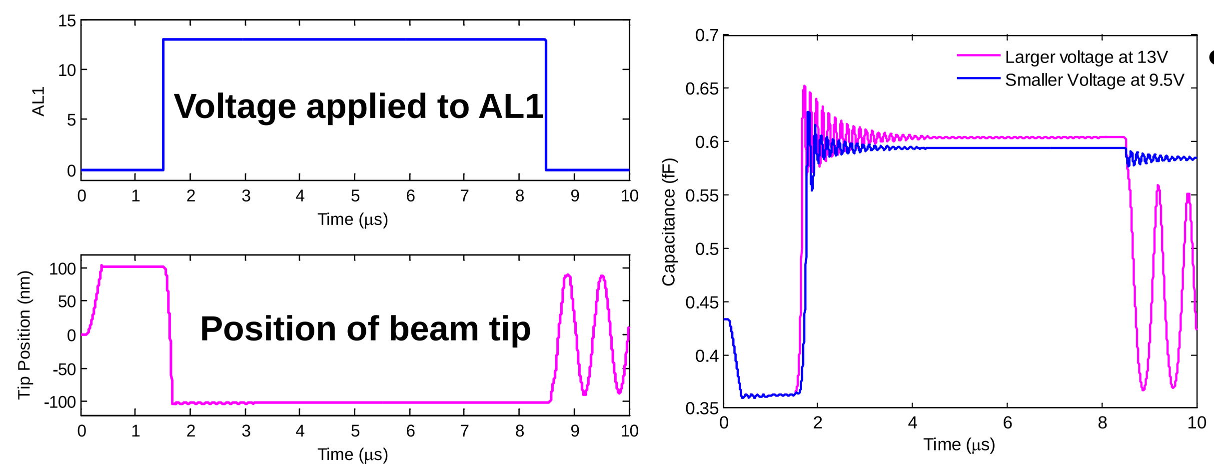

Fig. 5: Transient simulations of cell reprogramming failure.

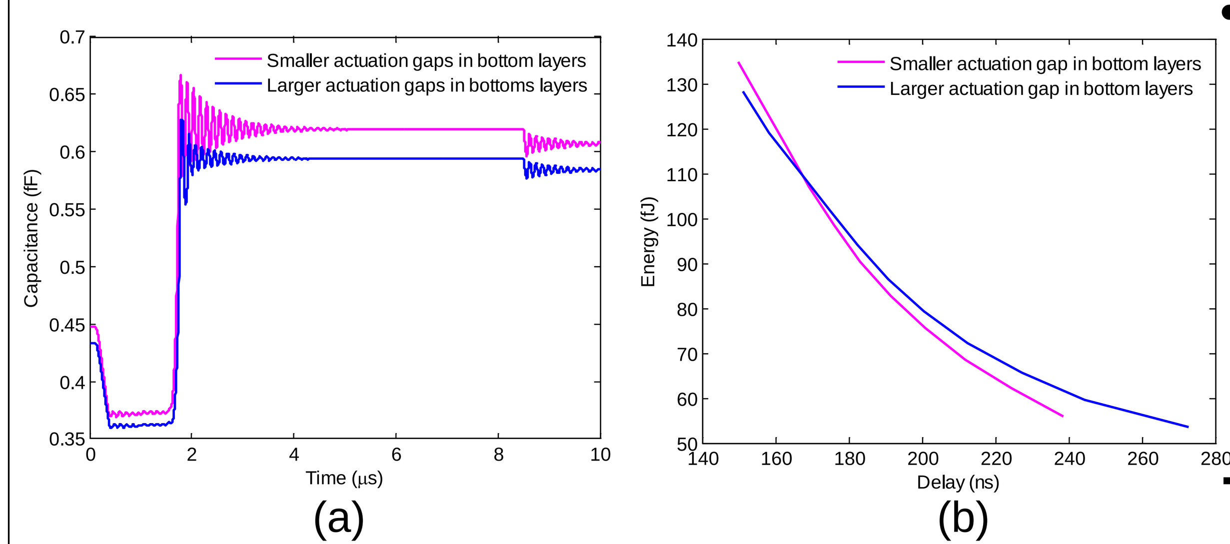

Fig. 6: Effects of bottom actuation gap size: (a) transient beam capacitance for V_{prog} = 9.5 V, (b) energy *vs.* delay.

- **Beam oscillation must cease before V_{prog} is removed for successful reprogramming.**
  - **Larger overdrive (higher contact velocity) results in stronger oscillation.**
- **To reduce oscillation upon contact:**
  - **Make actuation plate narrower in M4 and M5 layers**
  - **Use larger actuation gaps at bottom (M3)**

→Energy × delay product increases.

Summary

- **Design guidelines for SPDT NEM switch design to achieve non-volatile operation with minimum energy × delay are developed.**
- **A stiffer actuation plate is advantageous for avoiding catastrophic pull-in, at a tradeoff of longer switching delay.**

Reference:
[1] K. Kato *et al.*, "Non-Volatile Nano-Electro-Mechanical Memory for Energy-Efficient Data Searching," *IEEE Electron Device Letters*, vol. 37, no. 1, pp. 31-34, 2016.

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