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Three-Terminal CNT NEM Relays

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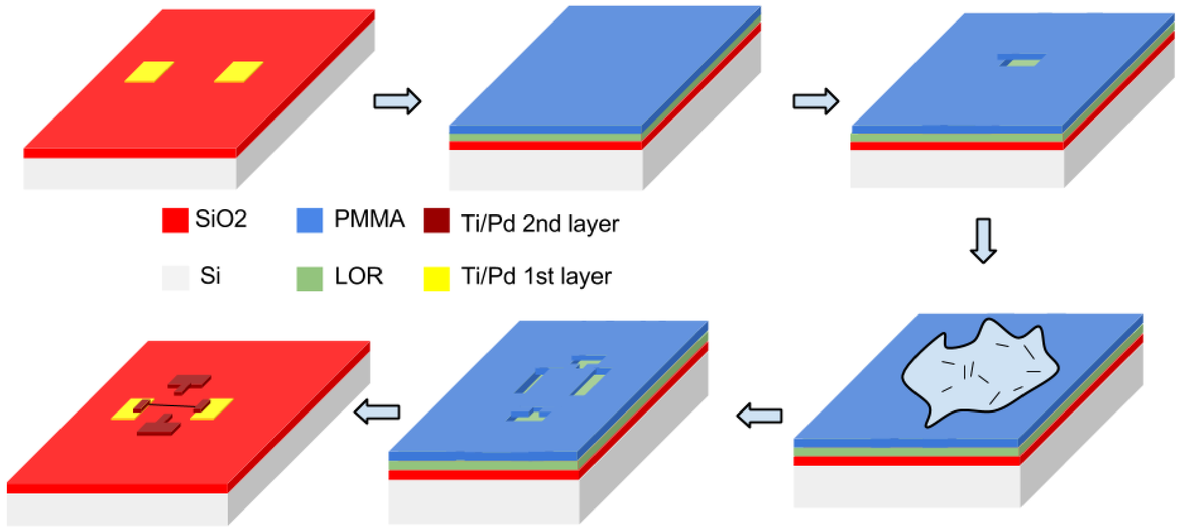
Abstract

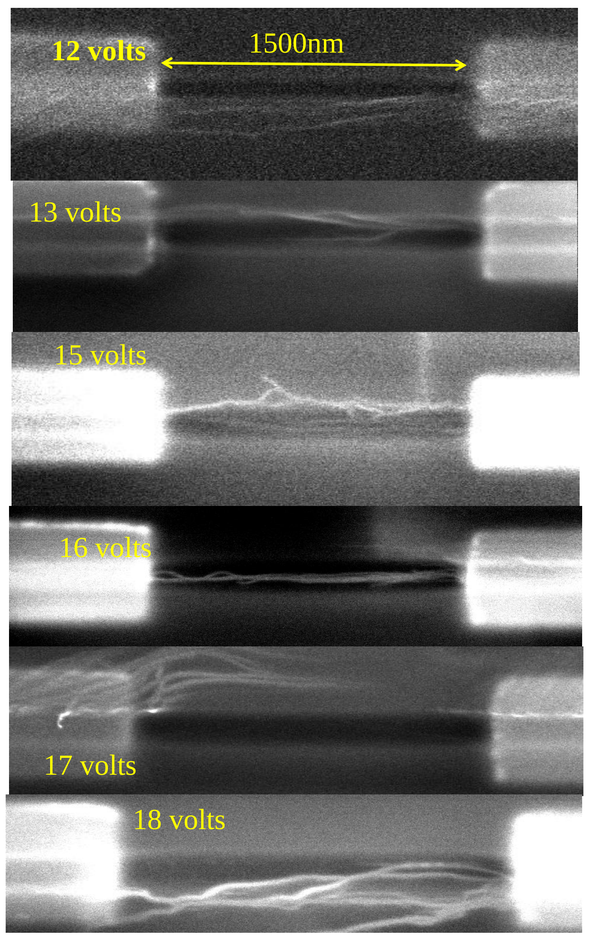
Design and fabrication of new low-power computing systems are of great interest and importance. By applying low van der Waals materials, carbon nanotube (CNT) relays are promising nano-electro-mechanical (NEM) devices due to CNTs' low mass, small dimension, high Young's modulus, and high current density. The CNT clamped-clamped relays have been fabricated using a bottom-up integration scheme, where single-walled metallic CNTs are self-aligned into electron-beam resist trenches using ac-dielectrophoresis (DEP). This research investigates a three-terminal CNT relay fabrication process and electrical measurements for use in low-power computing.

Resist-Assisted Dielectrophoresis Process



1. Electrodes are patterned onto the substrate for CNT deposition
2. Two layers of resist: PMMA (e-beam resist) and LOR (photo resist) are placed on the substrate
3. A trench is patterned into the top layer of the resist using e-beam lithography, the bottom layer is left to keep the CNT suspended
4. An AC voltage is applied across the electrodes while pulling the CNTs in solution into the trench (AC dielectrophoresis)
5. A new PMMA resist layer is applied, e-beam lithography and metal CVD are used to clamp the CNT in place
6. Resist is lifted, device is dried in critical point dryer

Optimizing the Dielectrophoresis Parameters



SEM images comparing deposition results for different AC peak-to-peak voltages at a deposition time of 50 s and 5 MHz frequency showed that:

15 and 16 volts were optimal for pulling CNTs into the trench.

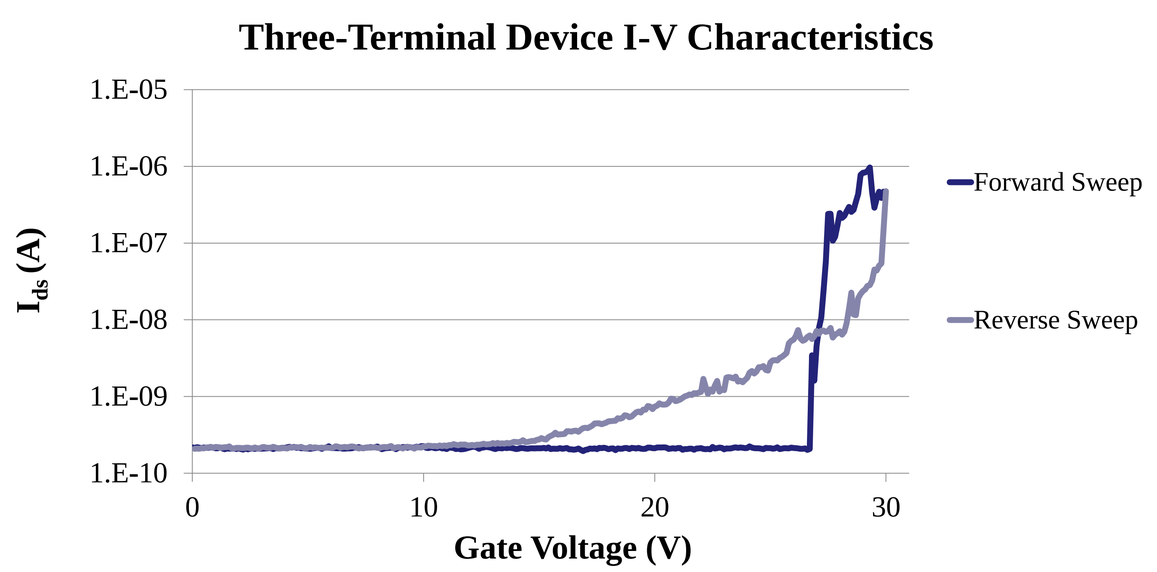
Higher voltages attracted too many CNTs, while lower voltages failed to pull CNTs into the trench at all.

Final Well-Aligned Devices

16 V_{pp}, 50 s deposition time, 5 MHz

15 V_{pp}, 50 s deposition time, 5 MHz

Electrical Characterization



Pull-in Voltage: 27.2 V

Leakage Current: $2.2 \cdot 10^{-10}$ A

I_{on}/I_{off}: 10^3

Conclusions and Future Work

Three-terminal CNT relays were demonstrated and electrically characterized. Future work can explore new device configurations for further computing applications such as logic gating.

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