Tunnel FET research in the EU STEEPER project

Adrian M. Ionescu, EPFL

2nd Berkeley Symposium on Energy Efficient Electronic Systems
Summary

• Introduction:
  – energy efficient steep slope devices
  – Tunnel FETs
• Objectives of STEEPER
• Partnership
• Workplan
• Highlights per workpackage
• Conclusion
• Power per chip continues increasing.
• Leakage power dominates in advanced technology nodes.
• $V_T$ scaling saturated by 60mV/dec physical limit.
• Voltage scaling slowed, 90nm=1.2V, 45nm=1V, 22nm=0.8V

Reducing threshold voltage by 60mV increases the leakage current (power) by ~10 times.

Performance metrics: $I_{ON}$, $I_{ON}/I_{OFF}$, $S$, $V_T$, $V_{dd}$, $\tau$

$\tau = \Delta Q/I_{eff}$

Adapted after: D. Antoniadis & C. Hu

Source: Intel Corporation
Average subthreshold swing & Vdd

\[ S_{avg} = \left( V_T - V_{Goff} \right) / \log \left( I_T / I_{off} \right) \approx V_{dd} / \log \left( I_{on} / I_{off} \right) \]

(mV/decade)
Energy, voltage supply and swing

\[ E_{total} = E_{dynamic} + E_{leakage} = \alpha L_d CV_{dd}^2 + L_d I_{off} V_{dd} \tau_{delay} \approx \]

\[ \approx \alpha L_d CV_{dd}^2 + L_d CV_{dd} \frac{I_{off}}{I_{on}} = \]

\[ = L_d CV_{dd}^2 (\alpha + \frac{I_{off}}{I_{on}}) \approx L_d CV_{dd}^2 (\alpha + 10^{-V_{dd}/S}) \]

\[ P = \alpha L_D CV_{dd}^2 f + I_{off} V_{dd} \approx KCV_{dd}^3 + I_{off} V_{dd} \]

a technology that would enable a voltage scaling by a factor of 5 (from 1 V to 0.2 V) with a negligible leakage power (with ultra-low \( I_{off} \) due to a small \( S \), as the TFET) could offer a power dissipation reduction of 125x.
CMOS has a fundamental lower limit in energy per operation due to subthreshold leakage: \( (V_{dd\min}, E_{min}) \)

Parallelism (multi-core) is a key technique to improve system performance under a power budget.


Source: T.J. King, UC Berkeley.

STEEPER @ UC Berkeley, November 2nd, 2011
Subthermal swing switches

Tunnel FET vs. future FET

Tunnel FET is the most promising small swing switch for $V_{dd}$ scaling.
Tunnel FET in ITRS-ERD 2009

Scalability → Performance

1. CMOS Architectural Compatibility
2. CMOS Technological Compatibility
3. Tunnel MOSFETs

Energy Efficiency → Gain → Operational Temperature → Operational Reliability
**Objectives (1)**

**General**

- **OBJ 1**: Demonstrate energy efficient steep subthreshold slope transistors based on quantum mechanical band-to-band tunneling (tunnel FETs) able to **reduce the voltage operation of advanced nanoelectronic circuits into sub-0.5V** and their **power consumption by one order of magnitude**.

- **OBJ 2**: Enable and demonstrate the power consumption benefits resulting from **hybridization of tunnel FET and CMOS technologies** and from tunnel FETs as stand-alone technology for digital, analog, RF and mixed-mode circuit applications.

**Technology**

- **OBJ 3**: Develop a **CMOS-compatible UTB SOI technology platform for tunnel FETs** with ultra-low standby power by exploiting key additive boosters for enhanced performance: high-k dielectrics, SiGe source, strain.

- **OBJ 4**: Study and identify advanced technology implementations for **high-Ion tunnel FETs**: III-V materials, nanowires, staggered versus broken band gaps, electrostatic doping.
Simulation and modelling

• **OBJ 5**: Develop accurate **numerical simulation tools**: semi-classical multi-sub-band Monte Carlo simulator and full-band quantum-transport simulation for in-depth study of UTB and nanowire tunnel FETs, respectively.

• **OBJ 6**: Study the **scaling, parameter sensitivity and variability** on the characteristics of nanometer tunnel FETs.

• **OBJ 7**: Develop and implement **DC and AC compact models** for the simulation and design of circuits based on tunnel FETs and or co-design with advanced CMOS.

**Industrial benchmarking: device and circuit**

• **OBJ 8**: **Benchmark tunnel FETs** developed in STEEPER for low standby power logic, high speed, memory, RF and analog applications. Evaluate their energy efficiency against CMOS.
<table>
<thead>
<tr>
<th>Beneficiary no.</th>
<th>Beneficiary legal name</th>
<th>Country</th>
<th>Type of Beneficiary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (Coord.)</td>
<td>Ecole Polytechnique Fédérale de Lausanne (EPFL)</td>
<td>CH</td>
<td>University</td>
</tr>
<tr>
<td>2</td>
<td>Commissariat à l’Energie Atomique - Laboratoire d’Electronique et de Technologie de l’Information (CEA-LETI)</td>
<td>FR</td>
<td>Research centre</td>
</tr>
<tr>
<td>3</td>
<td>Consorzio Nazionale Interuniversitario per la Nanoelettronica (IUNET)</td>
<td>IT</td>
<td>University</td>
</tr>
<tr>
<td>4</td>
<td>Global Foundries (GF)</td>
<td>DE</td>
<td>Industrial</td>
</tr>
<tr>
<td>5</td>
<td>IBM Research GmbH, Zurich Research Laboratory (IBM-ZRL)</td>
<td>CH</td>
<td>Industrial</td>
</tr>
<tr>
<td>6</td>
<td>Infineon Technologies (INFINEON) Intel Mobile Communications (IMC)</td>
<td>DE</td>
<td>Industrial</td>
</tr>
<tr>
<td>7</td>
<td>Research Center Juelich (FZJ)</td>
<td>DE</td>
<td>Research centre</td>
</tr>
<tr>
<td>8</td>
<td>SCIPROM Sàrl (SCIPROM)</td>
<td>CH</td>
<td>SME</td>
</tr>
<tr>
<td>9</td>
<td>Technische Universität Dortmund (TU-D) Aachen</td>
<td>DE</td>
<td>University</td>
</tr>
</tbody>
</table>
WP1: Silicon-On-Insulator platform
- Silicon Tunnel FET
  • UTB Si channel
  • High-k/metal gate
  • SiGe source
  • Strain
  • Optimized fringing
  • Nanowire

WP2: III-V nanowire platform
- III-V NW Tunnel FET
  • Si/III-V on Si
  • all-III-V on Si
  • Bandgap eng.
  • Strain

WP3: Modelling and simulation
- Device & technology specifications
  - Semiclassical transport simulator
  - Quantum-transport simulator
  - Compact models
  - Mixed device-circuit simulations

WP4: Physical challenges and novel concepts for the optimization of tunnel FETs
- Bandgap eng.
- Strain
- Electrost. doping
- Scalling, sensitivity

WP5: Benchmarking and integration of tunnel FETs with nano-CMOS
- Digital, analog/mixed circuit cells:
  - Hybrid CMOS/Tunnel FET
  - Tunnel FETs
Fundamental technology boosters

\[ I_{BTB} \propto T_{WKB} \approx \exp \left( -\frac{4\lambda \sqrt{2m^*E_g^{1.5}}}{3\hbar(\Delta \Phi + E_g)} \right) \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Means of improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>( m^* )</td>
<td>Small effective tunnel mass, SiGe, III-V, CNT</td>
</tr>
<tr>
<td>( E_G )</td>
<td>Source in SiGe, III-V heterostructures, strain CNT</td>
</tr>
<tr>
<td>( \lambda )</td>
<td>3D geometry (wrap gate), high-k gate dielectric, thin gate dielectric</td>
</tr>
</tbody>
</table>

Source: IBM
Additive techno boosters on CEA-LETI’s UTB SOI in Steeper

STEPPER DEVICES

- **III-V NW**
- **Si NW**
- **UTB SOI, SiGe source**

‘A’: base device

‘B’: Like A with high-k dielectric.

‘C’: Like B with narrower junction.

‘D’: Like ‘C’ with thinner body.

E: Like ‘D’ with higher source doping.

‘F’: Like E with double gate.

‘G’: Like ‘F’ with oxide over intrinsic region.

‘H’: Like ‘G’ with shorter length.

‘J’: Like ‘H’ with bandgap $E_g = 0.8$ eV at the tunnel junction.
Technology boosters + contact engineering. Various types of substrates studied.

Source: Cyrille Le Royer: CEA-LETI @ IEDM 2008 & ULIS 2010.

Drain current $I_D$ (A/µm) vs. $V_{GS}$ (V) and $V_{GD}$ (V) for p-channel and n-channel operation.

$V_{DS} = -1V$
-0.8V
-0.6V
-0.4V
-0.2V
-0.1V

$V_{SD} = +1V$
+0.8V
+0.6V
+0.4V
+0.2V
+0.1V

$S = 42$ mV/dec

Source: Cyrille Le Royer: CEA-LETI @ IEDM 2008 & ULIS 2010.
Importance of implant optimization

- Ion=46μA/μm and $I_{\text{OFF}}$ of 5pA/μm at $V_{\text{DD}}$=-1.2V demonstrated for narrow fin Tunnel FETs by IMEC.

- Implant optimization study carried out: spike anneal (‘SPIKE’), sub-ms laser anneal (‘LA’) and low temperature anneal for Solid Phase Epitaxy Regrowth (‘SPER’).

State-of-the-art: Ge-source

Ion ~ 300μA/μm @ Vd=3V
Ion ~ 10μA/μm @ Vd=1V
Ion ~ 0.2μA/μm @ Vd=0.5V
S=50mV/dec


Ion/Ioff ~3.10^6 @ Vdd=0.5V

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tox (nm)</td>
<td>Si TFET</td>
<td>SiGe TFET</td>
<td>s-Ge TFET</td>
<td>Ge TFET</td>
</tr>
<tr>
<td>Lg (nm)</td>
<td>70</td>
<td>100</td>
<td>1000</td>
<td>5000</td>
</tr>
<tr>
<td>@ Vd (V)</td>
<td>1</td>
<td>1.2</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>ION (μA/μm)</td>
<td>12.1</td>
<td>0.009</td>
<td>0.001</td>
<td>0.42</td>
</tr>
<tr>
<td>IOFF (μA/μm)</td>
<td>5400</td>
<td>8</td>
<td>0.3</td>
<td>0.12</td>
</tr>
<tr>
<td>ION/IOFF for Vdd=0.5V</td>
<td>6E3</td>
<td>3E3</td>
<td>4E4</td>
<td>3E6</td>
</tr>
</tbody>
</table>

S. Kim, H. Kam, C. Hu and T.-J. King Liu, VLSI 2009.
WP1 highlights in Y1 (1)

WP1: Silicon-On-Insulator technology platform

Highlight 1 (CEA-LETI): Integration of aggressive tunnel FET technology boosters in dedicated lots

- **Lot 2.0:**
  - Ultrathin SOI (~7nm)
  - HK-MG (EOT 1.18nm)
  - Si & Si$_{0.7}$Ge$_{0.3}$ Raised S-D

- **Lot 2.1:**
  - Si/SiGe/SOI (~8nm)
  - HK-MG
  - Si & Si$_{0.7}$Ge$_{0.3}$ Raised S-D

- **Lot 2.2:**
  - Ultrathin SOI (~7nm)
  - Trigate, HK-MG
  - Si$_{0.7}$Ge$_{0.3}$ Raised S-D
Strain as performance booster

1) e-beam lithography
2) RIE
3) oxidation

- tensile y-strain maintained
- lateral x-strain relaxed

Uniaxial tensile strained NW

STEEPER @ UC Berkeley, November 2nd, 2011
Highlight 2 (FZJ): Nanowire array TFETs with TiN/HfO$_2$ gate stack, sSi (strained silicon) NW: height 15nm, width 50nm, 5nm HfO$_2$ (ALD), $L_G$=100nm – functional.
WP 2: Technology Development for III-V Tunnel FETs on a Silicon Platform

Highlight 1 (IBM-ZRL): Growth established, tuned, characterized
- epitaxial growth of InAs nanowires on Si platform without the use of a catalyst material and with high yield.
- abrupt and high quality InAs-Si interface
Highlight 2 (IBM-ZRL): InAs-Si heterostructure diodes fabricated and characterized

- band alignment of InAs-Si heterostructure: small effective bandgap $E_{g,\text{eff}} = 220$ meV
WP3: Modeling and simulation

Semiclassical transport model
(task 3.1)

- Main features:
  - 2D semiclassical transport
  - Multi Subband Monte Carlo
  - Various scattering mechanisms

- Main applications:
  - UTB SOI
  - SiGe, Strain
  - Crystal orientations

Model Verification
Calibration
Benchmarking
(task 3.4)

- Main features:
  - based on exp. data, atomistic simul, templates

Quantum transport model
(task 3.2)

- Main features:
  - 3D quantum transport
  - Energy dispersion relation
  - Ballistic transport, phonon scatt.

- Main applications:
  - Nanowires
  - III-V materials (on Si)
  - Heterojunctions

Compact models and mixed device-circuit simulations
(tasks 3.3, 3.5)

- Main application:
  - Investigate devices in a circuit environment
WP3: Modelling and simulation

**Highlight 1 (IUNET):** Semi-Classical Transport model - Multi-subband MC:

- Can account for 2D quasi-ballistic transport, vertical quantization and 2D electrostatics
- Models for high-k, strain, SB, alternative materials already in place

Tunnel FET $L=20\text{nm}$

$N_{A,\text{SOURCE}} = 5 \times 10^{19} \text{ cm}^{-3}$

Intrinsic Channel

$N_{D,\text{DRAIN}} = 5 \times 10^{19} \text{ cm}^{-3}$

---

Graph showing $I_{DS}$ vs $V_{GS}$ with $V_{DS} = 1.5\text{V}$ and line labels:

- Sentaurus
- Integral Gen. Rate
Highlight 2 (IUNET): Preliminary version of a ballistic, full-quantum transport for direct bandgap nanowire Tunnel-FETs - eight-band $k^*\rho$ Kane’s model, accurate for direct band-gap semiconductors, implemented.

IUNET-IBM: Benchmarking against measurements: Si-InAs heterojunction Esaki diode (D=120 nm)
WP4: Physical challenges and novel concepts for the optimization of tunnel FETs

Highlight 1 (TuD/Aachen): Study of heterostructures as performance booster of tunnel FETs
New energy filtering devices

- to achieve sub-60mV/dec tunnel FET must operate as band-pass filter
- effective cooling of source Fermi distribution function

filter action can be achieved with band structure engineering

use superlattice structure to form miniband

Highlight 2 (IUNET): New energy filtering device: use superlattice structure to form miniband – benchmarking against CMOS specs performed

New electron-hole bilayer TFET

- body doping: \( N_D = 1 \times 10^{15} \text{ cm}^{-3} \)
- lateral S/D doping decay: \( x_{dec} = 5 \text{ nm/dec} \)
- back gate and drain bias: \( V_{BG} = -0.1 \text{ V} \) and \( V_{D} = 1.0 \text{ V} \)
- dynamic non-local path BTBT model (phonon-assisted)
Highlight 3 (EPFL): Novel concept of Electron-Hole bilayer tunnel FET (Si and Ge implementations)

- $I_{OFF} \sim 1 \text{ fA/\mu m}$ (Shockley-Read-Hall)
- $I_{ON} \sim 0.16 \text{ \mu A/\mu m } @ V_G = V_D = 1.0 \text{ V}$
- $SS_{AVG} \sim 12 \text{ mV/dec}$ (over 6 decades)

STEEPER targets: C-TFET on all-silicon and InAs/Ge

- all-Si CTFET UTB SOI as LSTP design option on SOI CMOS
- InAs/Ge CTFET as low power replacement option
The Ge/InAs C-TFET has the most abrupt transition from the 1 to the 0 state with the highest differential gain, \( \frac{dV_{\text{OUT}}}{dV_{\text{IN}}} \) (inset) and best noise margins.
Possible roadmap

- High-k/metal gate
- Multi-gate
- III-V
- Tunnel FETs

CMOS (FET)

Beyond CMOS

- sub-1V
- sub-0.8V
- sub-0.5V
- sub-0.25V

See CEA-LETI work.
See IMEC work.
See IBM work.
Conclusions (1)

- **Opportunities:**
  - Tunnel FET stands as the most promising steep slope switch candidate to reduce the supply voltage below 0.5 V and offer significant power dissipation savings.
  - Because of their low $I_{\text{off}}$, they appear suited for low power and low standby power logic applications operating at moderate frequency (hundreds of MHz).
  - Other promising applications of TFETs: ultra-low power specialized analog integrated circuits with improved temperature stability and low-power SRAM.
  - Hybrid CMOS complementary TFET design, with TFETs as an add-on ultra low power device option on advanced CMOS platforms.
Conclusions (2)

- **Challenges and perspectives:**
  - Achieve high $I_{on}$ without degrading $I_{off}$, combined with a subthreshold swing of less than 60 mV/decade over more than four decades of drain current.
  - Additive combination of specific technology boosters.
  - Carbon materials (graphene and carbon nanotubes) are well-suited for high-performance Tunnel FETs due to their ultra-thin body thickness and their one-dimensional transport characteristics but face enormous challenges for experimental implementation.
  - **Heterostructure Tunnel FETs** offer the best performance compromise for complementary logic through advanced band engineering, using Ge- and InAs-sources on silicon platforms for n- and p-type Tunnel FETs in ultra-thin films or nanowires.