# Design of Sensitive Phototransistor with III-V Nanopillars on Silicon

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**Abstract:** The need for amplifiers in optoelectronic receivers makes these devices highly inefficient. In order to eliminate the need for these amplifiers, a photodetector with internal gain is desired. The use of a III-V bipolar junction phototransistor is the proposed design to realize this internal gain. Integration of such a device with silicon is achieved through nanopillar growth of III-V material on silicon. In order to determine device parameters to yield maximum gain, simulations of the nanopillar HPT BJT device were conducted with Sentaurus Device Simulator. Simulations of a pn diode and npn BJT nanopillar device show a high internal electric field at region junctions, predicting a potential for high gain.

## Introduction

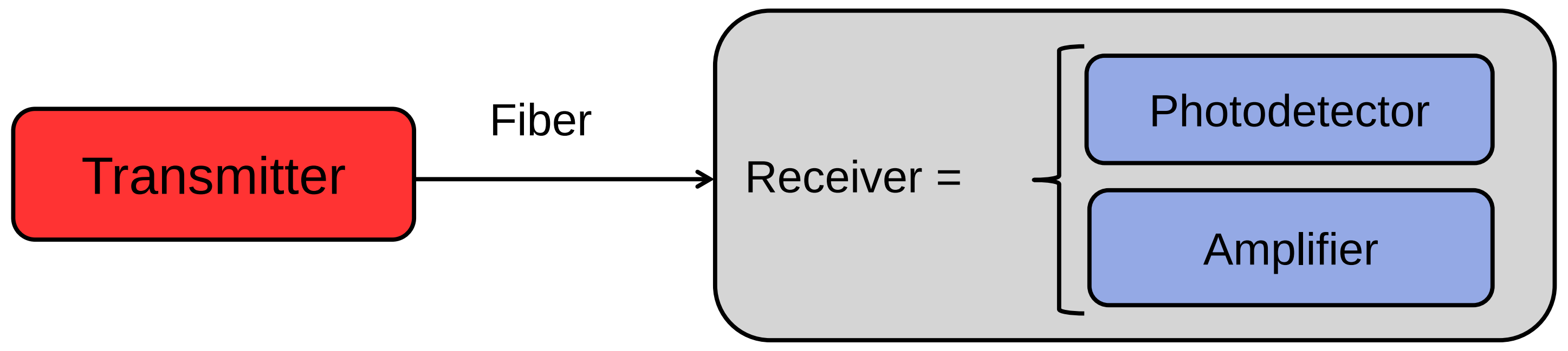
### *Energy Efficient High-speed Optical Interconnects:*

**Problem:**

- Huge power consumption in receiver side from amplifiers used to to recover large enough detected signals

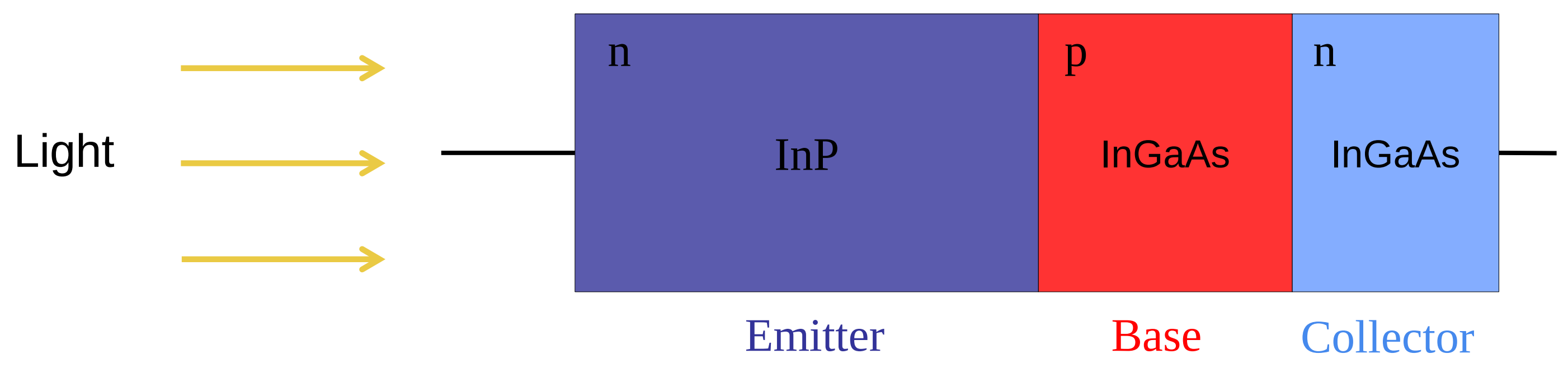
**Proposed Solution:**

- To create a receiver with internal gain, eliminating need for amplifiers

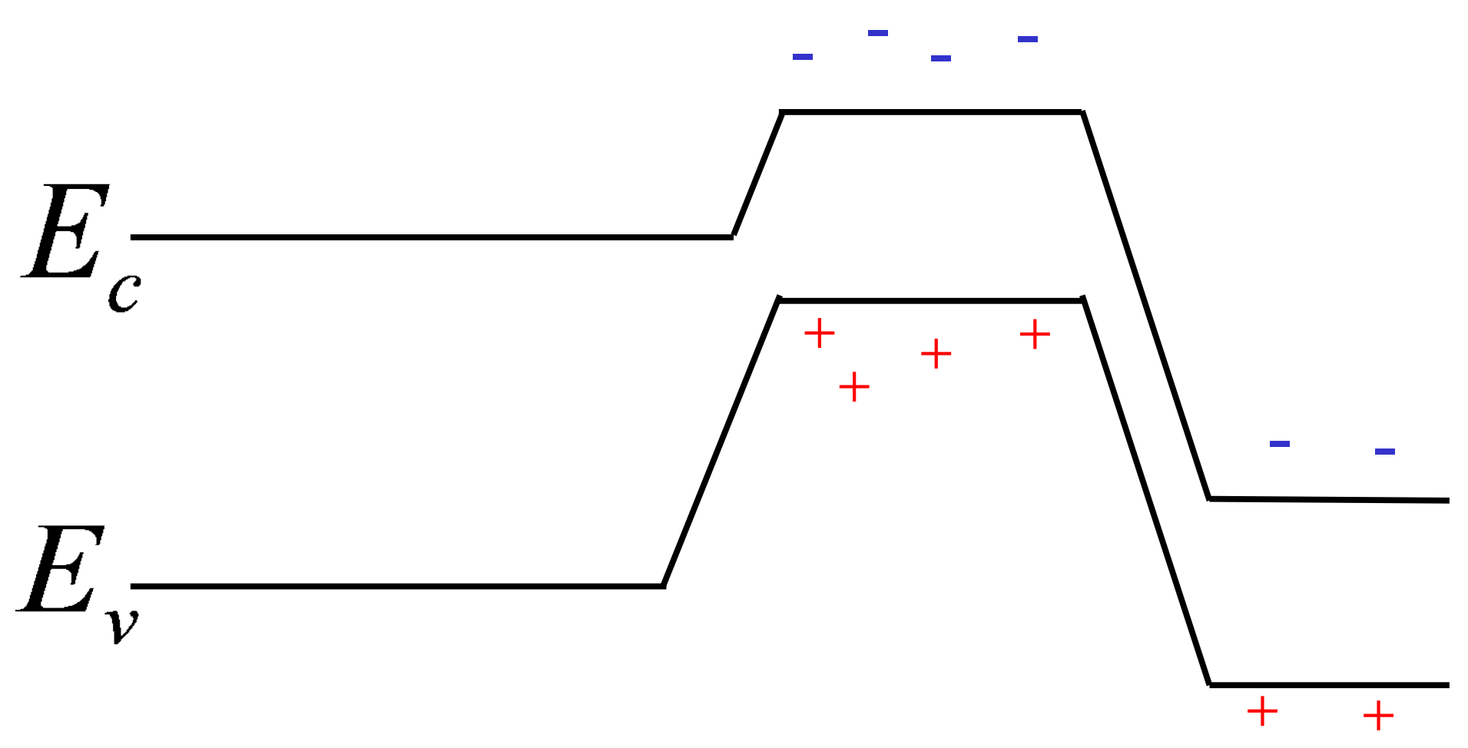


### *III-V Bipolar Junction Phototransistor:*

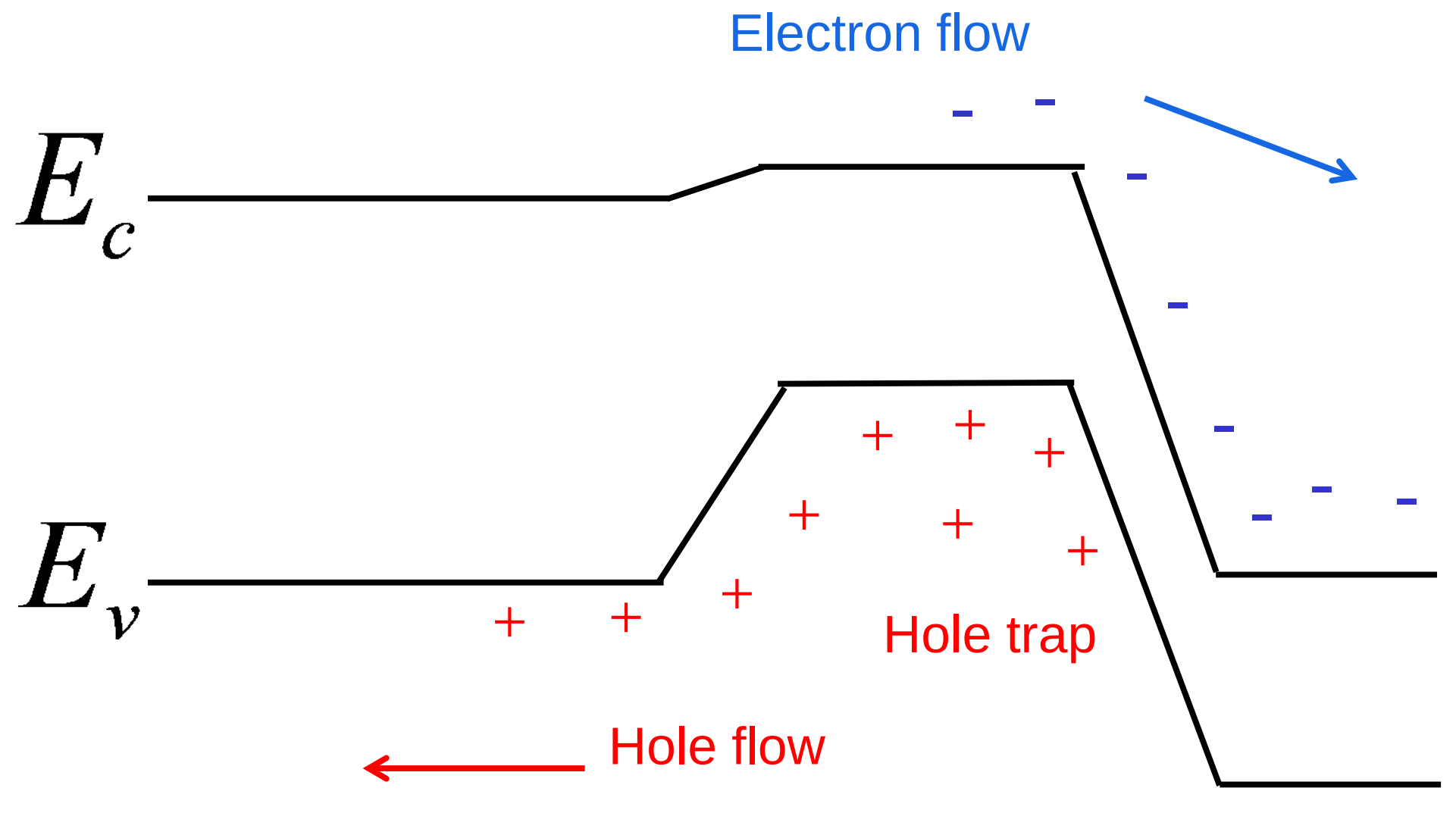
- Has potential for **high internal gain**
- First proposed in the 1980s
- Interest renewed in the design because of its **energy efficiency**



Light with $E_g(InGaAs) < \hbar\omega < E_g(InP)$ induces electron hole pairs in the base and collector



Accumulation of holes in base due to **natural bandgap barrier**, which causes **gain**; holes escape when base band is lowered enough

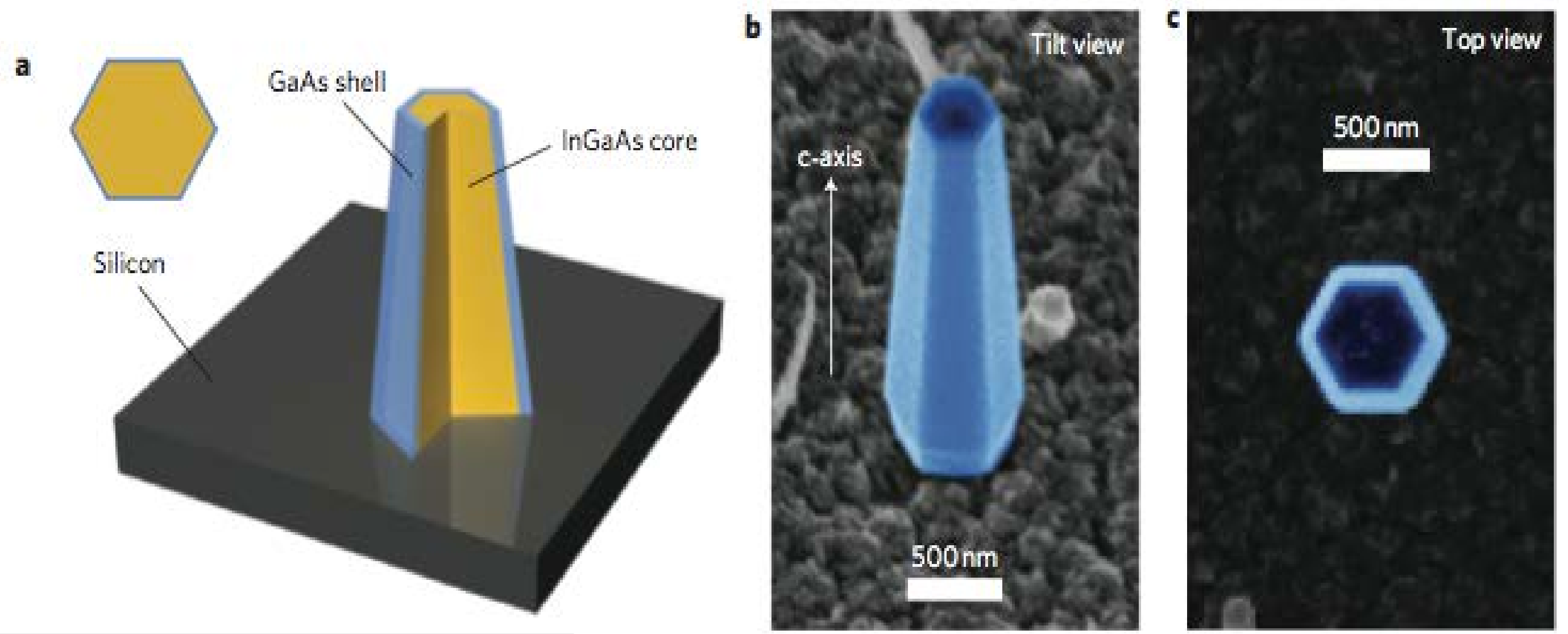


J.C.Campbell et.al. “InP/InGaAs heterojunction phototransistors,” IEEE QE, 1981

## Our Approach

### *III-V Nanopillars Grown on Silicon*

- III-V phototransistor integrated with silicon is desired, to accommodate to silicon-based microelectronic platform
- Professor Connie Chang-Hasnain’s group has demonstrated **III-V nanopillars grown on silicon despite lattice mismatch**
- **Goal** : **design bipolar junction phototransistor built in nanopillar**



R. Chen et.al. “Nanolasers grown on silicon,” nature photonics, 2010

*III-V Nanopillars Grown on Silicon*

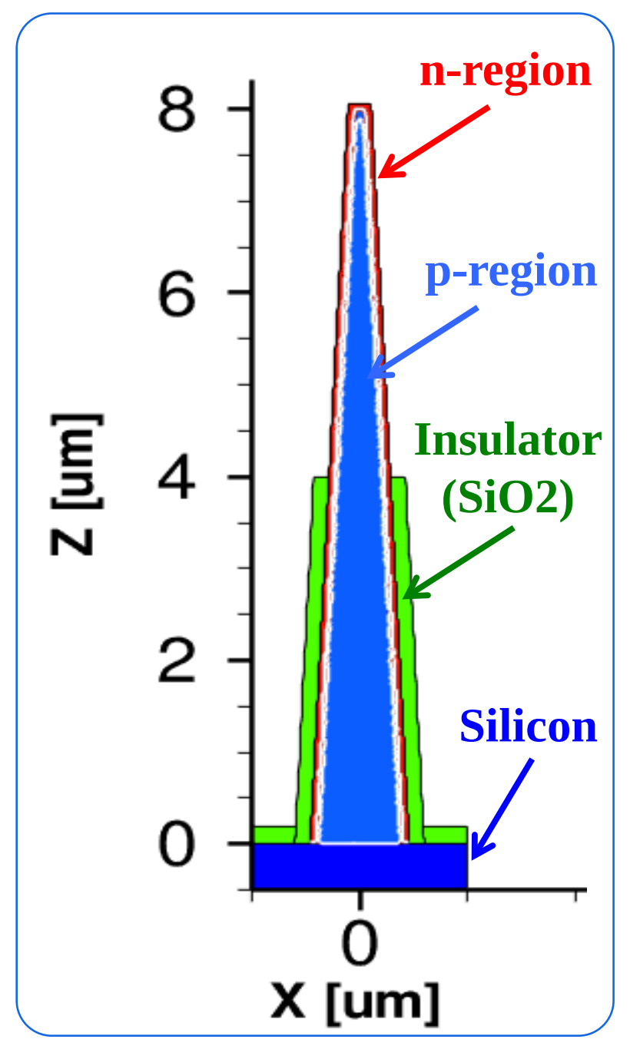
### *Sentaurus Device Simulator*

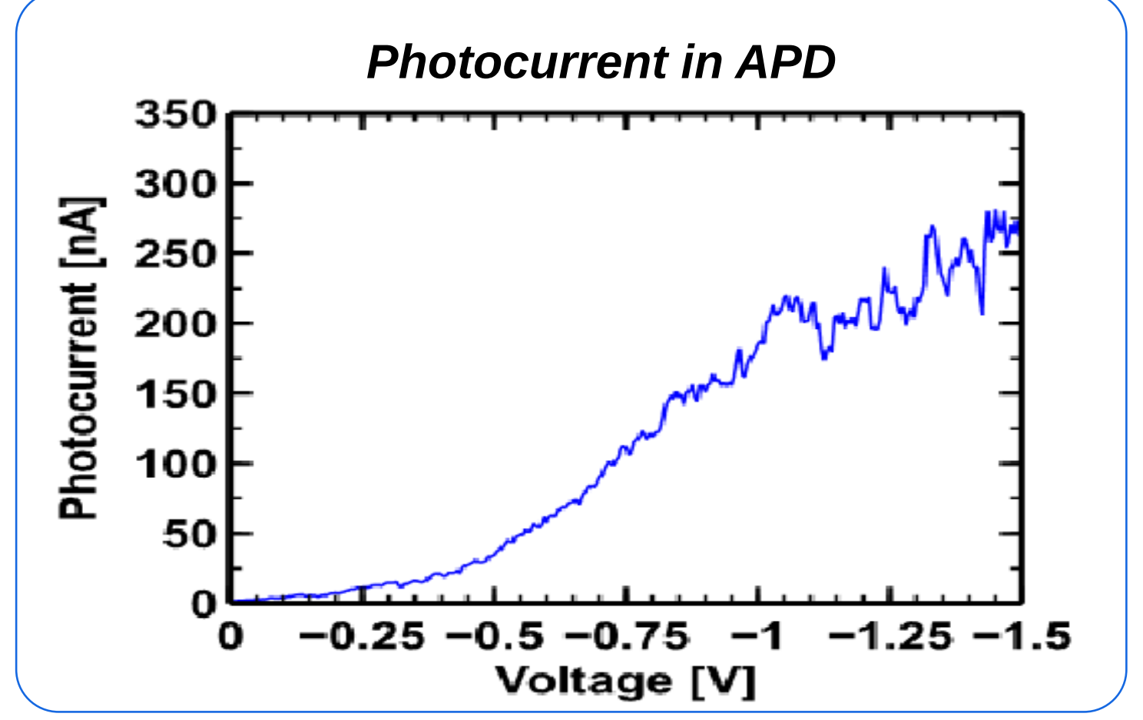
- Tool to simulate device behavior of nanopillar BJT designs
- Takes device parameters as input and returns internal electric field, carrier density, IV curves, etc.
- **Used to examine potential gain and find optimum design**

## Nanopillar pn Diode

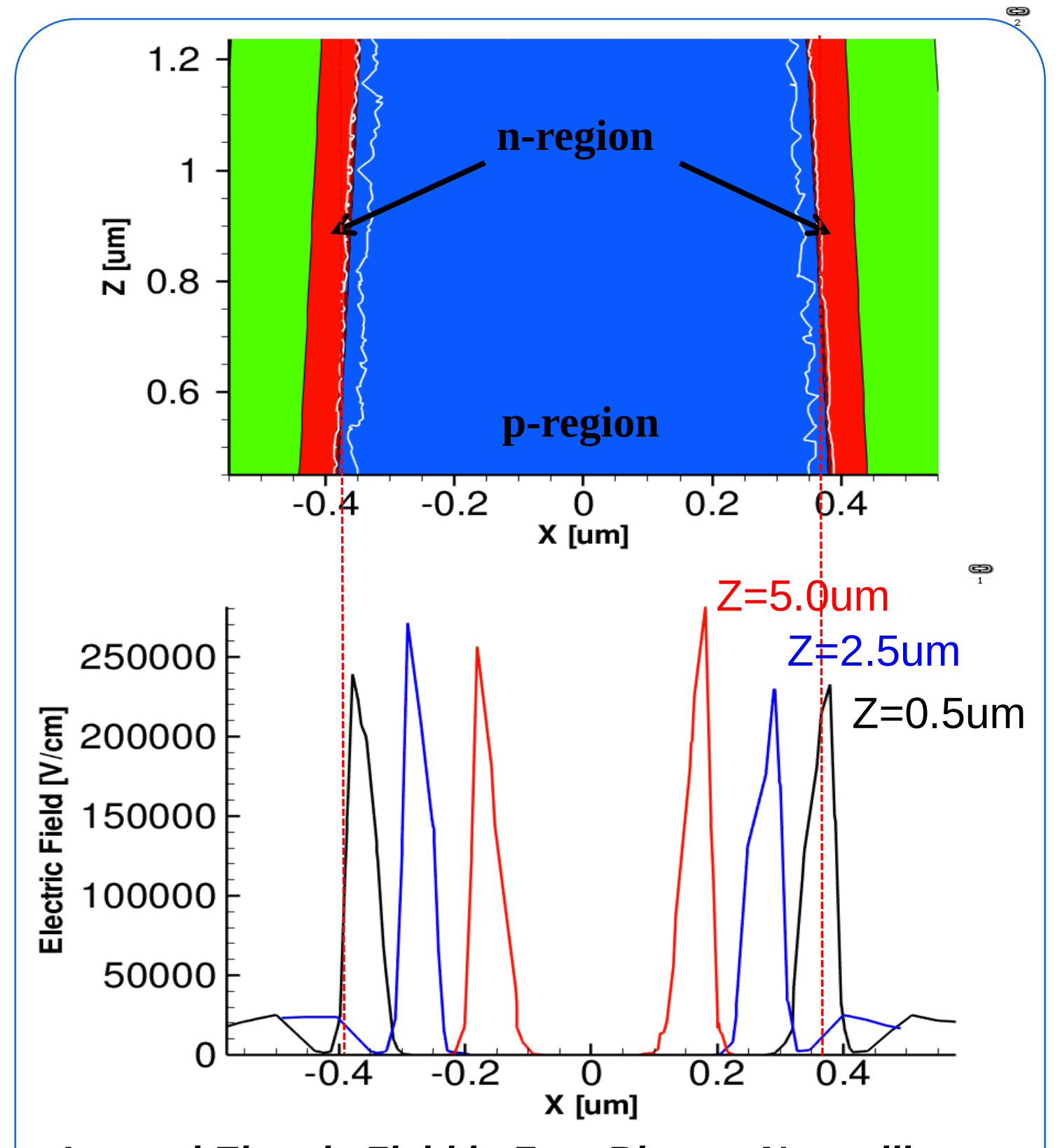
### *Nanopillar Diode Schematic*

- InP pn homojunction
- Simulated to determine internal electric field due to pillar structure





- Measurement result of a real photodetector relates high electric field to high gain

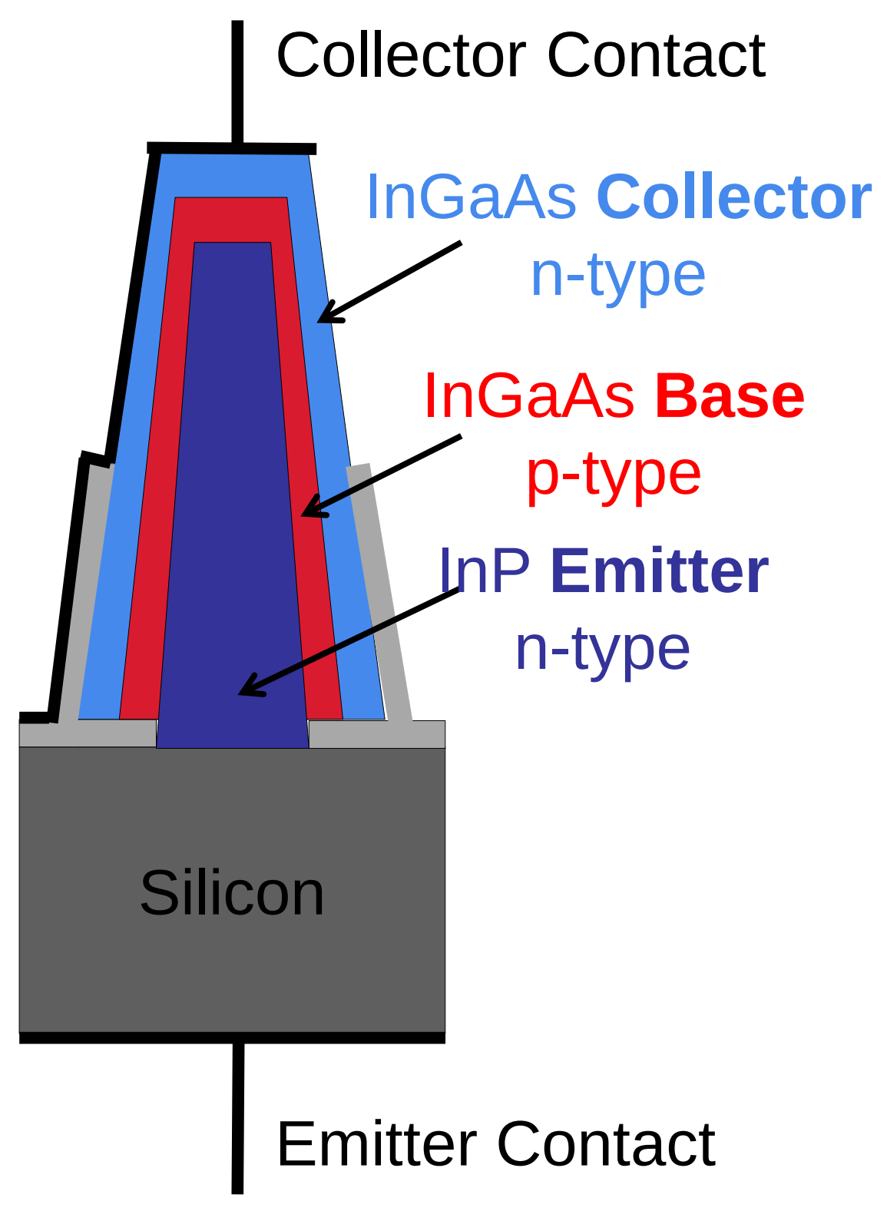


*Internal Electric Field in Zero Bias pn Nanopillar*

### *Electric Field in pn Nanopillar*

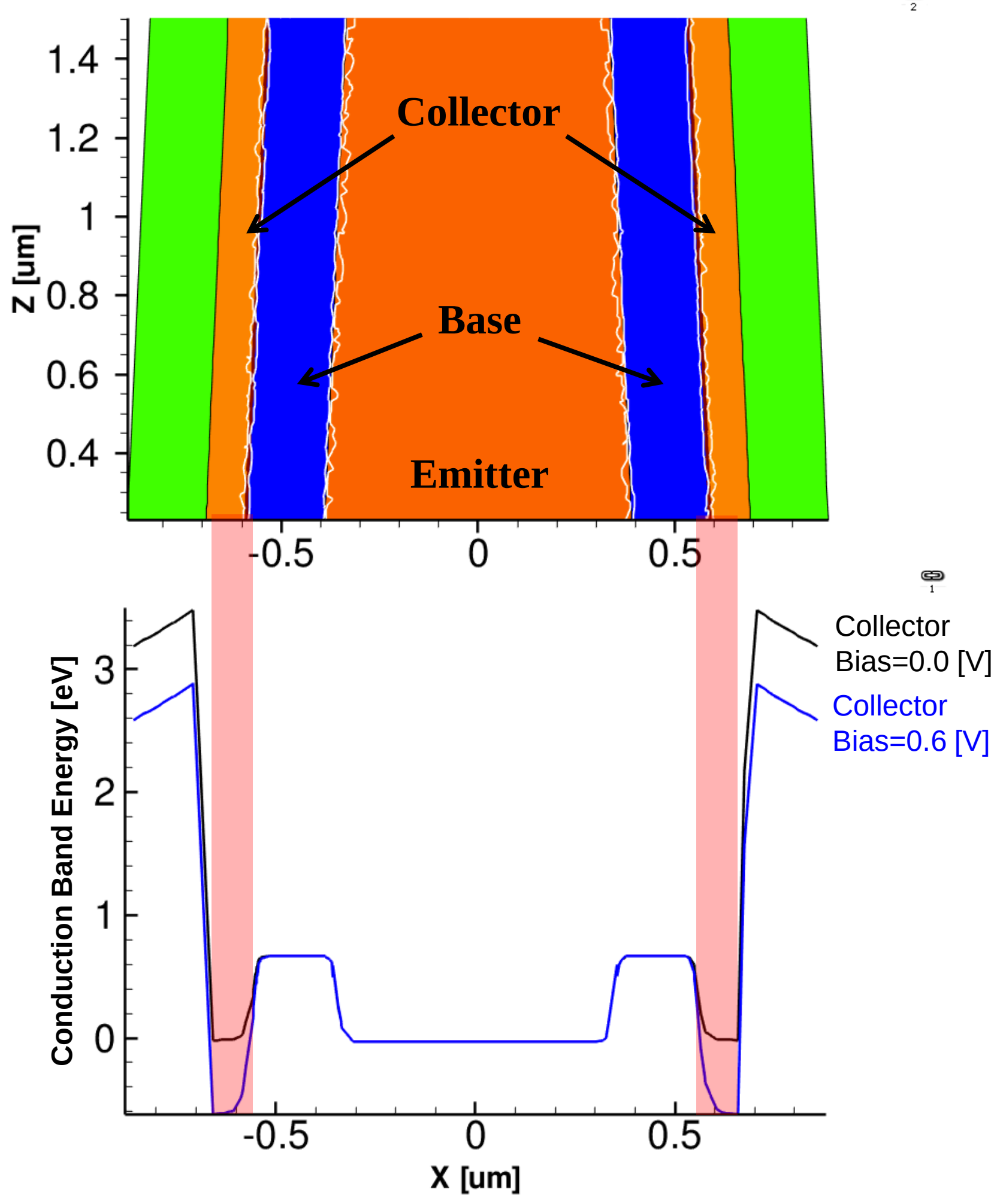
- **Due to nanopillar structure** large peaks in internal electric field are seen at pn interfaces
- **High gain** is predicted by high electric field peaks

## Nanopillar npn BJT



### *III-V Nanopillar BJT Design Schematic*

- Bipolar Junction Phototransistor **built into a nanopillar on silicon**



*Conduction Band Energy for BJT with Floating Base*

### *Conduction Band Energy*

- Band energy at zero bias looks as expected
- Band energy in the collector region drops when bias is applied to the collector
- **Collector side is responding properly**

## Conclusions and Future Work

- Nanopillar design allows for large internal electric fields, **predicting potential for high gain**
- Collector side of BJT nanopillar behaves expectedly under collector bias, **suggesting correct transistor action can be achieved with the nanopillar BJT**
- **Future work with optical bias on base will be conducted to verify correct transistor action**
- **Theoretical gain of the device will be calculated**
- **Sentaurus optimization of doping, pillar width and diameter, and SiO2 thickness will determine maximum possible gain**

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