Center for Energy Efficient Electronics Science

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Contact engineering of TMDC materials: Using Graphene at the TMDC/metal interface

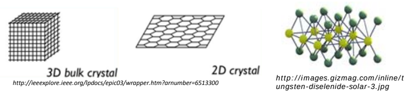
Christopher Gaytan[1]*, Tania Roy[2], Professor Ali Javey[2]

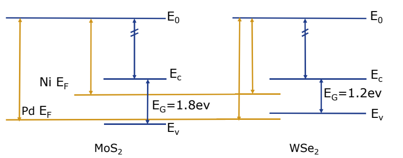
[1]The University of Texas at El Paso, cgaytan2@miners.utep.edu*

[2]Center, for Energy Efficient Electronics The University of California, Berkeley

Introduction

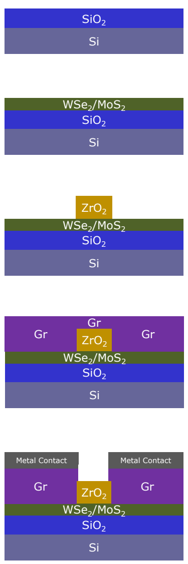
- 3 – Dimensional semiconductors reaching scaling limit
- 2– Dimensional semiconductors offer an attractive alternative
  - Atomically thin
  - Tunable band gap by the number of their layers
  - Absent of dangling bonds
  - Approach ideal subthreshold swing of 60mV/Dec (due to thermonic emission)





- Difficulty forming an ohmic contact with MoS_2 and WSe_2

Device Fabrication



1. Si/SiO_2 substrate (50nm oxide thickness)
2. Exfoliate WSe_2, MoS_2, & graphene
3. Deposit ZrO_2, & perform lift off
4. Dry transfer graphene
5. Dichloromethane (DCM) clean.
6. Metal Deposition and lift off.
7. O_2 plasma etching.

Contact Metal	Φ (eV)
Ni	5.24
Pd	5.40

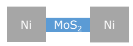
http://www.kayelaby.npl.co.uk/atomic_and_nuclear_physics/4_3/4_3.html

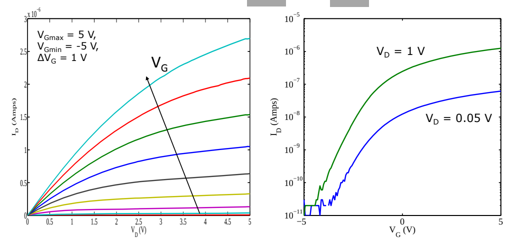
Abstract

Transition metal dichalcogenides (TMDC) materials MoS_2 and WSe_2 may be implemented for use in CMOS as n-type and p-type semiconductors. Although there is a challenge in forming a good electrical contact on these materials; traditional metals form a huge Schottky barrier due Fermi level pinning. To mitigate this behavior we use graphene as a lubricant layer between the TMDC material and our metal contacts: palladium and nickel. Ideally this method should decouple the TMDC material and contact resulting in an ohmic contact; unfortunately this is not the case and we still show Fermi level pinning.

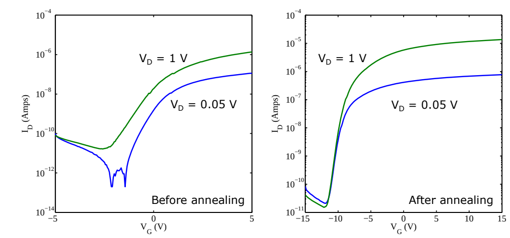
Results

MoS_2- Ni contacts

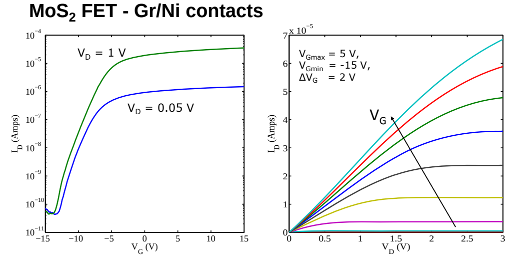


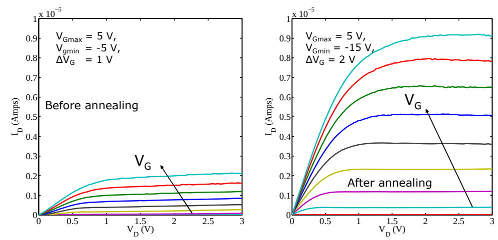


MoS_2 FET-Gr/Pd contact- Effect of Annealing

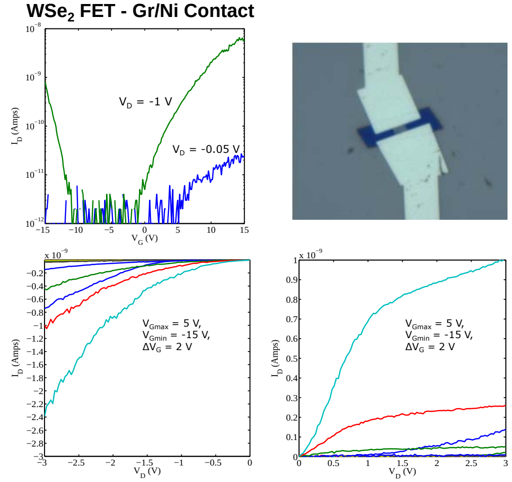


MoS_2 FET - Gr/Ni contacts

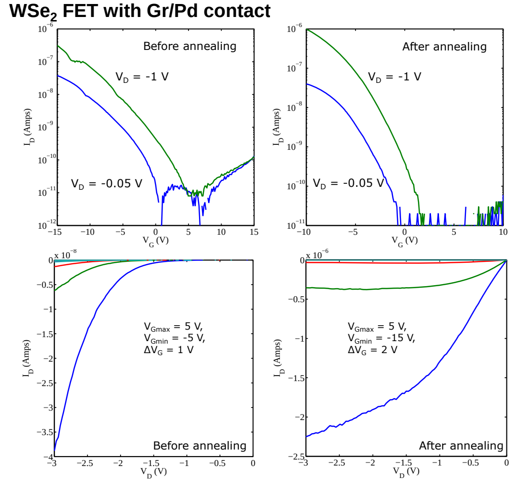




WSe_2 FET - Gr/Ni Contact



WSe_2 FET with Gr/Pd contact



Discussion

- MoS_2 FET with Ni contacts shows very strong n-type behavior, a strong indicator of conduction band (CB) pinning.
- MoS_2 FET with Gr/Ni contacts shows n-type behavior with a new V_t ~ -12V
- WSe_2 FET with Gr/Ni contacts shows ambipolar behavior with a high Schottky barrier for holes & low Schottky barrier for electrons
- MoS_2 FET with Gr/Pd contacts shows n-type behavior indicating Fermi level is pinned to CB. Annealing for 120 °C, 1 hr, in ambient air increased drain current by 350%
- WSe_2 FET with Gr/Pd contact shows p-type behavior. Annealing reduced Schottky barrier drastically. Current increased by a factor of 100X

MoS_2 Gr/Ni Contact	WSe_2 Gr/Ni Contact	MoS_2 Gr/Pd Contact	WSe_2 Gr/Pd Contact
μ = 70.8 cm^2/V*sec	TBD with Schottky Model	μ = 10.25 cm^2/V*sec μ_{Anneal} = 26.4 cm^2/V*sec	μ = 4.2 cm^2/V*sec μ_{Anneal} = 7.4 cm^2/V*sec

Conclusions & Future Work

Conclusions

- Fermi level unpinning does not occur with graphene layer at TMDC/metal interface
- MoS_2 with Ni: Graphene improves contact properties
- MoS_2 with Pd:
  - Device is n-type
  - Schottky barrier is absent
  - Annealing improves current and lowers Schottky barrier
- WSe_2 with Pd: Device is p-type, with low Schottky barrier at the contact
- WSe_2 with Ni:
  - Device is n-type
- Graphene + metal work function determines the effective work function of contact

Future Work

- Use other methods to unpin the Fermi level

References

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