Challenges in Sub-20nm Design

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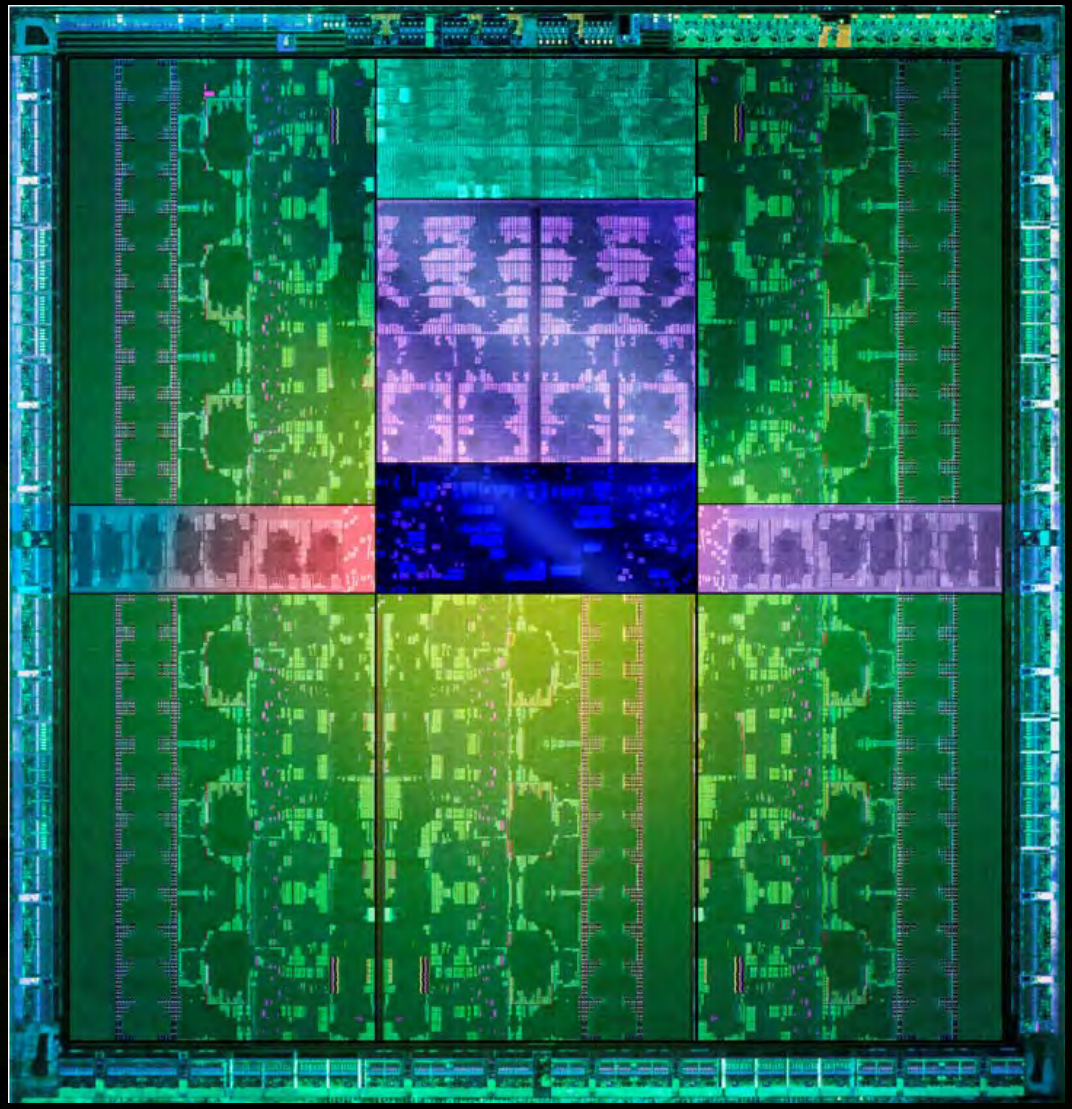
GK110 in Tesla K20X GPU Accelerator for High Performance Computing



- 2688 Processor cores
- 3.95 TFlops (FP32)
- 235 W

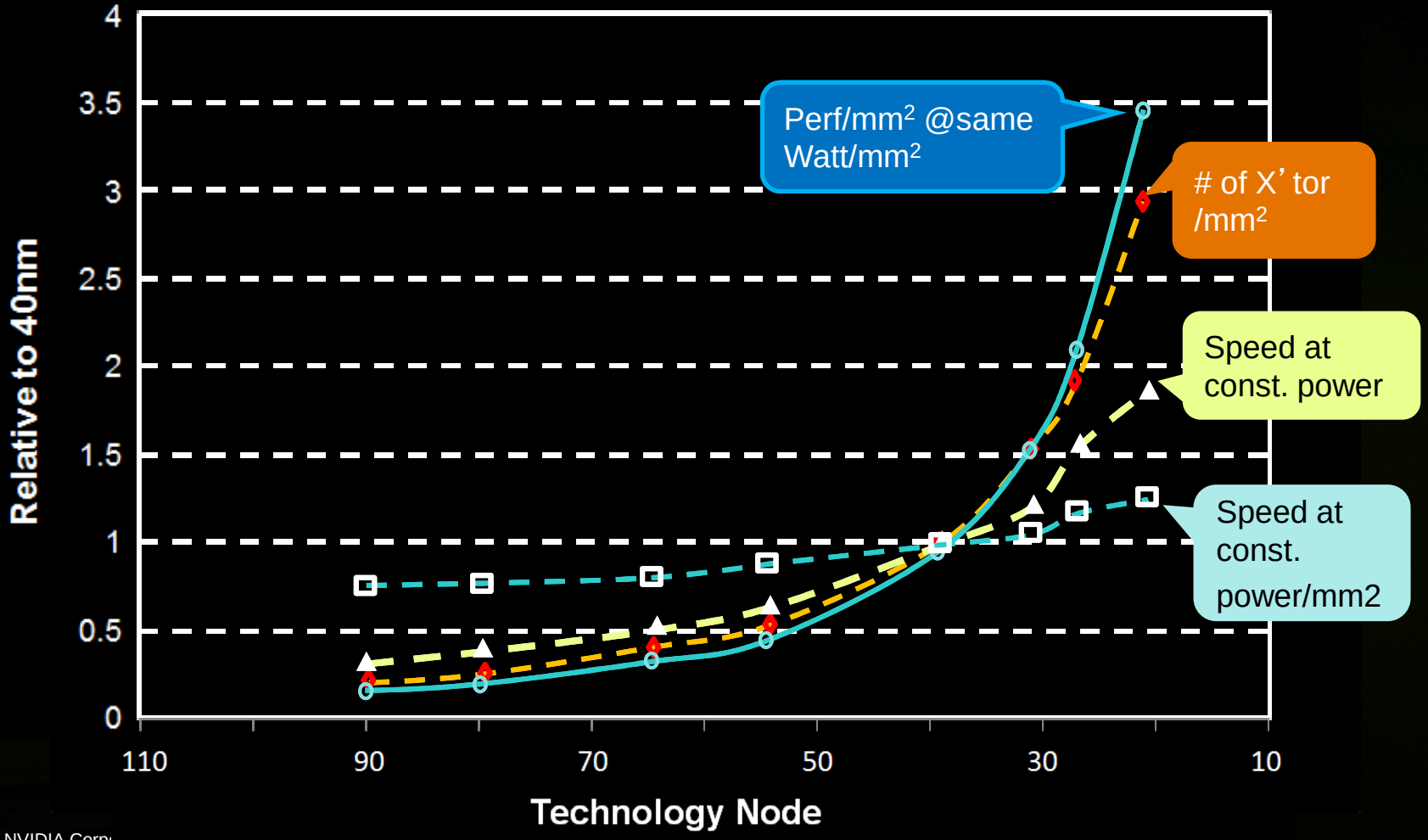
- 28nm HK/MG technology
- 7.1B X’tors
- >20km min. width interconnect
- >10B contacts
- >10B Vias

Sub-20nm Challenges

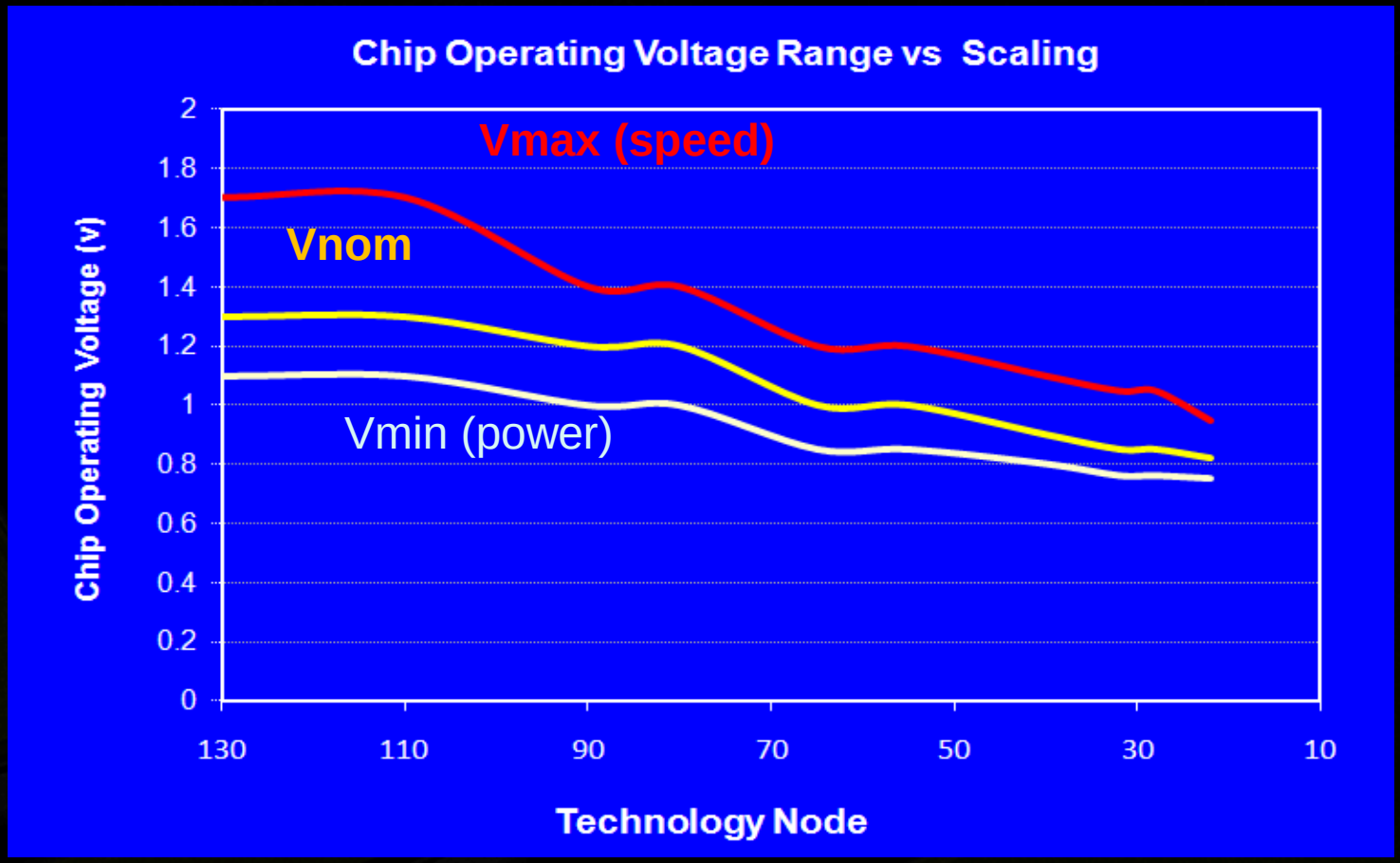
- **Performance**
- **Precision**
- **Perfection**

Max Performance within power constraint

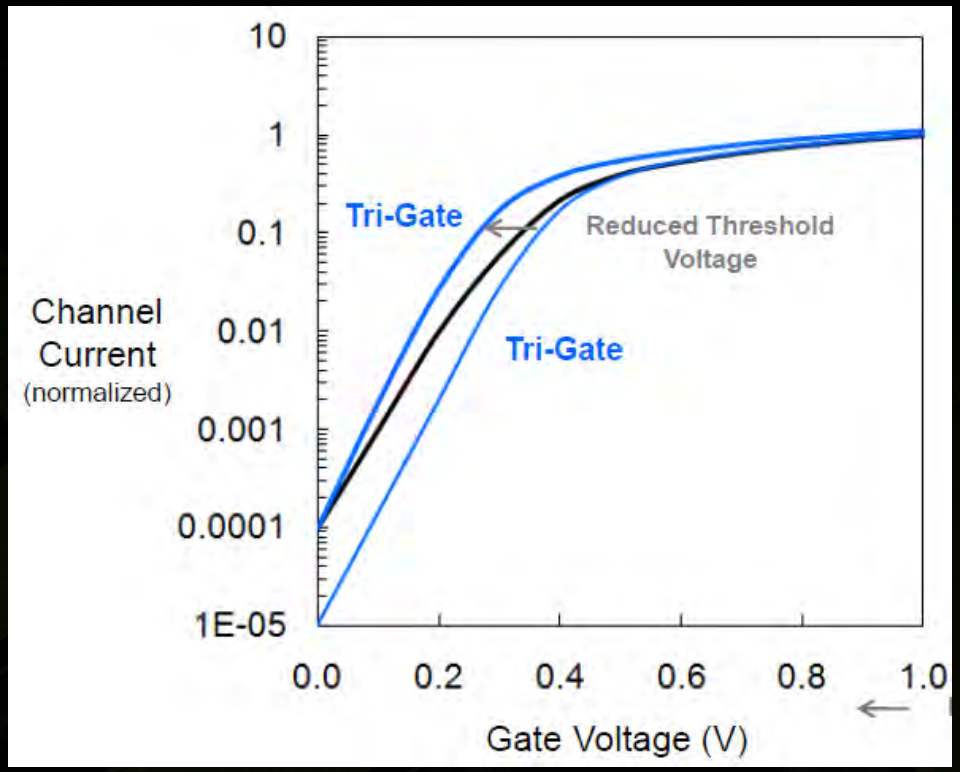
Performance/ChipArea = (# of X’tors/mm2) x circuit speed



Knob to optimize speed / power trade-off is diminishing

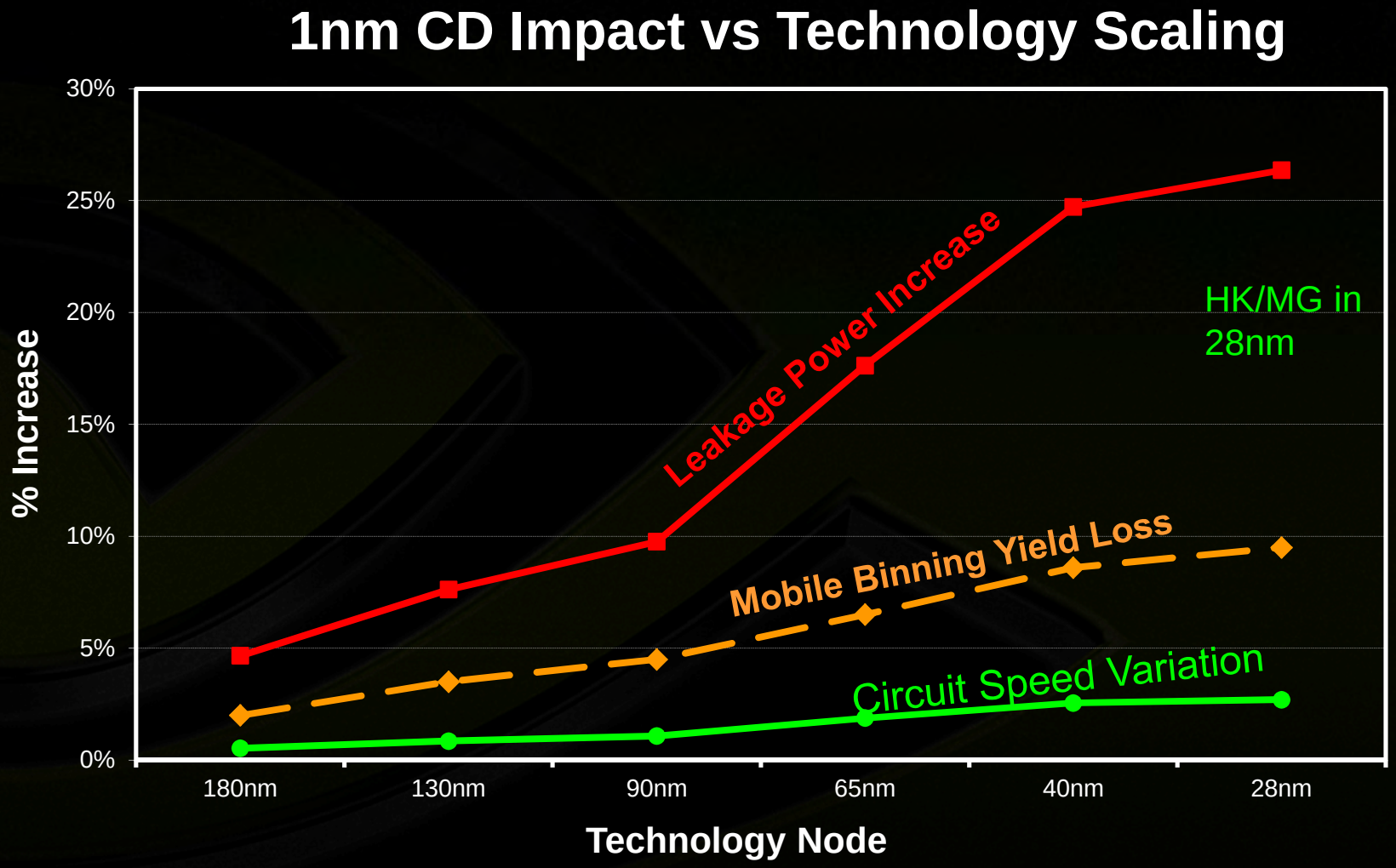


Performance Boost from FinFET



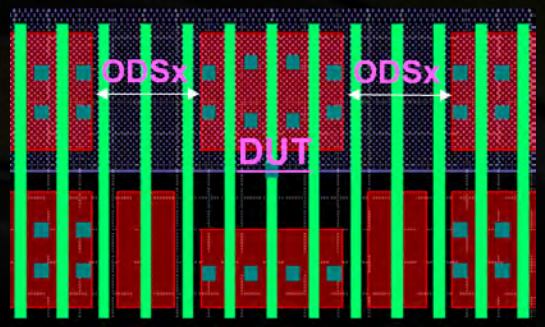
(Source: Intel website)

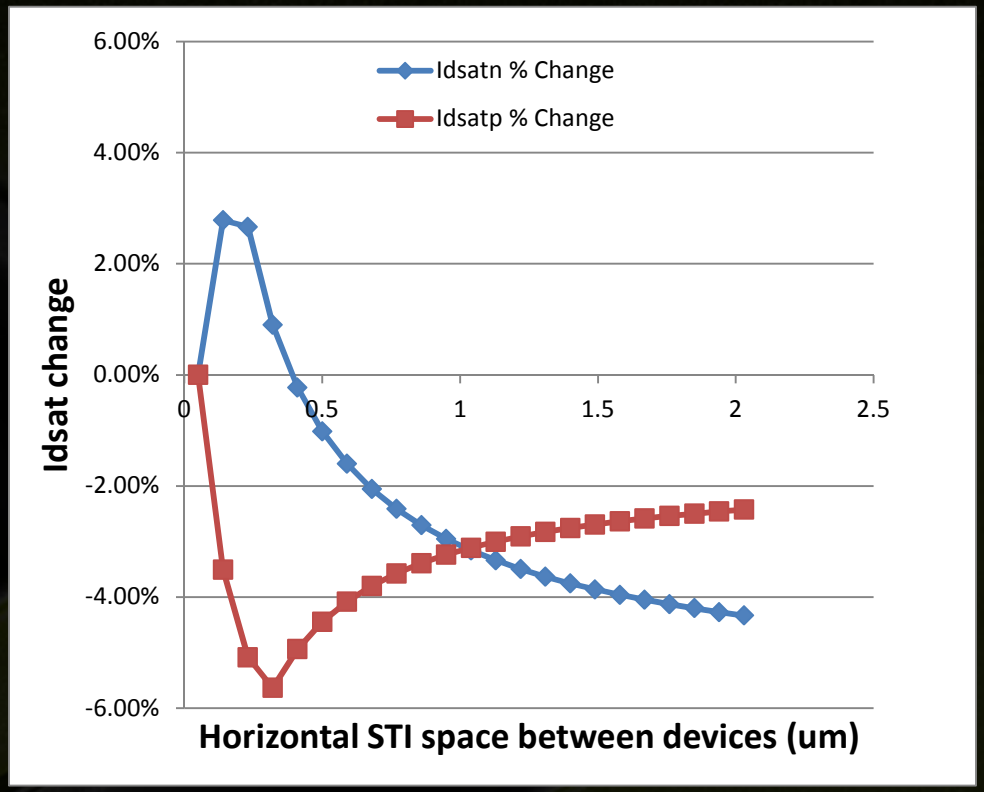
Impact of 1nm Lgate variation



Transistor Layout Effect

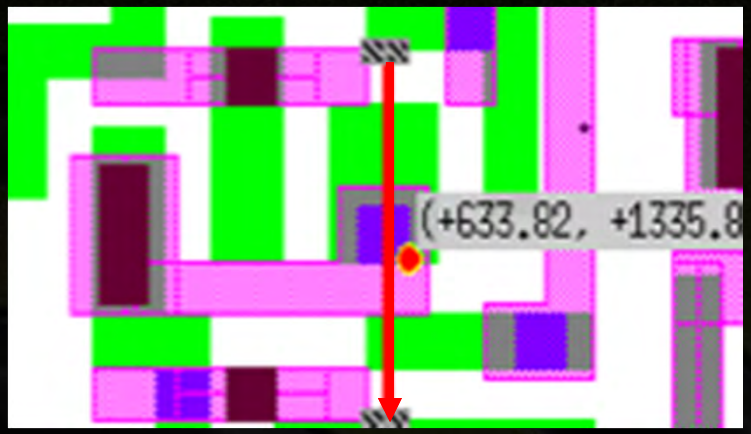
- Idsat & Vt depends on isolation space (ODSx) to adjacent active region

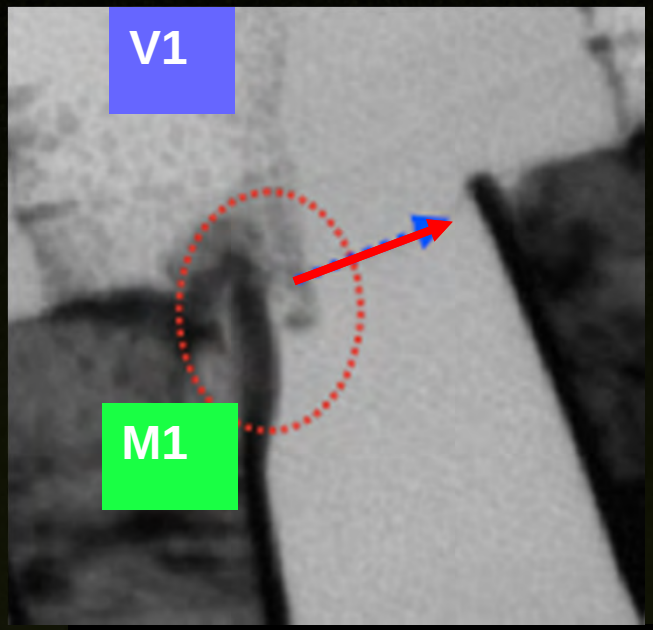




- Strain effect from shallow trench isolation liner & fill material
- Highly non-linear, changes from time to time, hard to model
- Layout effect widens the best/worst case variation in std.cell delay/power

Precision in CD and Overlay





Ref.1

Risk of V1 to M1 TDDB:

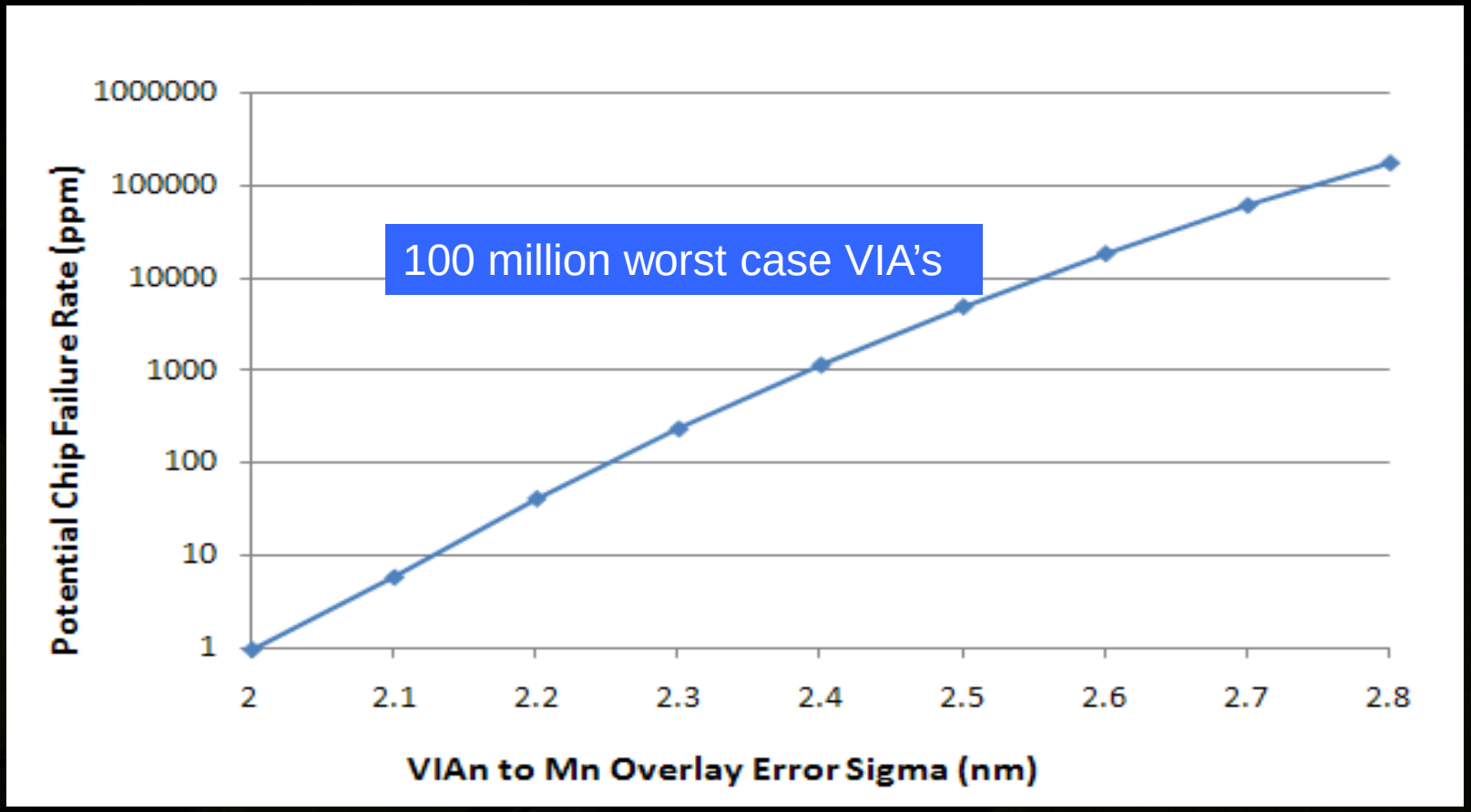
- V1 with zero M1 enclosure
- min space to adjacent M1 spacing
- large M2 enclosure of V1

Process control for sufficent V1-M1 space for yield & reliability:

- M1 CD
- V1 CD
- V1 to M1 overlay

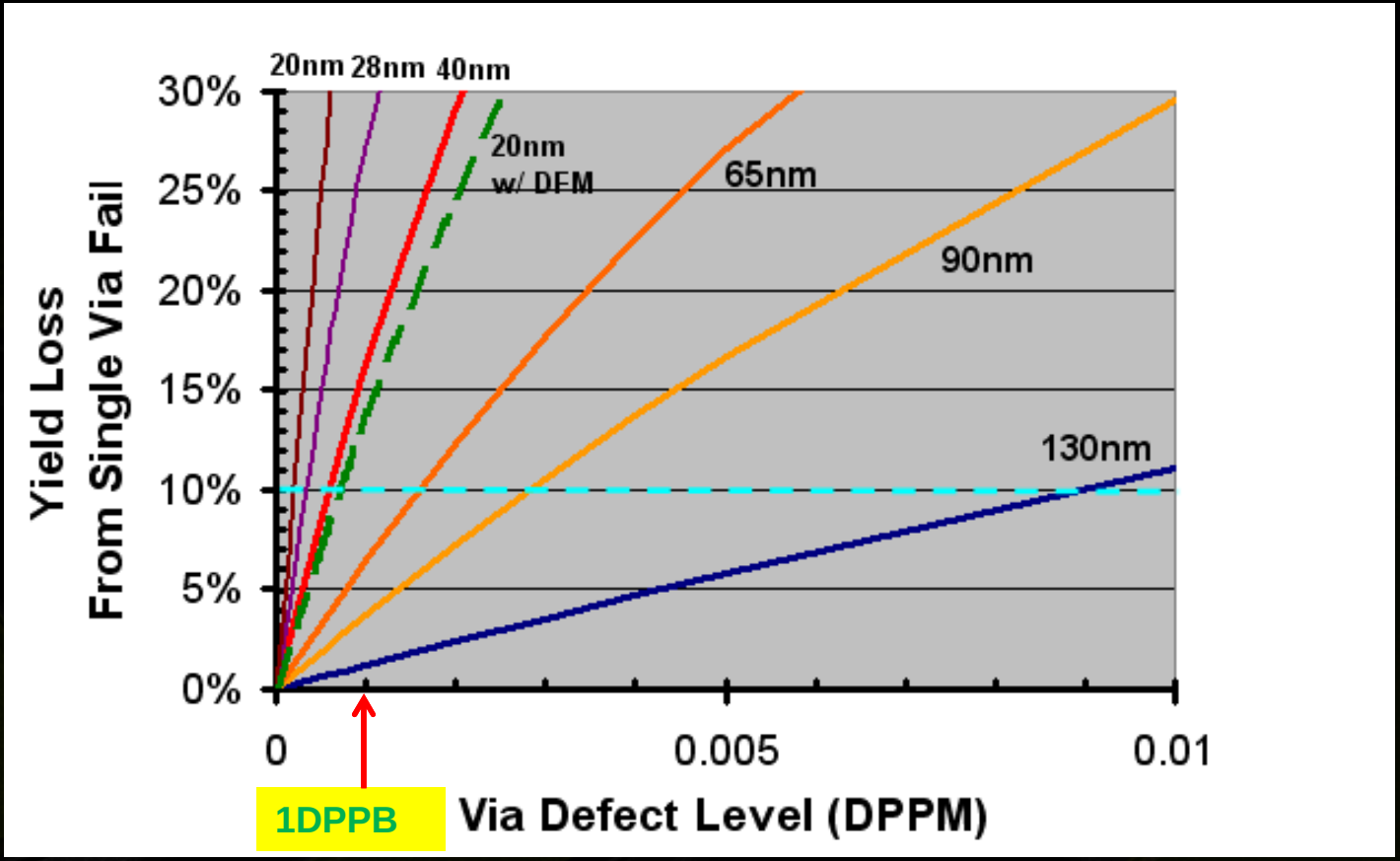
1. W.Liu, et al, "Study of TDDB reliability In misaligned via Chain structures," IRPS, p.3A.4.1 (2012)

Every tenth nm mis-alignment has huge effect to chip failure



Min Mn and VIAn in 20nm design
1 of Mn CD 1.4nm, 1 VIAn CD 2.0nm

Perfection in via defect control



Ref.1

Even with DFM practice: redundant via, rectangular via, via defect level needs to be < 0.5 DPPB!

1. J.Y. Chen, "GPU Technology Trends and Future Requirements," IEDM, p.1, 2009

Sub-20nm Challenges

- **Performance** -> transistor density x speed
- **Precision** in SPICE model, CD control & overlay
- **Perfection** defect density < 1 DPPB -> zero flaw