PROPLUS
The DFY Technology Provider

IC Design and EDA: View from Booming China

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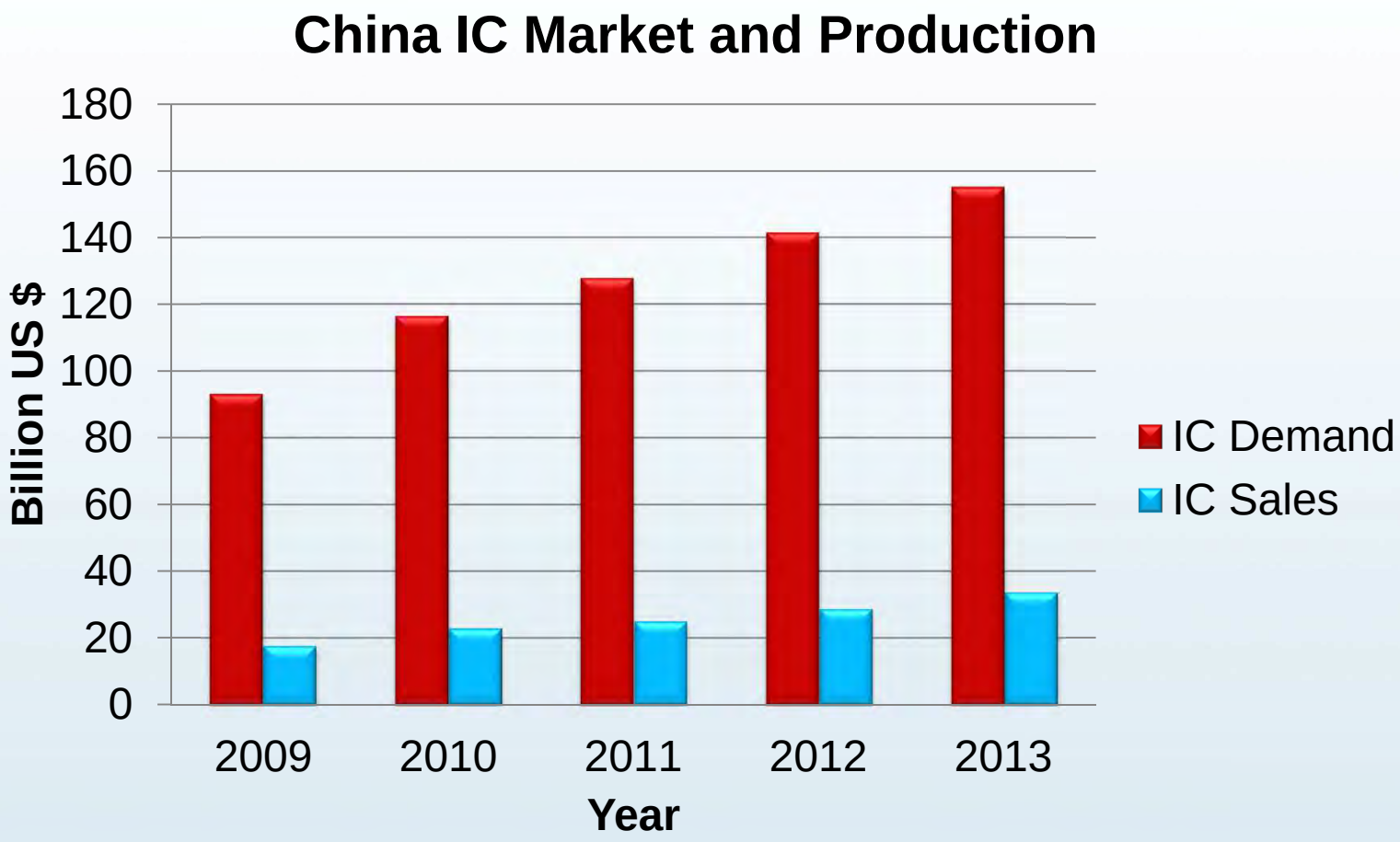
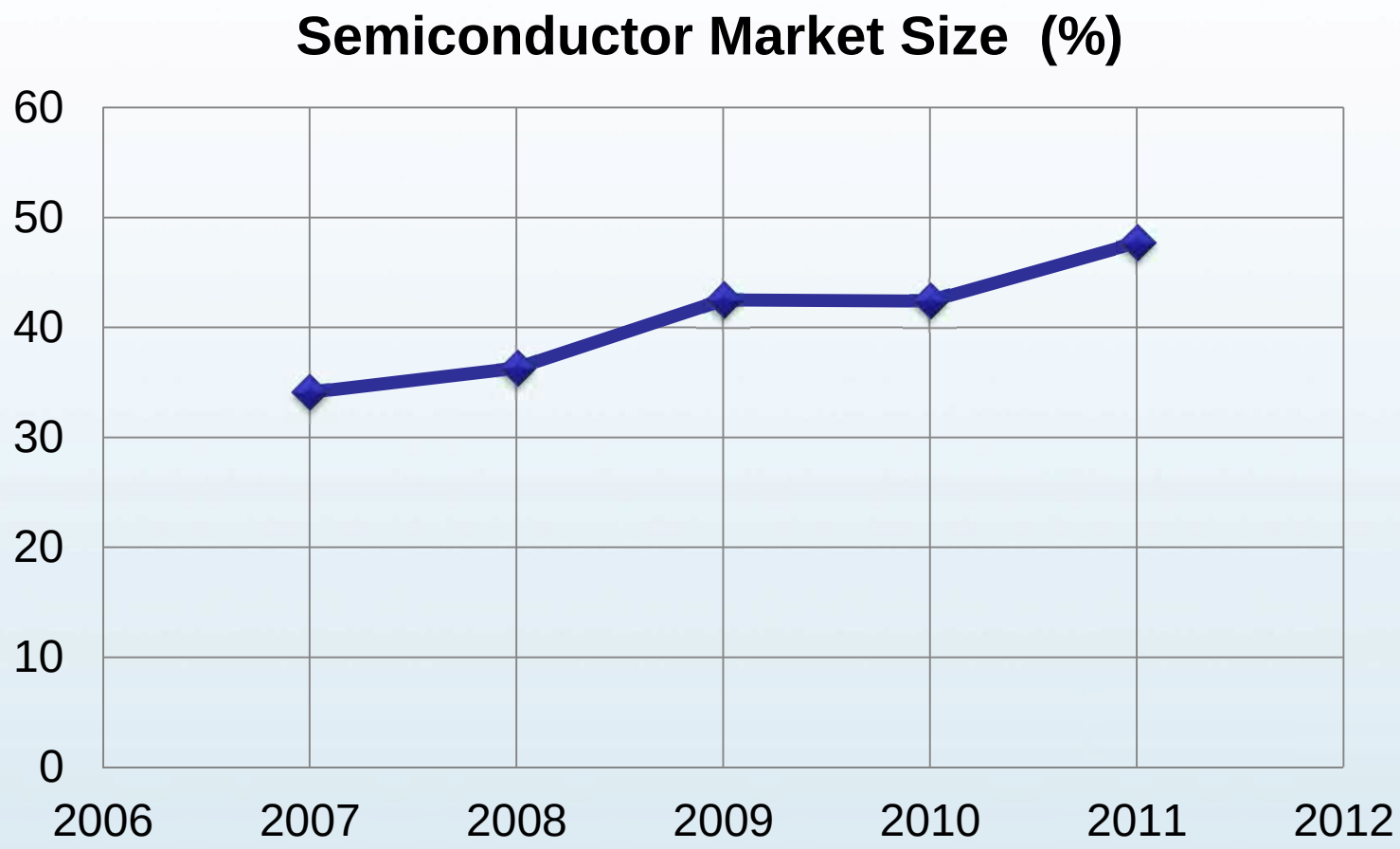
Outlines

- Brief introductions to China IC industry
- Current design ability of fabless companies in China
- The role of EDA, from China to the world
  - The importance of design flow and COT
  - DFY is not simply yield enhancement, but also opportunity and maintaining the competitiveness
  - What is ProPlus (and Chenming) doing in EDA

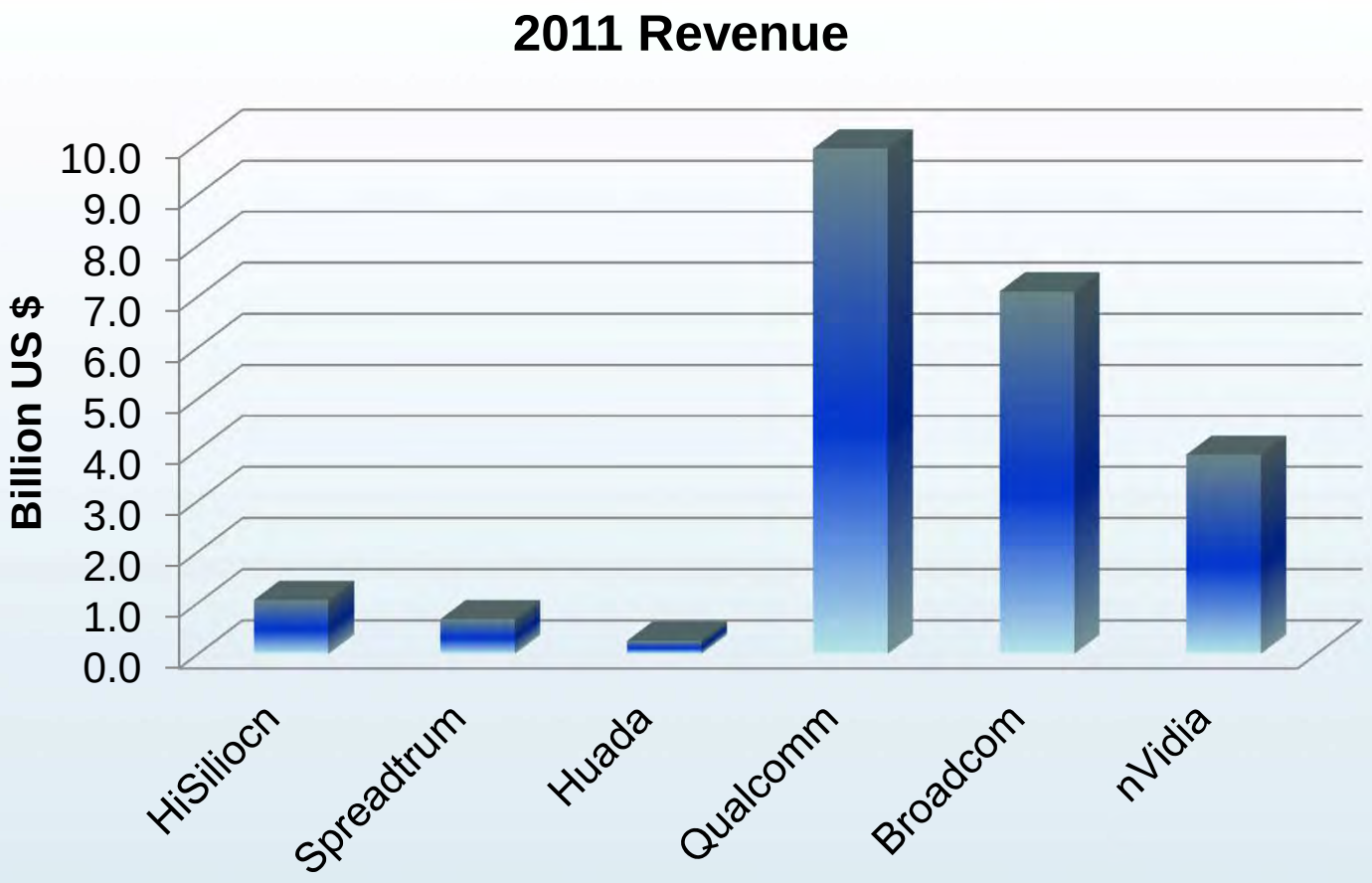
China IC Market Is Growing Steadily



China Market Size is Huge



However, China Not Yet a Main IC Supplier



Design Capability Limitation

- Lack of high end design capabilities
  - Largely rely on IP cores
  - Self core-IP creation is limited
  - Many is still playing the assembly games, the difference is what they assemble. It was Freezer and TV, now low-end ‘SOC’ with performance largely folded
- History of design creation is relative short
  - Lack of the necessary infrastructure (weak CAD , not pay attention to design flow and EDA tool investment)
  - Weak knowledge about IC foundation, partly (but very limitedly) improved by ‘returnees’ or foreign acquisitions

General Issues Related to EDA

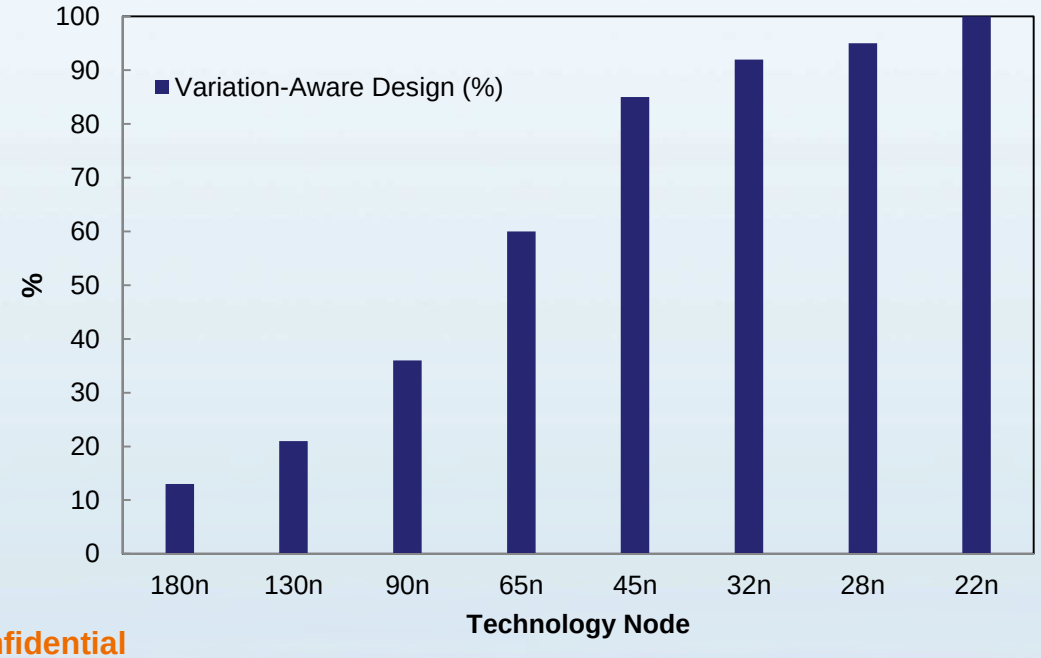
- Does not fully understand and utilize the PDK and Model information
- Not capable to customize or improve/integrate design flow with COT
- Limited knowledge for yield analysis, ie., MC, and/or design optimization, to trade of performance and yield
- Over design as not sure certain issues, ie., LDE, or reliability
  - Left the money on the table or not competitive performance on the same technology node
- High-end production yield is low, cost is high

What Designers Concern

- Process variations are increasing challenges
- Information provided by foundries are not enough or accurate
- DFY is must-have to achieve performance and yield trade-off, esp. at advanced nodes below 65nm
- EDA companies have not yet provided an integrated DFY solutions that make DFY more practical

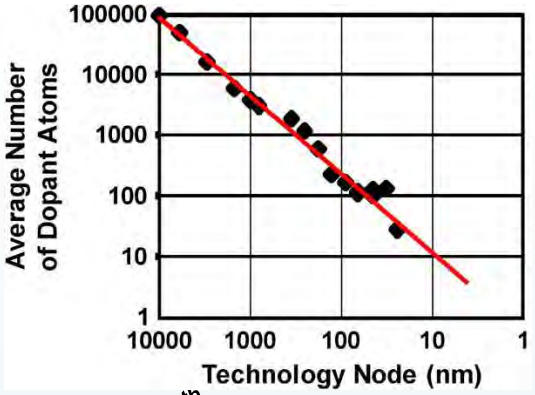
It Is Not Just Unique in China

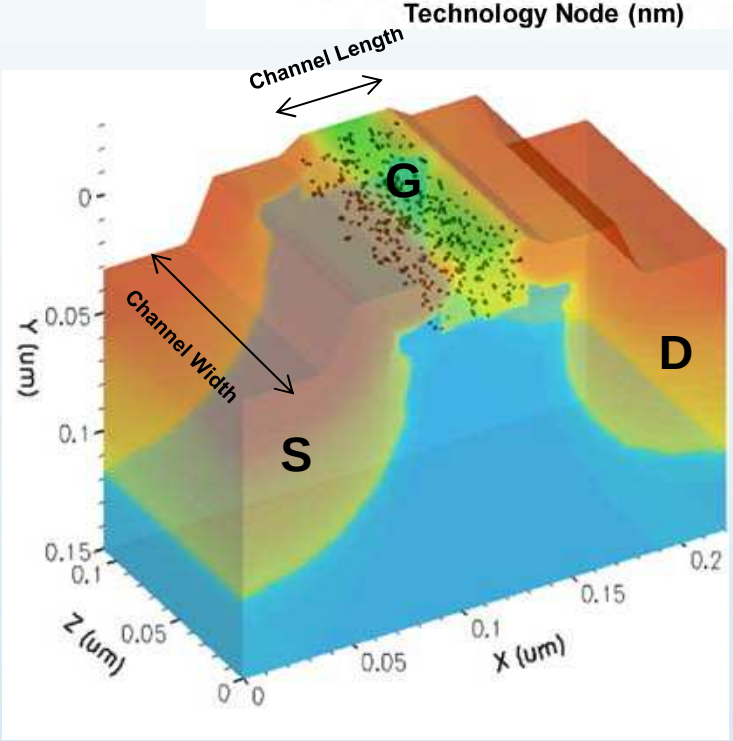
- A year 2011 independent survey revealed 65% engineers see variation as their top priority in the next 2 years
- Integration complexity and geometry shrinking led to higher variation design risk



Understand process variation

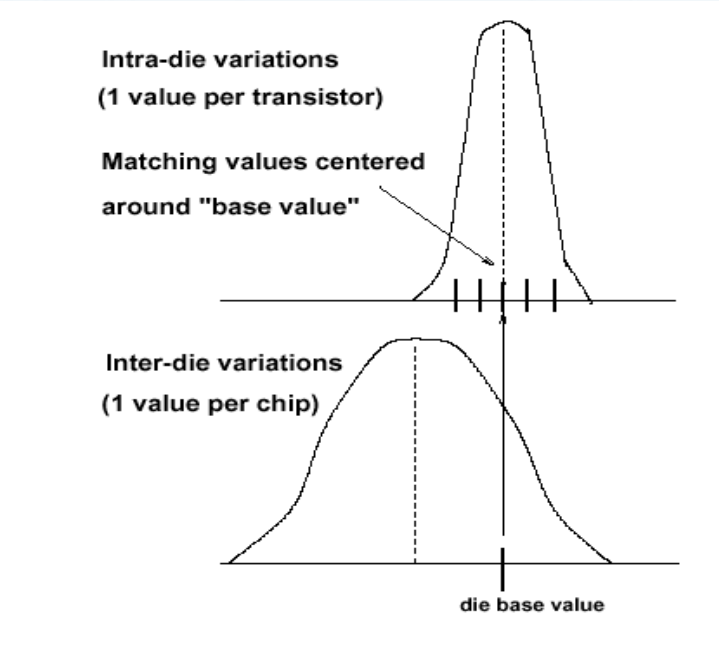
- Why process varies?
  - Device geometry changes with process
    - Litho process leads to what you drew is not what you get
    - L changes from device to device
  - Doping fluctuated as implementation volume getting less in the channel
    - V_{th} will changes from device to device
  - Nearby structure will affect device in concern: PLE
    - Distance to insulation sidewall: WPE
    - Contact to gate distance : LOD
    - Metal wire density: Micro-loading



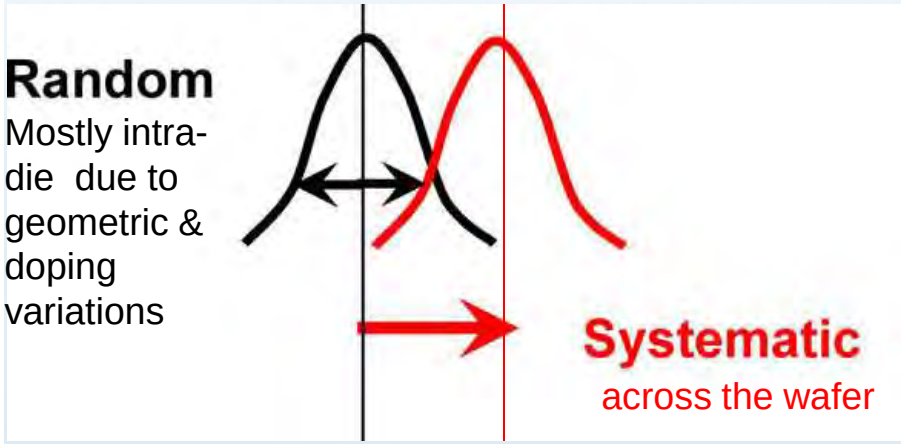


Understand process variation

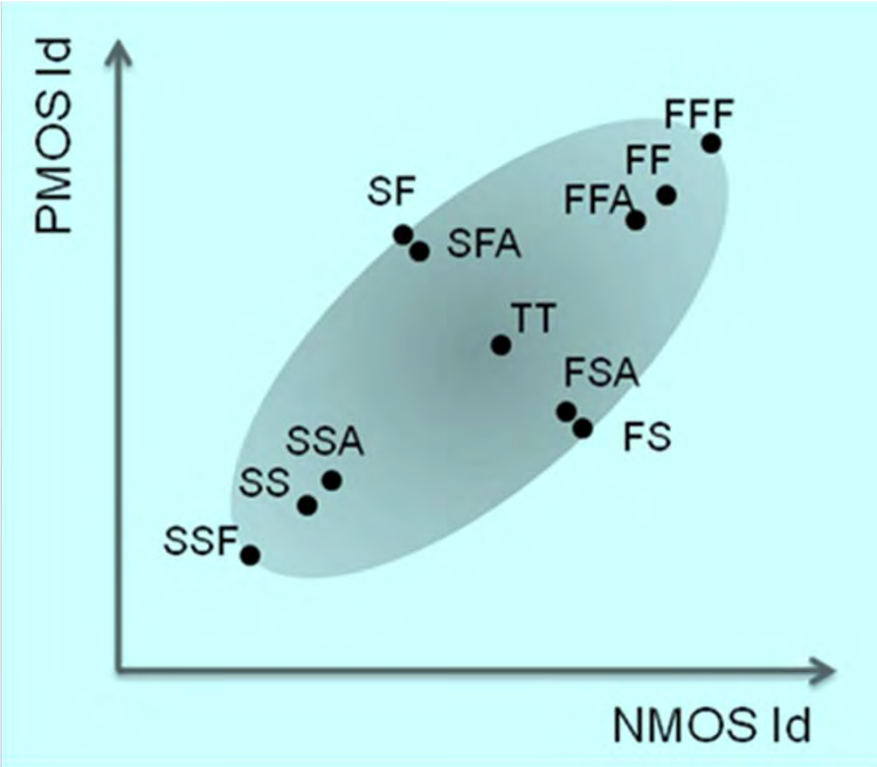
- Different type of variations
  - Local (intra-die, i.e., across the chip) vs. global (inter-die, i.e., wafer to wafer and die to die)
  - Random vs. systematic

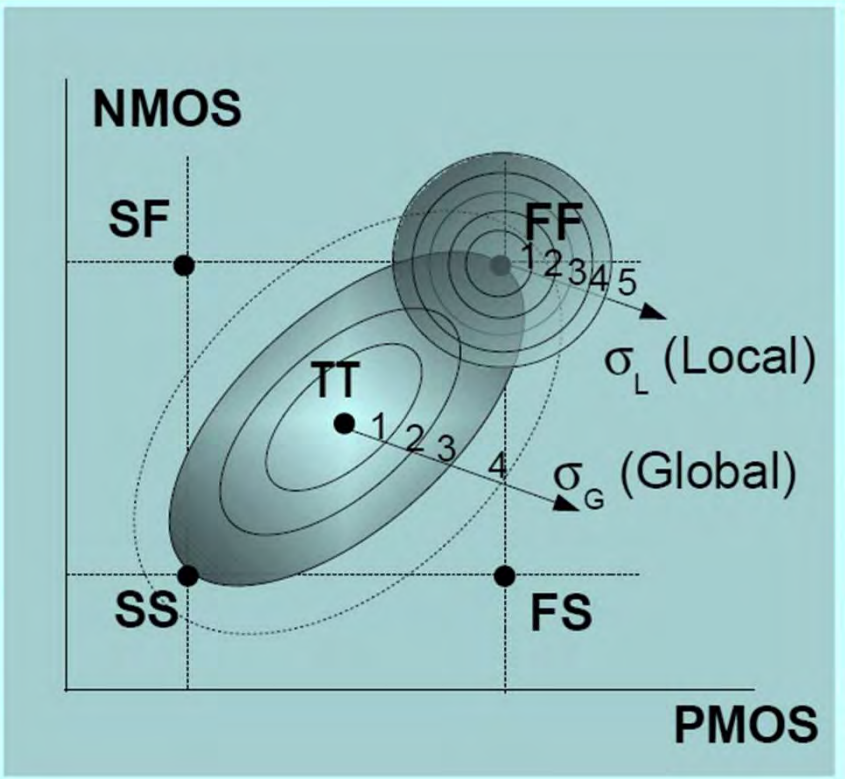


V_{th}, L



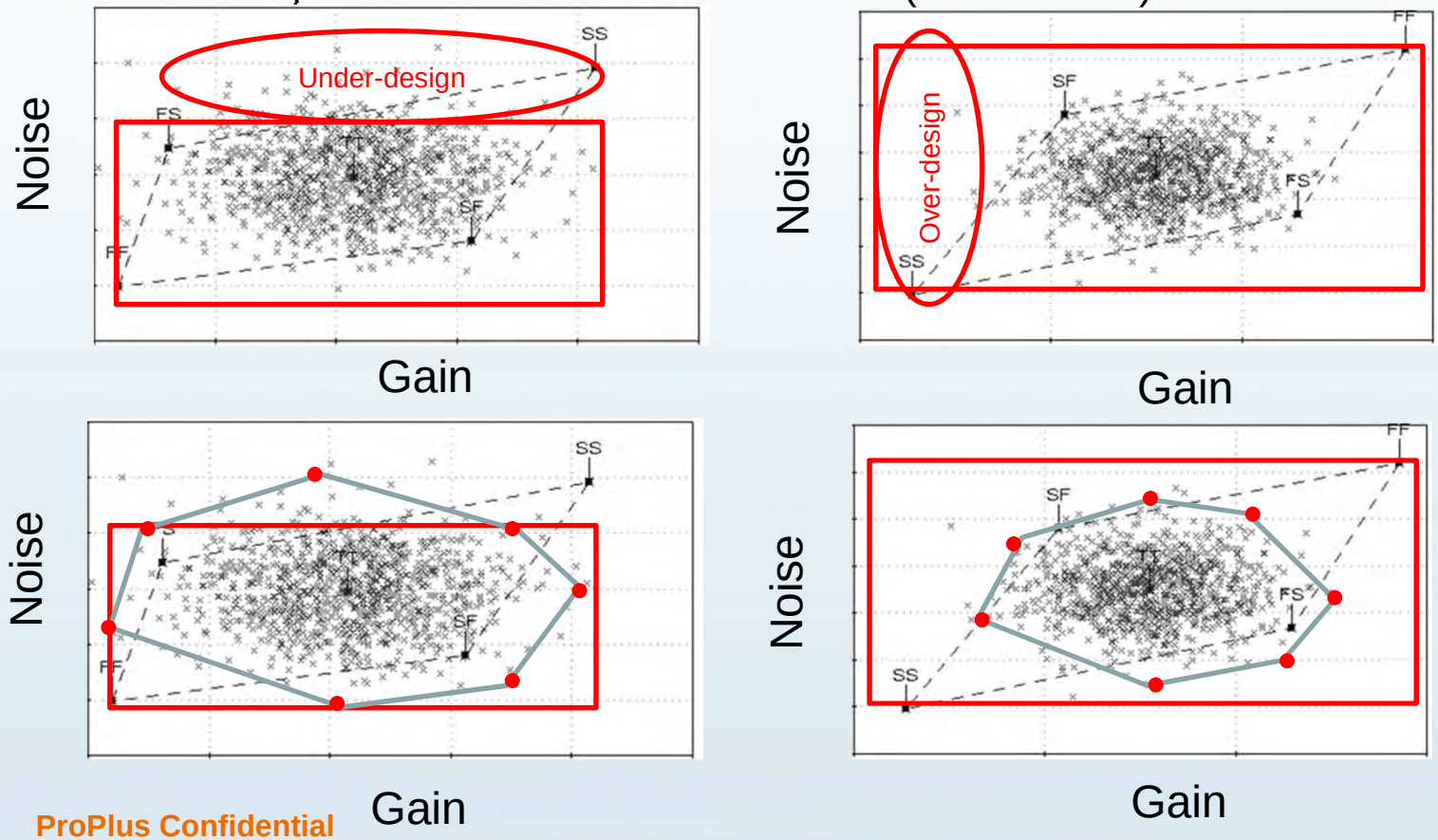
Corner Models Are Getting More Complicated





Why process variation a design challenge

- There needs for yield/performance trading off (Over design and waste time, or lower yield and performance)
  - PVT or performance corners or statistical (Monte-Carlo) simulations



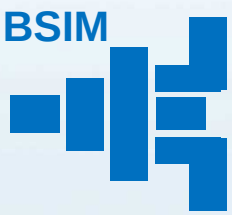
ProPlus Chartered To DFY Solutions

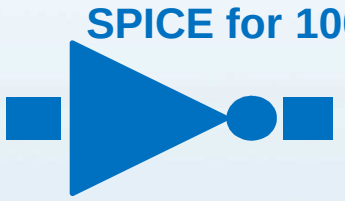
- Founded By Chenming's Team
  - Several Cory Hall guys from Chenming's team
    - Bruce: CTO, James: CEO
  - Of Course, Chenming as the Board member and one of the funding investors
- It has R&D centers in Beijing, Jinan and Shanghai
  - Keep growing for the past 3 years

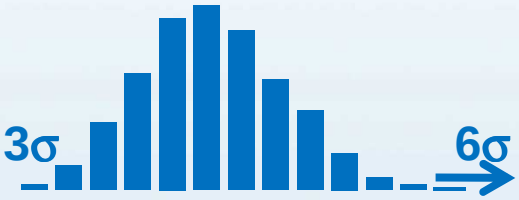
ProPlus Is Trying to Address Some of The Issues

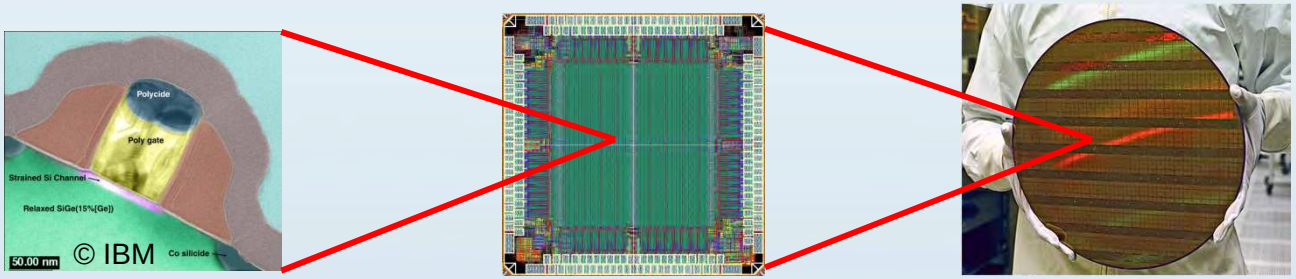
A complete silicon-to-silicon DFY flow

Silicon	BSIMProPlus™ Model Explorer™	NanoSpice™	NanoYield™ NanoExplorer™	Silicon
process ready	SPICE modeling & model validations	Circuit simulations & verifications	Design for yield & trade-off for PPA	meet spec & tape-out

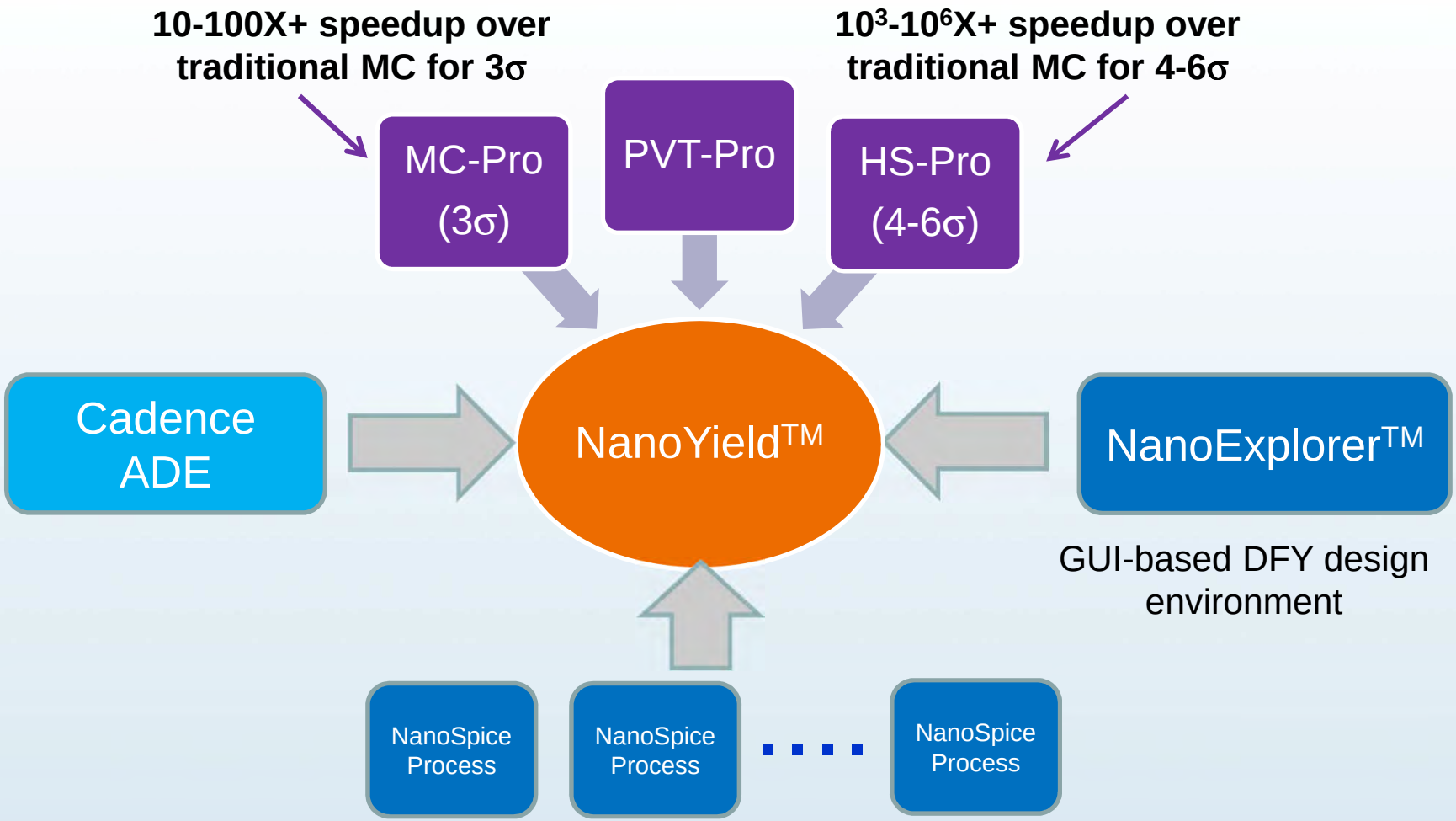






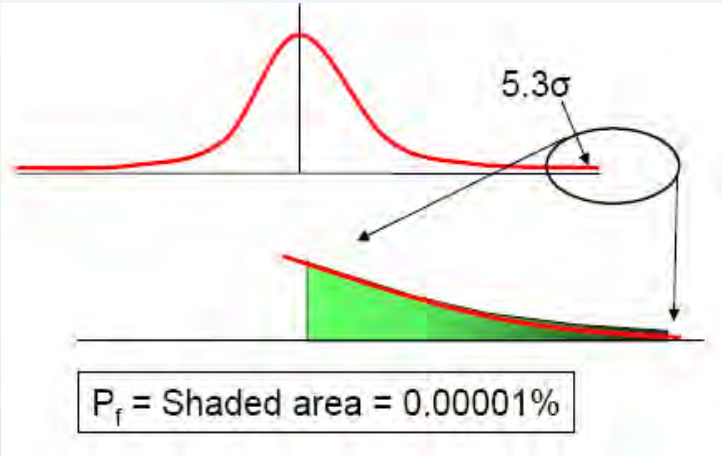


NanoYield™: An Integrated DFY Solution



NanoYield™ HS-Pro Technologies

- Fast and reliable yield prediction for high sigma problems
  - Memory or other Array: SRAM, eDRAM, Sense Amplifier, etc
  - Digital: Hit Logic, Flip-Flop, Standard Cells, etc
  - Hardware qualified by IBM for IBM servers and ASIC products for 5+ years



6T SRAM Bitcell 6σ Simulation
MC vs. HS-Pro

	# of Runs Required	Run Time
Monte Carlo	6.41e+09	454 days
HS-Pro	6024	36.9s

Case Study: SRAM Bitcell Design

Design Target

- Read noise margin<0.18V
- Bitcell yield target:

  99.999999 (6σ)
- 1M SRAM yield: 99%

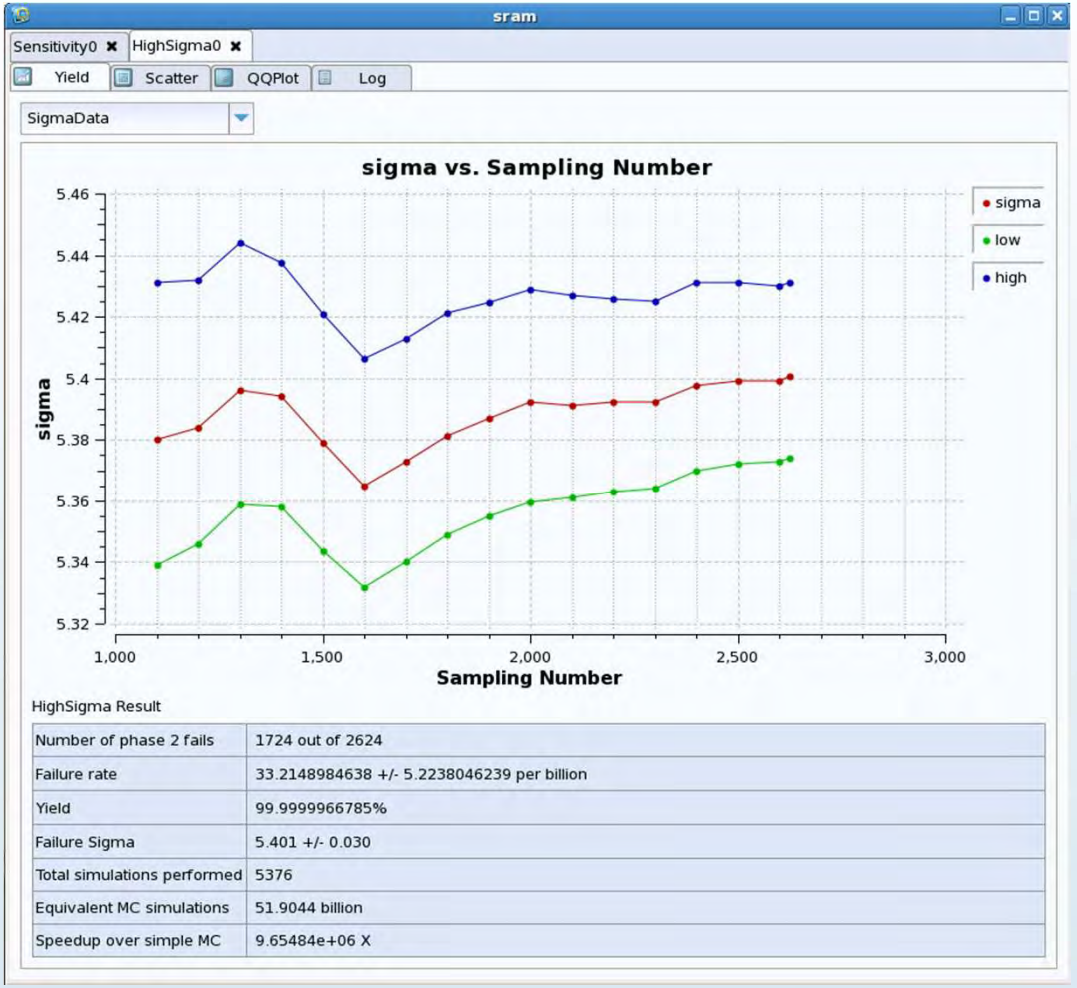
Yield Prediction

- Predicted yield:

  99.999997% (5.4σ)

Speedup over MC

- 9.65×10^6 times faster



HighSigma Result

Number of phase 2 fails	1724 out of 2624
Failure rate	33.2148984638 +/- 5.2238046239 per billion
Yield	99.9999966785%
Failure Sigma	5.401 +/- 0.030
Total simulations performed	5376
Equivalent MC simulations	51.9044 billion
Speedup over simple MC	9.65484e+06 X

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THANK YOU !

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